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Model No.: N154Z3 - L03 Approval

TFT LCD Approval Specification

MODEL NO.: N154Z3 - L03

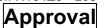
Customer :	Fujitsu	
Approved by :		
Note :		

記錄	工作	審核	角色	投票
2008-09-12 15:04:40 CST	PMMD III Director	annie_hsu(徐凡 琇/56522 / 54873)	Director	Accept

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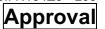
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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 3.0	Sep. 18,'08	All	All	Approval Specification was first issued.
		2		



1. GENERAL DESCRIPTION

1.1 OVERVIEW

N154Z3 - L03 is a 15.4" TFT Liquid Crystal Display module with single CCFL Backlight unit and 30 pins LVDS interface. This module supports 1680 x 1050 Wide-SXGA+ mode and can display 262,144 colors. The optimum viewing angle is at 6 o'clock direction. The inverter module for Backlight is not built in.

1.2 FEATURES

- Thin and High Brightness
- WSXGA+ (1680 x 1050 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 2 pixel/clock
- Meet RoHS requirement

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	331.2 (H) x 207.0 (V) (15.4 inch Diagonal)	mm	(1)
Bezel Opening Area	334.7 (H) x 210.5 (V)	mm	(1)
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1680 x 3 (RGB) x 1050	pixel	-
Pixel Pitch	0.1971 x 0.1971	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Hard coating (3H), Anti-glare	-	-

1.5 MECHANICAL SPECIFICATIONS

lt	Item		Min. Typ. Max.		Unit	Note
	Horizontal (H)	343.5	344	344.5	mm	
Module Size	Vertical (V)	221.5	222	222.5	mm	(1)
	Depth (D)		6.2	6.5	mm	
We	eight		515	530	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

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2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

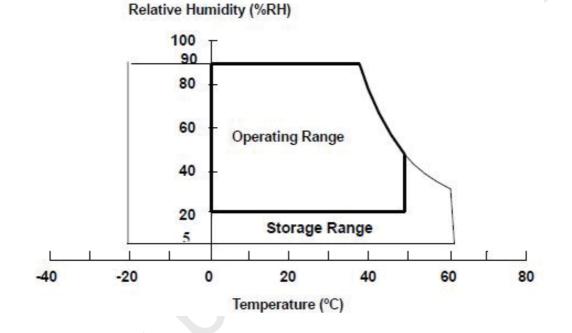
ltem	Svmbol	Va	lue	Unit	Note	
item	Symbol	Min.	Max.	Unit	NOLE	
Storage Temperature	T _{ST}	-20	+60	°C	(1)	
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)	
Shock (Non-Operating)	S _{NOP}	-	200/2	G/ms	(3), (5)	
Vibration (Non-Operating)	V _{NOP}	-	1.5	G	(4), (5)	

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta \leq 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation.



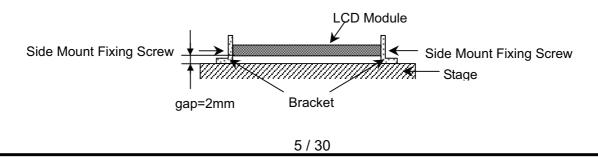
Note (2) The temperature of panel surface should be 0 °C Min. and 50 °C Max.

Note (3) 1 time for ± X, ± Y, ± Z. for Condition (200G / 2ms) is half Sine Wave,

Note (4) 10 ~ 200 Hz, 0.5 Hr / Cycle, 1 cycles for each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

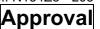
The fixing condition is shown as below:



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2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

		Value			
Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V _{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V _{IN}	-0.3	V _{CC} +0.3	V	(1)

2.2.2 BACKLIGHT UNIT

Item	Svmbol	Value		Unit	Note
nem	Symbol	Min.	Max.	Unit	Note
Lamp Voltage	VL		2.5K	V _{RMS}	(1), (2), I _L = 6.0 mA
Lamp Current	١L	3	7.0	mA _{RMS}	(1) (2)
Lamp Frequency	FL	40	80	KHz	(1), (2)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation

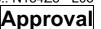
should be restricted to the conditions described under Normal Operating Conditions.

Specified values are for lamp (Refer to 3.2 for further information). Note (2)

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3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

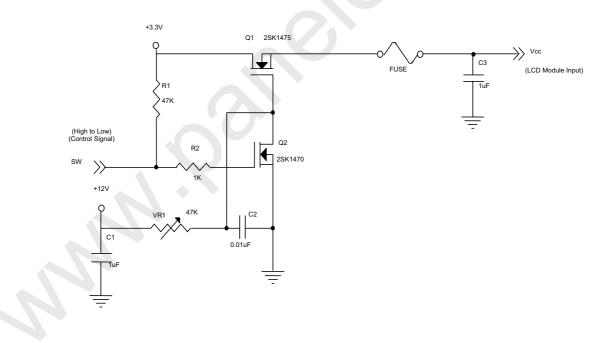
				Ta =	: 25 ± 2 ℃
Symbol		Value	Lloit	Note	
Symbol	Min.	Тур.	Max.	Onit	Note
Vcc	3.0	3.3	3.6	V	-
V_{RP}		50		mV	-
I _{RUSH}			1.5	Α	(2)
I _{IS}			1.0	Α	(2)
		350	380	mA	(3)a
LCC		490	520	mA	(3)b
$V_{\text{TH}(\text{LVDS})}$			+100	mV	(5), V _{CM} =1.2V
V _{TL(LVDS)}	-100			mV	(5) V _{CM} =1.2V
V _{CM}	1.125		1.375	V	(5)
V _{ID}	100		600	mV	(5)
R _T		100		Ohm	
P _{EBL}	-	3.63		W	(4)
	$\begin{array}{c c} & V_{RP} \\ \hline V_{RP} \\ \hline I_{RUSH} \\ \hline I_{IS} \\ \hline \\ Lcc \\ \hline \\ V_{TH(LVDS)} \\ \hline \\ V_{TL(LVDS)} \\ \hline \\ V_{CM} \\ \hline \\ V_{ID} \\ \hline \\ R_{T} \\ \end{array}$	$\begin{tabular}{ c c c c c } \hline V_{CC} & 3.0 \\ \hline V_{RP} & & \\ \hline I_{RUSH} & & \\ \hline I_{IS} & & \\ \hline & Lcc & & \\ \hline & & \\ \hline & & \\ \hline & & \\ \hline & & \\ V_{TH(LVDS)} & & \\ \hline & & \\ \hline & & \\ V_{TL(LVDS)} & -100 \\ \hline & & \\ \hline & & \\ \hline & & \\ V_{CM} & & 1.125 \\ \hline & & \\ \hline & & \\ V_{ID} & & 100 \\ \hline & & \\ R_{T} & & \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c } \hline Symbol & \hline Min. & Typ. \\ \hline Vcc & 3.0 & 3.3 \\ \hline V_{RP} & 50 \\ \hline I_{RUSH} & & & \\ \hline I_{IS} & & & \\ \hline & Lcc & & 350 \\ \hline & & 490 \\ \hline V_{TH(LVDS)} & & & \\ \hline V_{TL(LVDS)} & -100 \\ \hline & V_{CM} & 1.125 \\ \hline & V_{ID} & 100 \\ \hline & R_T & 100 \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c c } \hline Symbol & \hline Min. & Typ. & Max. \\ \hline Vcc & 3.0 & 3.3 & 3.6 \\ \hline V_{RP} & 50 & & & \\ \hline I_{RUSH} & & 1.5 & \\ \hline I_{IS} & & 1.0 & & \\ \hline Lcc & 350 & 380 & \\ \hline & 490 & 520 & & \\ \hline V_{TH(LVDS)} & -100 & & +100 & \\ \hline V_{TL(LVDS)} & -100 & & & \\ \hline V_{CM} & 1.125 & 1.375 & \\ \hline V_{ID} & 100 & 600 & \\ \hline R_T & 100 & & \\ \hline \end{tabular}$	$\begin{tabular}{ c c c c c c } \hline Symbol & \hline Value & Unit \\ \hline Min. & Typ. & Max. \\ \hline Min. & Typ. & Max. \\ \hline W_{RP} & 50 & mV \\ \hline V_{RP} & 50 & mV \\ \hline I_{RUSH} & 1.5 & A \\ \hline I_{IS} & 1.0 & A \\ \hline Lcc & 350 & 380 & mA \\ \hline V_{TH(LVDS)} & -100 & F100 & mV \\ \hline V_{TL(LVDS)} & -100 & mV \\ \hline V_{CM} & 1.125 & 1.375 & V \\ \hline V_{ID} & 100 & 600 & mV \\ \hline R_T & 100 & Ohm \\ \hline \end{tabular}$

Note (1) The ambient temperature is Ta = 25 ± 2 °C.

Note (2) IRUSH: the maximum current when VCC is rising

 $I_{\mbox{\scriptsize IS}}$ the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black.



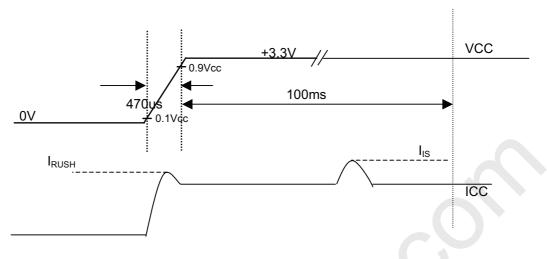
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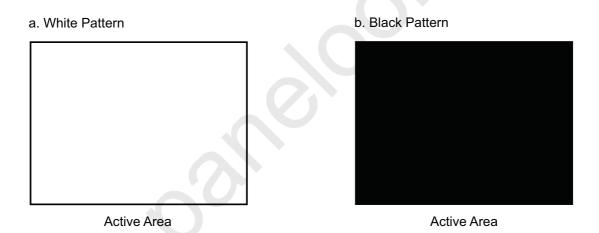


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Vcc rising time is 470us

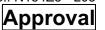


Note (3) The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2 °C, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.



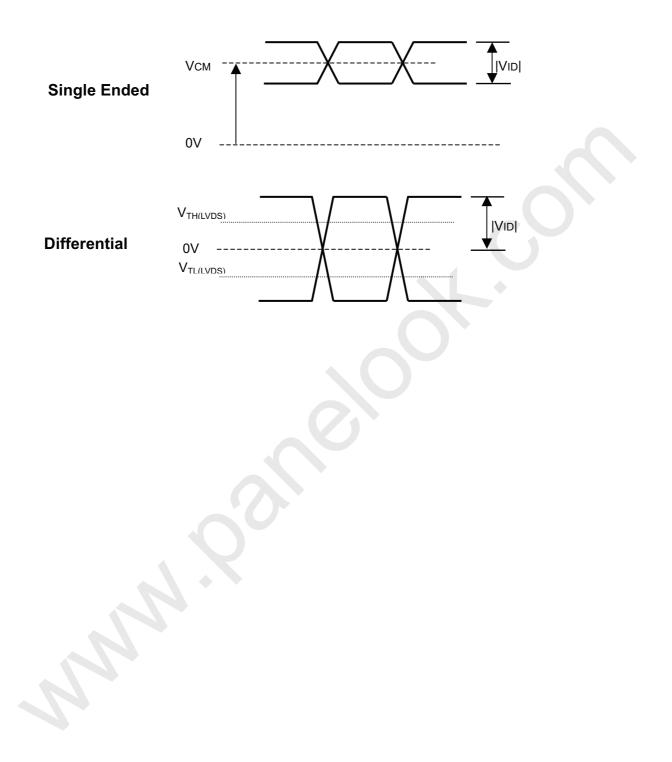
- Note (4) The specified power are the sum of LCD panel electronics input power and the inverter input power. Test conditions are as follows.
 - (a) Vcc = 3.3 V, Ta = 25 ± 2 °C, f_v = 60 Hz,
 - (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
 - (c) Luminance: 60 nits..
 - (d) The inverter used is provided from <u>Sumida</u>. Please contact them for detail information. CMO doesn't provide the inverter in this product.





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Note (5) The parameters of LVDS signals are defined as the following figures.



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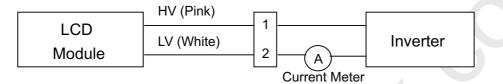
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3.2 BACKLIGHT UNIT

2 BACKLIGHT UNIT		Ta = 25 ± 2 °C				
Parameter	Symbol		Value		Unit	Note
raiametei	Symbol	Min.	Тур.	Max.	Unit	NOLE
Lamp Input Voltage	VL	675	730	945	V _{RMS}	I _L = 6.0 mA
Lamp Current	١L	2.0	6.0	6.5	mA _{RMS} -	(1),(2)
Lamp Guneni		3.0	0.0			(1),(3)
Lamp Turn On Voltage	Vs			1000 (0 °C)	V_{RMS}	(4)
Operating Frequency	F∟	40		80	KHz	(5)
Lamp Life Time	L _{BL}	15,000			Hrs	(7)
Power Consumption	PL		4.38		W	(4), I _L = 6.0 mA

Note (1) Lamp current is measured by utilizing a high frequency current meter as shown below:



Note (2) for burst mode inverter design

Note (3) for continuous mode inverter design

- Note (4) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.
- Note (5) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (6) $P_L = I_L \times V_L$

- Note (7) The lifetime of lamp can be defined as the time in which it continues to operate under the condition Ta = 25 \pm 2 °C and I_L = 6.0 mArms until one of the following events occurs:
 - (a) When the brightness becomes or lower than 50% of its original value.
 - (b) When the effective ignition length becomes or lower than 80% of its original value.
 - (The effective ignition length is a scope that luminance is over 70% of that at the center point.)
- Note (8) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid generating too much current leakage from high voltage output of the inverter. When designing or ordering the

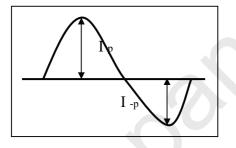


inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter, which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

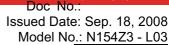
Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

- a. The asymmetry rate of the inverter waveform should be 10% below;
- b. The distortion rate of the waveform should be within $\sqrt{2 \pm 10\%}$;
- c. The ideal sine wave form shall be symmetric in positive and negative polarities.



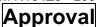
 * Asymmetry rate: | I _p – I _{-p} | / I_{rms} * 100%
* Distortion rate I _p (or I _{-p}) / I_{rms}

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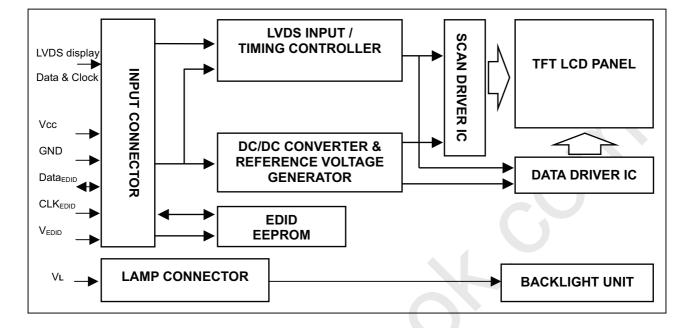
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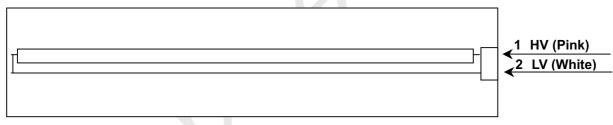
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4. BLOCK DIAGRAM

4.1 TFT LCD MODULE

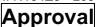


4.2 BACKLIGHT UNIT



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5. INPUT TERMINAL PIN ASSIGNMENT

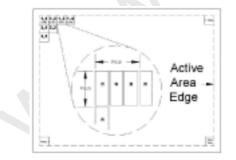
5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Vss	Ground		
2	V _{cc}	Power Supply +3.3 V (typical)		
3	V _{cc}	Power Supply +3.3 V (typical)		
4	V _{EDID}	DDC 3.3V Power		
5	NC	Non-Connection		
6	CLK _{EDID}	DDC Clock		
7	DATA _{EDID}	DDC Data		
8	RXO0-	LVDS Differential Data Input (Odd)	Negative	
9	RXO0+	LVDS Differential Data Input (Odd)	Positive	
10	Vss	Ground		
11	RXO1-	LVDS Differential Data Input (Odd)	Negative	
12	RXO1+	LVDS Differential Data Input (Odd)	Positive	
13	Vss	Ground		
14	RXO2-	LVDS Differential Data Input (Odd)	Negative	
15	RXO2+	LVDS Differential Data Input (Odd)	Positive	
16	Vss	Ground		
17	RXOC-	LVDS Clock Data Input (Odd)	Negative	
18	RXOC+	LVDS Clock Data Input (Odd)	Positive	
19	Vss	Ground		
20	RXE0-	LVDS Differential Data Input (Even)	Negative	
21	RXE0+	LVDS Differential Data Input (Even)	Positive	
22	Vss	Ground		
23	RXE1-	LVDS Differential Data Input (Even)	Negative	
24	RXE1+	LVDS Differential Data Input (Even)	Positive	
25	Vss	Ground		
26	RXE2-	LVDS Differential Data Input (Even)	Negative	
27	RXE2+	LVDS Differential Data Input (Even)	Positive	
28	Vss	Ground		
29	RXEC-	LVDS Clock Data Input (Even)	Negative	
30	RXEC+	LVDS Clock Data Input (Even)	Positive	

Note (1) Connector Part No.: JAE FI-XB30SL-HF10 or equivalent

Note (2) User's connector Part No: FI-X30M or equivalent

Note (3) The first pixel is odd as shown in the following figure.



Note (4) Mounting inclination of a connector carries out as fol



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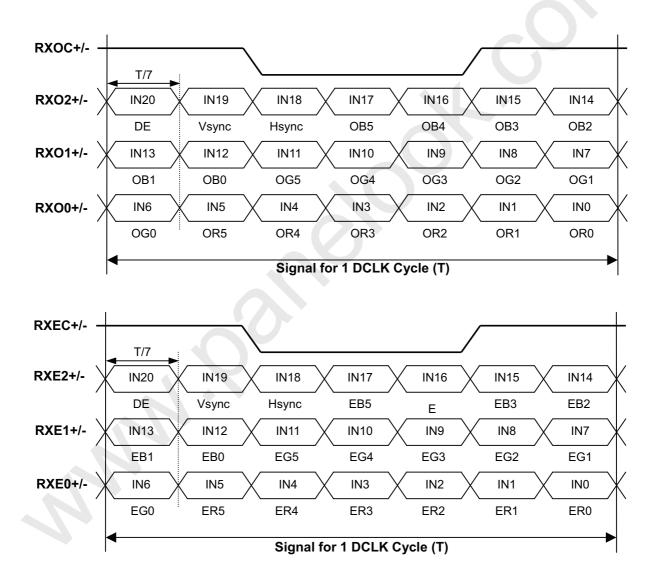
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	Black

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL





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5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

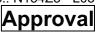
					-			1	[Data		al							
	Color			R						Gre						BI			
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-1	1	1	1
	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:	:	:	:	:			:		:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:			:	:	:	:	:	:
Red	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Gray	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Scale	:	:	:	:	:	:			. : .	:	:		:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:)):	:	:		:	:	:	:	:	:	:
Green	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
	Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Gray	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Scale	:	:		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0
	Blue(63)	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

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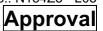
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5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte #	Byte #	Field Name and Comments	Value	Value
(decimal) 0	(hex) 0		(hex) 00	(binary) 00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8		00 0D	000000000
9	9	EISA ID manufacturer name ("CMO")	AF	10101111
10	0A	EISA ID manufacturer name (Compressed ASCII)		01100100
10	0A 0B	ID product code (N154Z3-L03)	64	00010101
12	0D 0C	ID product code (hex LSB first; N154Z3-L03)	15 00	00000000
12	00 0D	ID S/N (fixed "0")	00	00000000
13	0D 0E	ID S/N (fixed "0")		
14	0E 0F	ID S/N (fixed "0")	00	00000000
15 16	10 10	ID S/N (fixed "0")	00	00000000
10	10	Week of manufacture (fixed week code)	12 12	00010010
17	12	Year of manufacture (fixed year code)		00010010
18	12	EDID structure version # ("1")	01	00000001
20	13	EDID revision # ("3")	03	00000011
20	14	Video I/P definition ("digital")	80 21	10000000 00100001
21	16	Max H image size ("33.12 cm")	14	00100001
22	10	Max V image size ("20.7 cm")	78	01111000
23	17	Display Gamma (Gamma = "2.2")		00001010
24	19	Feature support ("Active off, RGB Color")	0A F4	
26	13 1A	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0		01000111
20	1B	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	25 93	11110001
28	1C	Rx=0.577	93 56	10100000 01011011
20	10 1D	Ry=0.339		
30	1D 1E	Gx=0.313	50 8E	01001011 10010110
31	1F	Gy=0.555	0⊑ 29	00100100
31	20	Bx=0.160	29	000100100
33	20	By=0.154	50	01001111
33	21	Wx=0.313		
34	22	Wy=0.329	54	01010100
36	23	Established timings 1	00	00000000
30	24	Established timings 2		00000000
37	25 26	Manufacturer's reserved timings	00	000000000000000000000000000000000000000
30		Standard timing ID # 1	01	
	27	Standard timing ID # 1	01	00000001
40 41	28 29	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

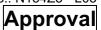




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Byte #	Byte #		Value	Value
(decimal)	(hex)	Field Name and Comments	(hex)	(binary)
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34		01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Standard timing ID # 8 Detailed timing description # 1 Pixel clock ("119MHz", According to	UT	0000001
54	30	VESA CVT Rev1.1)	7C	01111100
55	37	# 1 Pixel clock (hex LSB first)	2E	00101110
56	38	# 1 H active ("1680")	90	10010000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank ("1680 : 160")	60	01100000
59	3B	# 1 V active ("1050")	1A	00011010
60	3C	# 1 V blank ("30")	1E	00011110
61	3D	# 1 V active : V blank ("1050 : 30")	40	01000000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 6")	36	00110110
65		# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 6")	00	00000000
66	42	# 1 H image size ("331.2 mm")	4B	01001011
67	43	# 1 V image size ("207.0 mm")	CF	11001111
68		# 1 H image size : V image size ("331.2 : 207")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71		# 1 Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives	18	00011000
72	48	Detailed timing description # 2	00	00000000
73	49	# 2 Flag	00	00000000
74		# 2 Reserved	00	00000000
75	4B	# 2 FE (hex) defines ASCII string (Model Name "N154Z3-L03", ASCII)	FE	11111110
76	4C	# 2 Flag	00	00000000
77	4D	# 2 1st character of name ("N")	4E	01001110
78	4E	# 2 2nd character of name ("1")	31	00110001
79	4F	# 2 3rd character of name ("5")	35	00110101
80	50	# 2 4th character of name ("4")	34	00110100
81	51	# 2 5th character of name ("Z")	5A	01011010
82	52	# 2 6th character of name ("3")	33	00110011
83		# 2 7th character of name ("-")	2D	00101101
84	54		4C	01001100
-		# 2 8th character of name ("L")		01001100





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Byte #	Byte #	Field Name and Comments	Value	Value
(decimal) 85	(hex) 55		(hex)	(binary)
86	56	# 2 9th character of name ("0")	30	00110000
87		# 2 9th character of name ("3")	33	00110011
		# 2 New line character indicates end of ASCII string	0A	00001010
88	58	# 2 Padding with "Blank" character	20	00100000
89	59	# 2 Padding with "Blank" character	20	00100000
90	5A	Detailed timing description # 3	00	00000000
91		# 3 Flag	00	00000000
92		# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Vendor "CMO", ASCII)	FE	11111110
94	5E	# 3 Flag	00	0000000
95	5F	# 3 1st character of string ("C")	43	01000011
96	60	# 3 2nd character of string ("M")	4D	01001101
97	61	# 3 3rd character of string ("O")	4F	01001111
98	62	# 3 New line character indicates end of ASCII string	0A	00001010
99	63	# 3 Padding with "Blank" character	20	00100000
100	64	# 3 Padding with "Blank" character	20	00100000
101	65	# 3 Padding with "Blank" character	20	00100000
102		# 3 Padding with "Blank" character	20	00100000
103		# 3 Padding with "Blank" character	20	00100000
104		# 3 Padding with "Blank" character	20	00100000
105	69	# 3 Padding with "Blank" character	20	00100000
106	6A	# 3 Padding with "Blank" character	20	00100000
107	6B	# 3 Padding with "Blank" character	20	00100000
108	6C	Detailed timing description # 4	00	00000000
109	6D	# 4 Flag	00	00000000
110	6E	# 4 Reserved	00	00000000
111	6F	# 4 FE (hex) defines ASCII string (Model Name"N154Z3-L03", ASCII)	FE	11111110
112	70	# 4 Flag	00	00000000
113	71	# 4 1st character of name ("N")	4E	01001110
114	72	# 4 2nd character of name ("1")	31	00110001
115	73	# 4 3rd character of name ("5")	35	00110101
116	74	# 4 4th character of name ("4")	34	00110100
117	75	# 4 5th character of name ("Z")	5A	01011010
118	76	# 4 6th character of name ("3")	33	00110011
119	77	# 4 7th character of name ("-")	2D	00101101
120	78	# 4 8th character of name ("L")	4C	01001100
121	79	# 4 9th character of name ("0")	30	00110000
122	7A	# 4 9th character of name ("3")	33	00110011
123	7B	# 4 New line character indicates end of ASCII string	0A	00001010
124	7C	# 4 Padding with "Blank" character	20	00100000
125	7D	# 4 Padding with "Blank" character	20	00100000
126	7E	Extension flag	00	00000000
120	7F		DB	10111100
121		Checksum		10111100

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6. INTERFACE TIMING

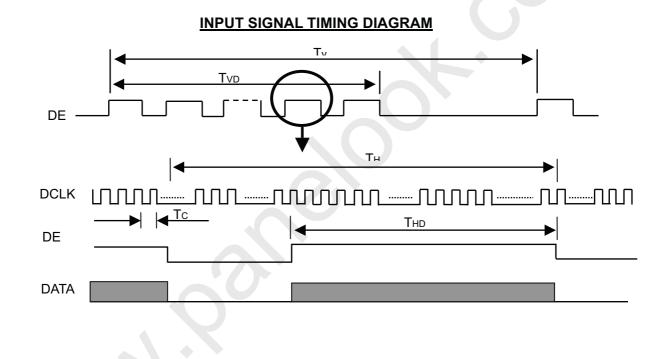
6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
DCLK	Frequency	1/Tc	53.6	59.6	62.6	MHz	(2)
	Vertical Total Time	TV	1057	1080	1090	TH	-
	Vertical Active Display Period	TVD	1050	1050	1050	TH	-
DE	Vertical Active Blanking Period	TVB	TV-TVD	30	TV-TVD	TH	-
DE	Horizontal Total Time	TH	890	920	1010	Tc	(2)
	Horizontal Active Display Period	THD	840	840	840	Тс	(2)
	Horizontal Active Blanking Period	THB	TH-THD	80	TH-THD	Тс	(2)

Note (1) Because of this module is operated by DE only mode, Hsync and Vsync are ignored.

(2) 2 channels LVDS input.

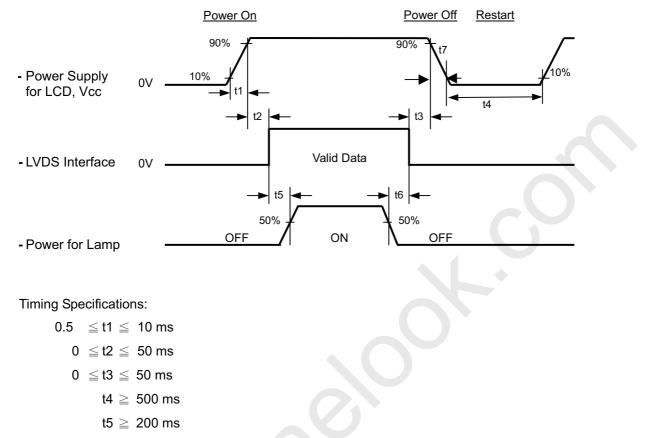






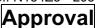


6.2 POWER ON/OFF SEQUENCE



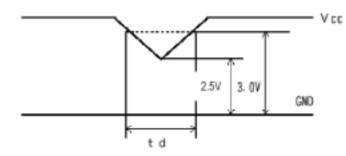
- $t6 \ge 200 \text{ ms}$
- Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.
- Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.
- Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.
- Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow 1ms<t7<10 ms.





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6.3 Momentary Voltage Drops

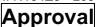


- (1) When 2.5V \leq Vcc $<\!3.0V$ and td $\leq\!10ms$, the unit must work normally when VCC return to 3.0V.
- (2) When Vcc < 2.5V, momentary voltage shall conform to the input voltage sequence.

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7. OPTICAL CHARACTERISTICS

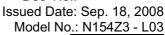
7. 1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Та	25±2	О°
Ambient Humidity	На	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical v	alue in "3. ELECTRICAL	CHARACTERISTICS"
Inverter Current	ΙL	6.0	mA
Inverter Driving Frequency	FL	61	KHz
Inverter		Sumida H05-4915	

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

7.2 OPTICAL SPECIFICATIONS

Iten	n	Symbol	Condition	Min.	Тур.	Max.	Unit	Note
Contrast Ratio		CR		350	500		-	(2), (5)
Deenenee Time		T _R		ł	2	5	ms	(2)
Response Time		Τ _F			6	11	ms	(3)
Average Lumina	ance of White	L _{AVE}		170	200		cd/m ²	(4), (5)
	Red	Rx	θ _x =0°, θ _Y =0°		0.577			
	Reu	Ry	Viewing Normal		0.339			
	Green	Gx	Angle		0.313			
Color	Green	Gy	, anglo	TYP	0.555	TYP		(1)
Chromaticity	Blue	Bx		-0.03	0.160	+0.03		(1)
	Diue	Ву			0.154			
	White	Wx			0.313			
	VVIIILE	Wy			0.329			
White Variation	n of 5 Points	δW_{5p}	θ _x =0°, θ _Y =0°	80			%	(5),(6)
	Horizontal	θ _x +		70	80			
	Horizoniai	θ _x -	CD>10	70	80		Deg	(1) (5)
Viewing Angle	Vertical	θ_{Y} +	CR≥10	60	70		Deg.	(1), (5)
	vertical	θ _Y -		60	70			

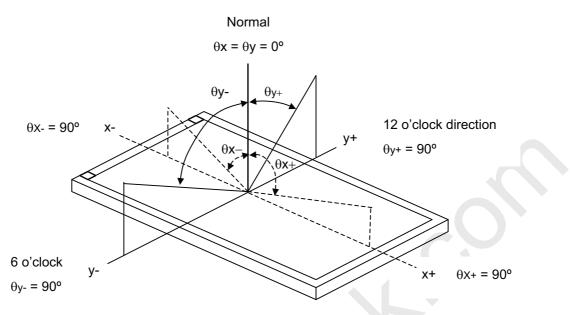


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Note (1) Definition of Viewing Angle (θx , θy):

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Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

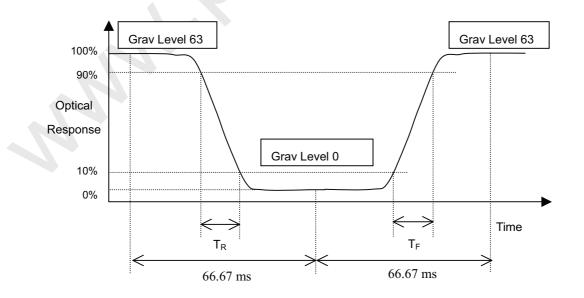
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time (T_R, T_F) :



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Note (4) Definition of Average Luminance of White (LAVE):

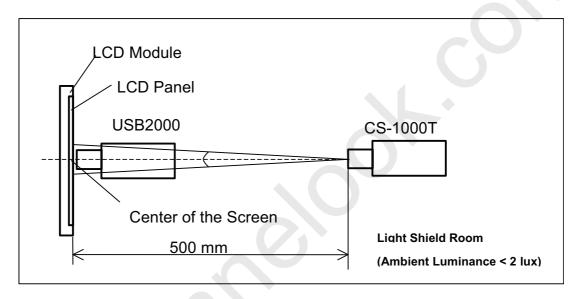
Measure the luminance of gray level 63 at 5 points

 $L_{AVE} = [L (1) + L (2) + L (3) + L (4) + L (5)] / 5$

L (x) is corresponding to the luminance of the point X at Figure in Note (6)

Note (5) Measurement Setup:

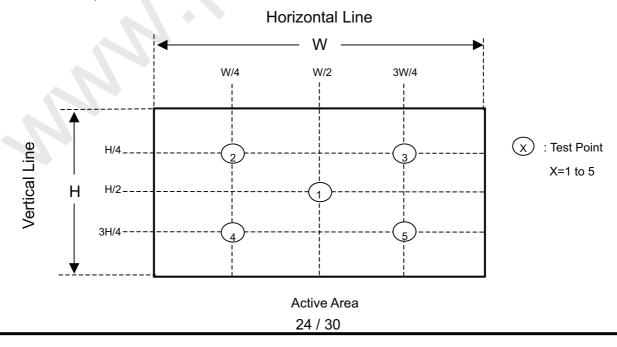
The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



Note (6) Definition of White Variation (δ W):

Measure the luminance of gray level 63 at 5 points

```
\delta W_{5p} = Minimum [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / Maximum [L (1)+ L (2)+ L (3)+ L (4)+ L (5)]
```







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8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.
- (4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- (5) Do not pull the I/F connector in or out while the module is operating.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.
- (9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (10) When ambient temperature is lower than 10°C may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

8.2 SAFETY PRECAUTIONS

- (1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

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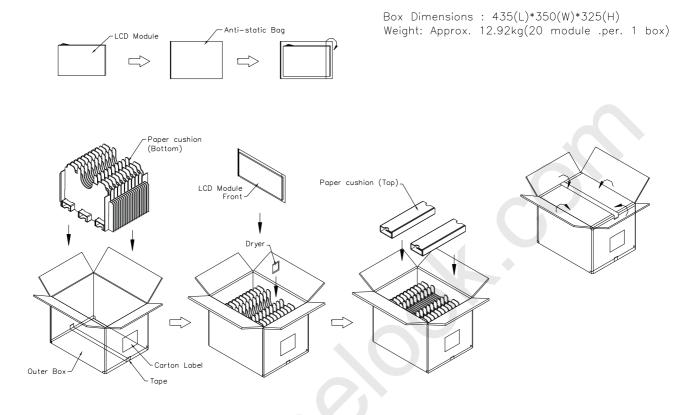
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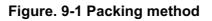
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9.1 CARTON





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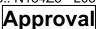
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9.2 PALLET

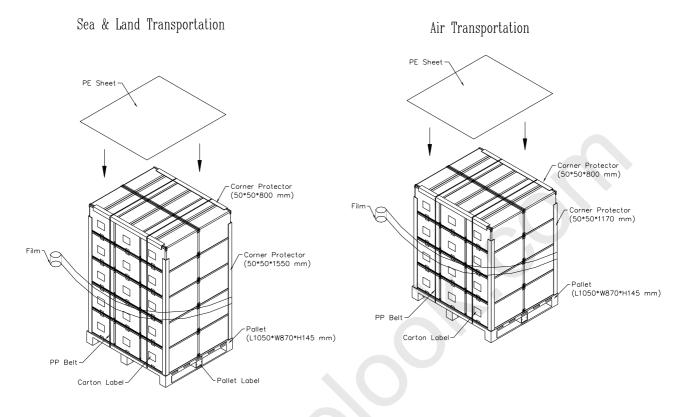


Figure. 9-2 Packing method

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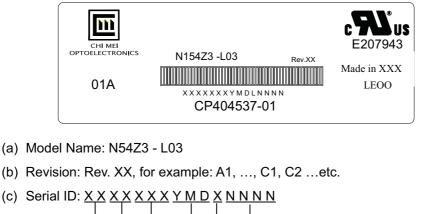


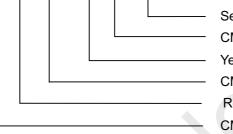
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10. DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.





Serial No. CMO Internal Use Year, Month, Date CMO Internal Use Revision CMO Internal Use

Serial ID includes the information as below:

(a) Manufactured Date: Year: 1~9, for 2001~2009

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U

- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

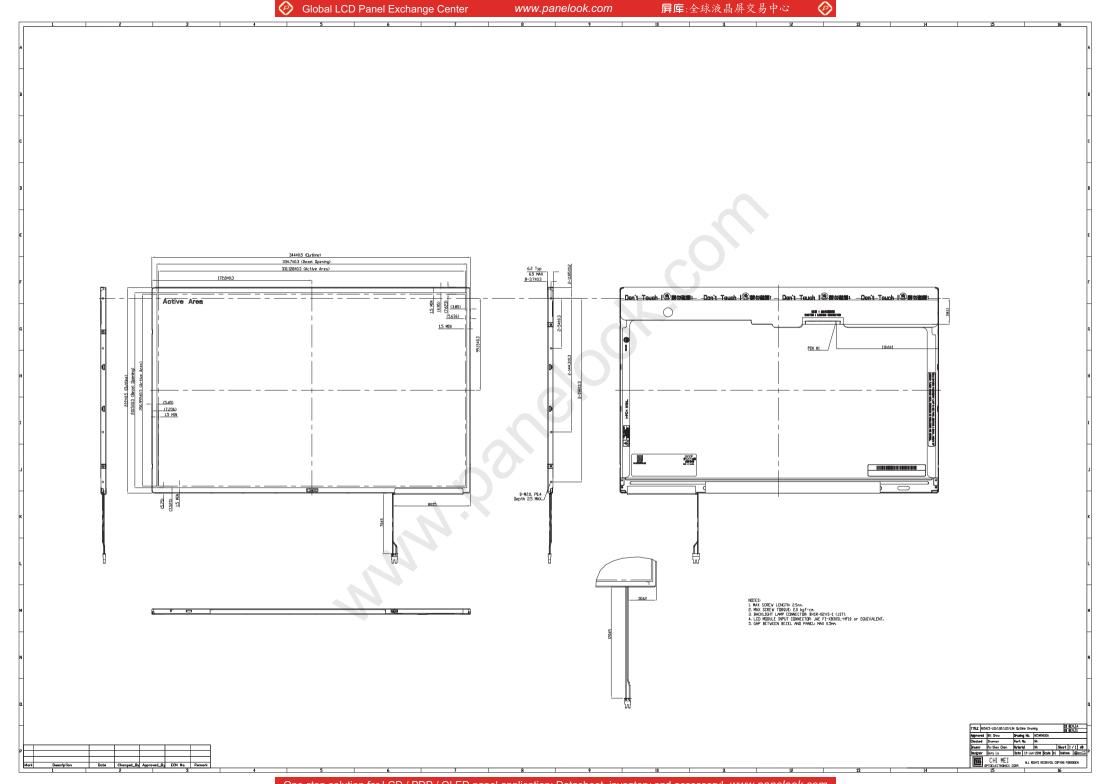


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10.2 CARTON LABEL

PO.NO.				-
Part ID	CP404537-01	01A	dinin.	
Model No	ame	AT L		-
Carton ID	۱ <u> </u>		Quantities	s



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