MAXLINEAR

MXL241SF
CABLE INTEGRATED RECEIVER

General Description

The MxL241SF is a single-chip integrated tuner and demodulator receiver IC targeting all global digital cable standards (ITU-T J.83 Annex A [DVB-C], Annex B [US Cable] and Annex C). The MxL241SF can also receive and demodulate OOB FDC signals without FEC processing. The interface complies with the open cable - cable card interface specification (OC-SP-CCIF2.0).
The MxL241SF is compliant to all SCTE40 requirements and all SCTE55-1 requirements in OOB mode.
Broadband input filter, channel filter, automatic gain control, LO generation, PLL and demodulation functions are integrated on the chip, simplifying board-level design and faster design cycle. High integration along with a small device footprint enables a very compact design, reduced bill-of-materials cost, and low power consumption.
In J.83 mode, The MxL241SF takes an RF input signal from 44 to 1002MHz and outputs MPEG transport. In OOB mode, the MxL241SF takes an RF of 70 to 130MHz and converts it to CRX and DRX. All functions are controlled by I2C interface. The IC can operate with a single 3.3V supply or with both 3.3V and 1.8V supplies for lower power consumption. The MxL241SF is available in a 6 x 6 mm^2 40-pin QFN package.

Applications

High-performance receivers for digital cable applications such as:

- STBs
- EMTAs
- Cable modems
- Cable DTAs
- Cable Gateways

Features

- Wide tuning range from 44 to 1002 MHz
- OOB tuning range of 70 to 130MHz
- Single RF input pin for all bands
- Integrated channel filtering requiring no external SAW filters
- Programmable channel bandwidths of 6 or 8MHz
- Loopthrough output function
- On-chip voltage regulators enable single supply 3.0V-3.6V operation
- Low-power consumption of < 500mW when both 3.3V and 1.8V power supplies are used
- Automatic QAM type detector
- High accuracy input power reporting
- Fast locking time
- Reference clock output is available for re-use by demodulators and additional tuners in multi-channel applications
- Serial or parallel MPEG output

Standards Supported

MxL241SF is compliant to the following standards:

- ITU-T J.83
  - Annex A (DVB-C),
  - Annex B (US Cable),
  - Annex C
- DOCSIS
- EURODOCSIS

Pin Configuration

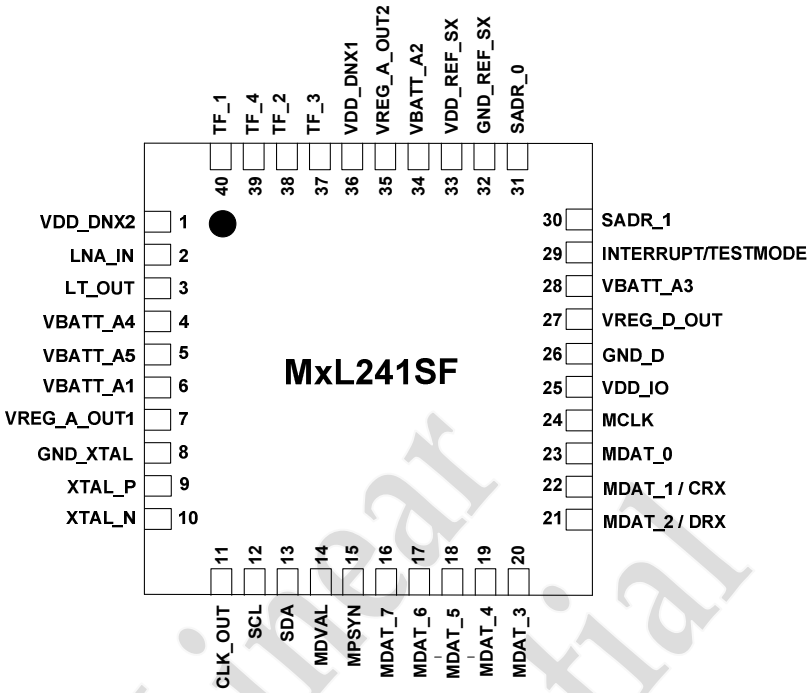


Figure 1: MxL241SF Pin Configuration

IC Block Diagram

The architecture of MxL241SF integrated receiver is illustrated in the functional block diagram of Figure 2. The device incorporates a fully-integrated tuner and demodulator. On-chip regulators regulate the battery voltage to the internal supplies of 1.6 and 1.2V. The MPEG output provides demodulated TS (Transport Stream) in serial or parallel format.

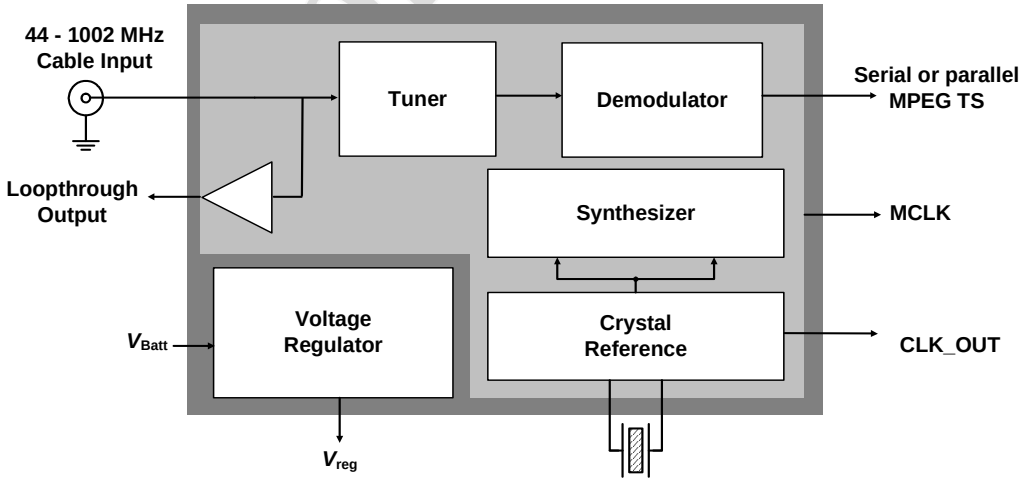


Figure 2: MxL241SF Simplified Block Diagram

Pin Description

Pin #	Pin Name		Pin #	Pin Name
1	VDD_DNX2		21	MDAT_2 / DRX
2	LNA_IN		22	MDAT_1 / CRX
3	LT_OUT		23	MDAT_0
4	VBATT_A4		24	MCLK
5	VBATT_A5		25	VDD_IO
6	VBATT_A1		26	GND_D
7	VREG_A_OUT1		27	VREG_D_OUT
8	GND_XTAL		28	VBATT_A3
9	XTAL_P		29	INTERRUPT/TESTMODE
10	XTAL_N		30	SADR_1
11	CLK_OUT		31	SADR_0
12	SCL		32	GND_REF_SX
13	SDA		33	VDD_REF_SX
14	MDVAL		34	VBATT_A2
15	MPSYN		35	VREG_A_OUT2
16	MDAT_7		36	VDD_DNX1
17	MDAT_6		37	TF_3
18	MDAT_5		38	TF_2
19	MDAT_4		39	TF_4
20	MDAT_3		40	TF_1

Table 1: Pin name list of MxL241SF

RF Interface

Pin Name	Direction	Description
LNA_IN	Input	Single-ended RF input with 75 Ω input impedance
LT_OUT	Output	Loopthrough output with open drain
TF_1-4	Input-Output	Pins used for input broadband filtering

Table 2: Description of RF interface

I²C Interface

This chip can be controlled through I²C compatible interface.

Pin Name	Direction	Description
SCL	Input	Clock
SDA	Bi-directional	Open drain data pin
SADR_0, 1	Input	Address select pin

Table 3: Description of I2C Interface

Supply and Ground

This chip contains on-chip regulators that regulate the battery voltage to lower voltages for on-chip operation.

Pin Name	Direction	Description
VDD_NAME	Input	Supply voltage for on-chip circuits
GND_NAME	Input	Ground for on-chip circuit blocks
VBATT_A1, A2	Input	Supply voltage input for on-chip analog regulator
VBATT_A3	Input	Supply voltage input for on-chip digital regulator
VREG_A_OUT1, 2	Output	On-chip analog regulator output
VREG_D_OUT	Output	On-chip digital regulator output
VDD_IO	Input	Supply voltage input for I/O interface
VBATT_A4, A5	Input	Supply voltage input for on-chip blocks

Table 4: Description of supply and ground pins

Analog and Digital I/O

Pin Name	Direction	Description
INTERRUPT/ TESTMODE	Output	Interrupt signal output / Testmode is reserved for MaxLinear internal use only.
XTAL_N	Input	Crystal negative input
XTAL_P	Input	Crystal positive input. It can be used as an external system clock input pin if no crystal is used
CLK_OUT	Output	Crystal clock output for clock re-use
MDVAL	Output	MPEG data valid
MPSYN	Output	MPEG frame sync
MDAT_0 - 2 MDAT_4 - 7	Output	MPEG parallel output. MDAT_0 is used for serial mode. In OOB mode MDAT_1 is CRX and MDAT_2 is DRX
MDAT_3	Bi-dir	MPEG parallel output. GPI when MPEG is set to serial output format
MCLK	Bi-dir	MPEG clock

Table 5: Description of I/O interface

Specifications

Absolute Maximum Ratings

Parameter	Min	Max	Units
VBATT_A1, A2, A3, A4, A5	0	3.6	V
VDD_NAME	0	3.6	V
LT_OUT	0	3.6	V
SDA, SCL	0	3.6	V
INTERRUPT/TESTMODE	0	3.6	V
RF Input Power		10	dBm
Storage Temp	-65	150	°C
Junction Temp		150	°C
Soldering Temp		260	°C

Table 6: Absolute Maximum Ratings

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device above these, or any other conditions beyond those "recommended" is not implied. Exposure to conditions above those "recommended" for extended periods of time may affect device reliability.

Required Operating Conditions

Parameter		Symbol	Min	Typical	Max	Units
Analog Supply		VDD_DNX2, VDD_REF_SX, VDD_DNX1	1.5	1.6	1.65	V
Battery Supply		VBATT_A4, A5	3.0	3.3	3.6	V
Battery Supply	Dual Voltage Supply	VBATT_A1, A2, A3	1.7	1.8	2	V
	Single Voltage Supply	VBATT_A1, A2, A3	3.0	3.3	3.6	V
I/O Supply		VDD_IO	1.7	3.3	3.6	V
Operating Temperature		T	0	25	70	°C

Table 7: Operating Conditions

Digital IO Specifications

Parameter	Symbol	Min	Typical	Max	Units
Output Logic Voltage SDA	VOH	0.8 x VDD_IO			V
	VOL			0.2 x VDD_IO	V
Output Logic Voltage all other pins	VOH	0.8 x VDD_IO			V
	VOL			0.2 x VDD_IO	V
Input Logic Voltage	VIH	0.7 x VDD_IO			V
	VIL			0.3 x VDD_IO	V

Table 8: Digital IO Operating Condition

*Note: VOH/VOL is 2mA source/sink for VDD_IO 3-3.6V. VOH/VOL is 1mA source/sink for VDD_IO 1.7-1.9V

Integrated Receiver Specifications

All specifications apply to using on-chip analog regulators with conditions defined in Table 7.

Parameter		Symbol	Min	Typical	Max	Units
System						
Input Return Loss (75 Ω)		S_{11}		8		dB
RF frequency range		f_{RF}	44		1002	MHz
Channel bandwidth				6, 8		MHz
Supply (VBATT_A1, A2, A3, A4, A5) Ripple Susceptibility (1KHz – 500KHz)					15	mVpp
Loop through						
Gain		G_{LT}	-3.5	0	3.5	dB
Noise Figure (LT Only)		NF_{LT}		7.5	10	dB
Crystal Oscillator						
Negative Resistance				250		Ω
Input level to XTAL_P pin when using external clock			400	800	1200	mVpp
Others						
Input power Reporting	Absolute Accuracy		-3		+3	dB
	Relative Accuracy with 1dB step		-0.5		+0.5	dB
Clock Output Swing *	24MHz crystal		500	750	900	mVpp
	48MHz crystal		300	500	750	mVpp

Table 9: Receiver Specifications

*Note: Clock output swing is specified with 10pF load capacitance and CLKOUT_GAIN set to 10. Specific program information is described in the programming guide.

OOB Mode Receiver Specifications

All specifications apply to using on-chip analog regulators with conditions defined in Table 7. The specifications of the MxL241SF are shown in Table 10. All the applicable specifications shown in Table 9 also apply to OOB mode.

Parameter		Symbol	Min	Typical	Max	Units
RF frequency range		f_{RF}	70		130	MHz
Frequency offset	Symbol rate = 0.772MHz		-90		90	kHz
	Symbol rate = 1.024MHz		-115		115	
	Symbol rate = 1.544MHz		-125		125	

Table 10: OOB Mode Receiver Specifications

Current Consumption

The current consumption accounts for temperature and process variations. Typical condition applies to using on-chip regulators with typical conditions defined in Recommended Operation Conditions.

Mode	Condition	RF (MHz)	Supply Pin	Min	Typ	Max	Units
Active	Loopthrough off	50 - 300	VBATT_A1+A2 +A3		217		mA
			VBATT_A4 + A5		35		mA
		300 – 1002	VBATT_A1+A2+ A3		203		mA
			VBATT_A4 + A5		35		mA
Standby	Loopthrough off	50 – 1002	VBATT_A1+A2+ A3		26		mA
			VBATT_A4 + A5		0		mA

Table 11: Current Consumption

Crystal Requirements

MxL241SF supports only fundamental mode crystals frequencies listed in Table 12. A 48MHz crystal is chosen as the default due to phase noise performance.

Crystal Frequencies	Units	Comments
48	MHz	Supported default
24, 25	MHz	Optional crystal frequencies

Table 12: Supported Crystal Frequencies

Parameter	Min	Typical	Max	Units
ESR		50	100	Ω
Frequency Accuracy (includes temperature and tolerance)		±30	±50	ppm
Aging (1st year)		±5		ppm/year
Load Capacitance		10		pF
Drive Level			500	µW

Table 13: Crystal Requirements

The crystal loading capacitors are implemented on-chip and provide a programmable range of 1-25pF in 1pF steps. Table 14 lists specifications of the crystal oscillator.

Parameter	Min	Typical	Max	Units
Negative Resistance (with typical 48MHz SMD crystal)		250		Ohm
On-chip loading capacitors	2	10 (default)	25	pF
Drive level			500	uWatt

Table 14: Crystal Oscillator Specifications

ESD Performance

All pins pass the ESD performance of 2000V using the Human Body Model (HBM), and of 500V using the Charged Device Model (CDM).

Supply Voltage Ramp-Up Rules

The supply voltage ramp-up timing rules are described below. Violating the rules can cause reset failure to the MxL241SF IC:

a) Ramp-up time constraints of all supply voltages (90% of VBATT_A1, VBATT_A2, VBATT_A3, VBATT_A4, VBATT_A5 and VDD_IO) shall be 100us < t < 10ms

b) The ramp-up sequence between any voltage supplies (VBATT_A1, VBATT_A2, VBATT_A3, VBATT_A4, VBATT_A5 and VDD_IO) is arbitrary

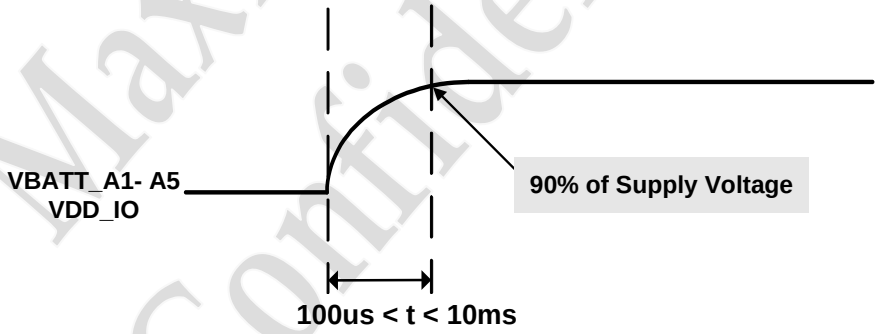


Figure 3: Supply voltage ramp-up timing rules

Timing Specifications

MPEG TS parallel output interface

The waveform for the MPEG TS parallel output interface is shown in Figure 4. This interface has the following features:

- Support all MPEG data rates for J.83
- Maximum MPEG clock frequency is 57 MHz
- The MPEG clock polarity can be inverted.
- The polarity of the MPEG valid and MPEG sync signals can be controlled.

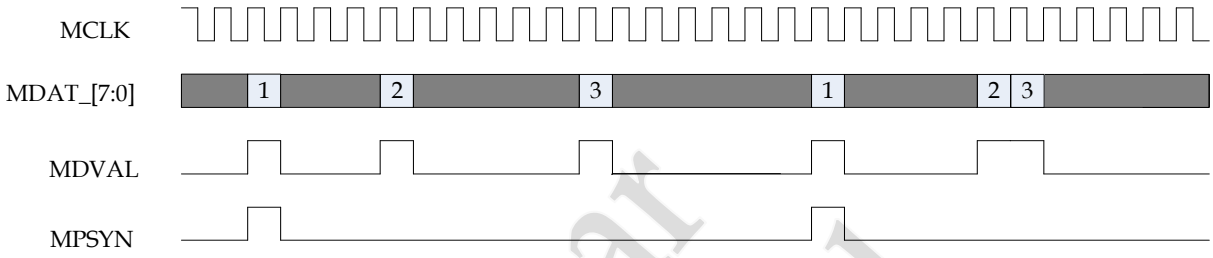


Figure 4: MPEG-2 TS parallel output interface waveform

MPEG TS serial output interface

The waveform for the MPEG TS serial output interface is shown in Figure 5. This interface has the following features:

- All MPEG data rates for J.83 are supported
- Maximum MPEG clock frequency is 57 MHz
- Endian-ness programmable Most-Significant Bit or Least Significant Bit first input
- The polarity of the MPEG valid and MPEG sync signal can be controlled by programming registers

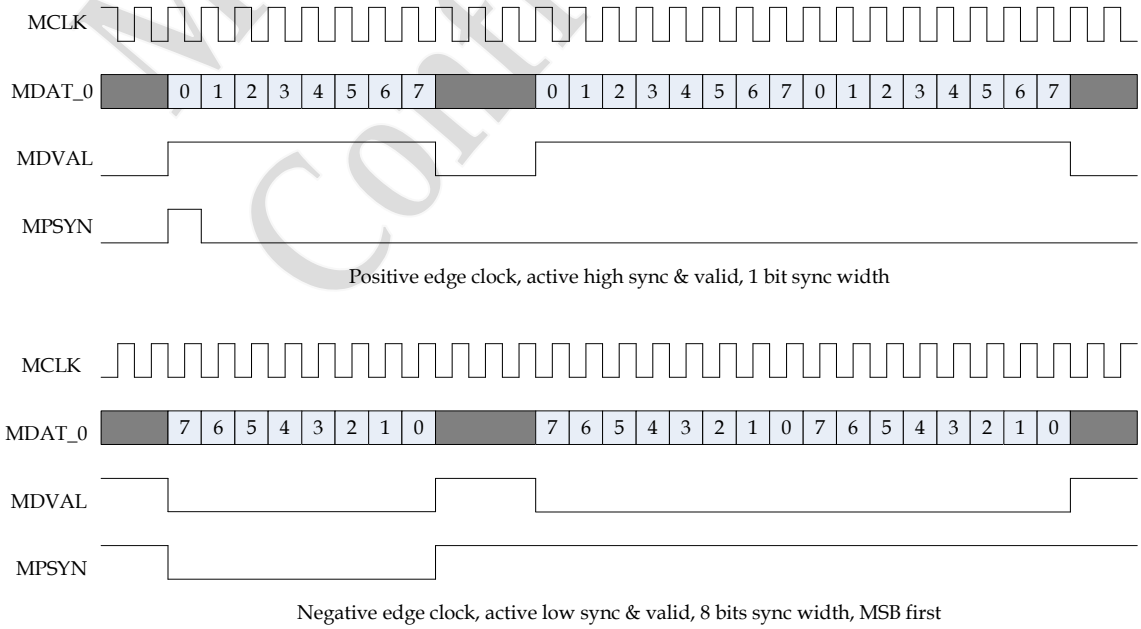


Figure 5: MxL241SF MPEG2 serial output waveforms

MPEG TS output and I2C input timing spec

Timing diagrams for the MPEG TS output and I2C input timing spec are shown in Figure 6 to Figure 9. The corresponding specifications are shown in Table 15.

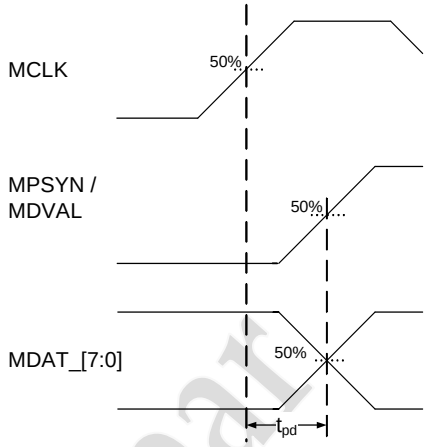


Figure 6: MPEG parallel output timing

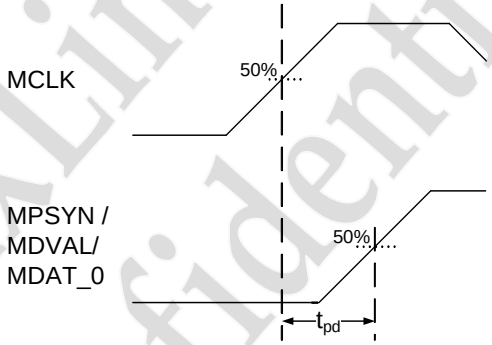


Figure 7: MPEG serial output timing

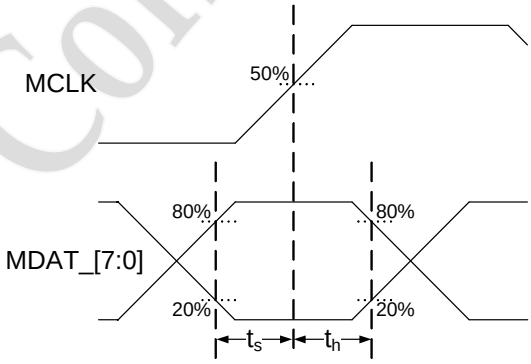


Figure 8: Output Set-up and Hold Time

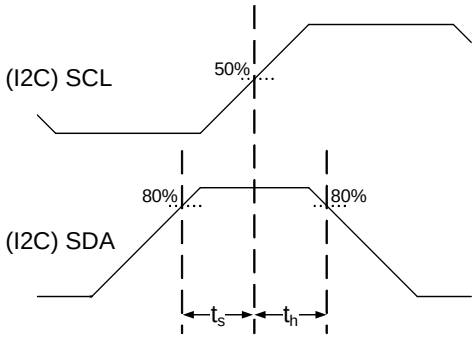


Figure 9: I2C input timing diagram

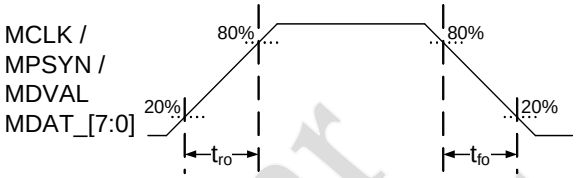


Figure 10: Output rise and fall time

Parameter	Symbol	Min	Typical	Max	Units
MPEG output					
MPEG clock duty cycle [1]		45	50	55	%
MPEG clock frequency [1]		3.5625		57	MHz
Master Propagation delay [1] (Figure 7)	t_{pd}	7.6		10.2	ns
Slave Propagation delay [1] (Figure 7)	t_{pd}	4.6		12.8	ns
Rise time [1,2] (Figure 10)	t_{ro}	0.8		2	ns
Fall time [1,2] (Figure 10)	t_{fo}	0.9		1.8	ns
Master set-up time [1] (Figure 8)	T_s	7.3		9.9	ns
Slave set-up time [1] (Figure 8)	T_s	4.7		12.9	ns
Master hold time [1] (Figure 8)	T_h	7.6		10.2	ns
Slave hold time [1] (Figure 8)	T_h	4.6		12.8	ns

1. Measurements for VDD_IO = 3.3V and drive strength =2x
2. Capacitive load = 10pf

Table 15: Timing specifications

OOB (Out-of-Band) Interface

The interface complies with open cable - cable card interface specification (OC-SP-CCIF2.0). MDAT_1 and MDAT_2 signals are used to transfer the data. MDAT_1 and MDAT_2 are CRX and DRX equivalent signals defined in OC-SP-CCIF2.0 document. In this interface the actual received symbols are transferred without FEC processing. Table 16 specifies the MDAT_1 and MDAT_2 signals parameters:

Parameter	Signal	Unit	Min	Typ	Max	Condition
Frequency	MDAT_2	KHz			3088	
Clock High Time (t_H)		nsec	129			Notes 1,2,3
Clock Low Time (tL)		nsec	129			Notes 1,2,3

Set-up (t_u)	MDAT_2	nsec	10			From time signal reachs 90% of high level (rising) or 10% of high (falling) until MDAT_1 mid-point transition
Hold (t_h)	MDAT_2	nsec	5			From MDAT_1 mid-point transition until signal reaches 10% of high level(rising) or 90% of high level (falling)

Table 16: OOB Frequency and Timing Specifications

Notes:
1. Refer to Figure 11 MDAT_1 and MDAT_2 Timing Diagram in OOB mode.
2. AC timing is measured with timing reference level at 1.5V.
3. Minimum value derived assuming a duty cycle of 60/40.

Timing characteristics of MDAT_1 and MDAT_2 during OOB demodulation are depicted in Table 16, Figure 11 and Figure 12.

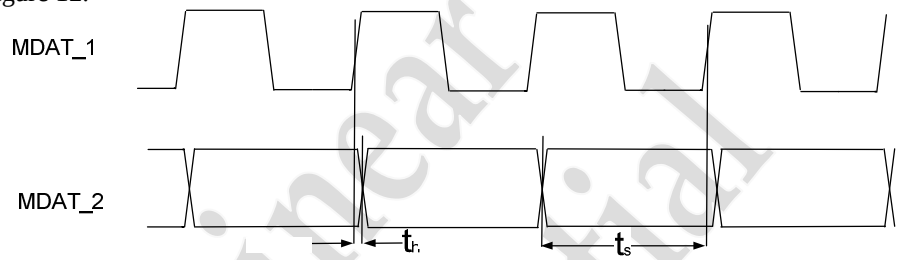


Figure 11: Output Timing Diagram in OOB Demodulation

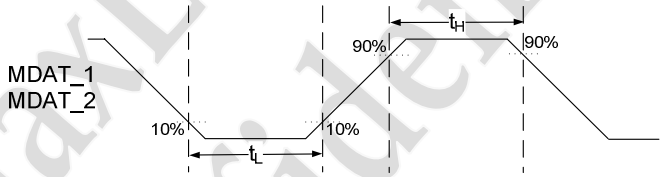


Figure 12: Output High and Low Time in OOB Demodulation

Ordering Information

Part Number	Package Type	Description
MxL241SF	QFN40	40-Pin QFN with no leads. Body size 6 x 6 x 0.85mm. Exposed backside paddle.

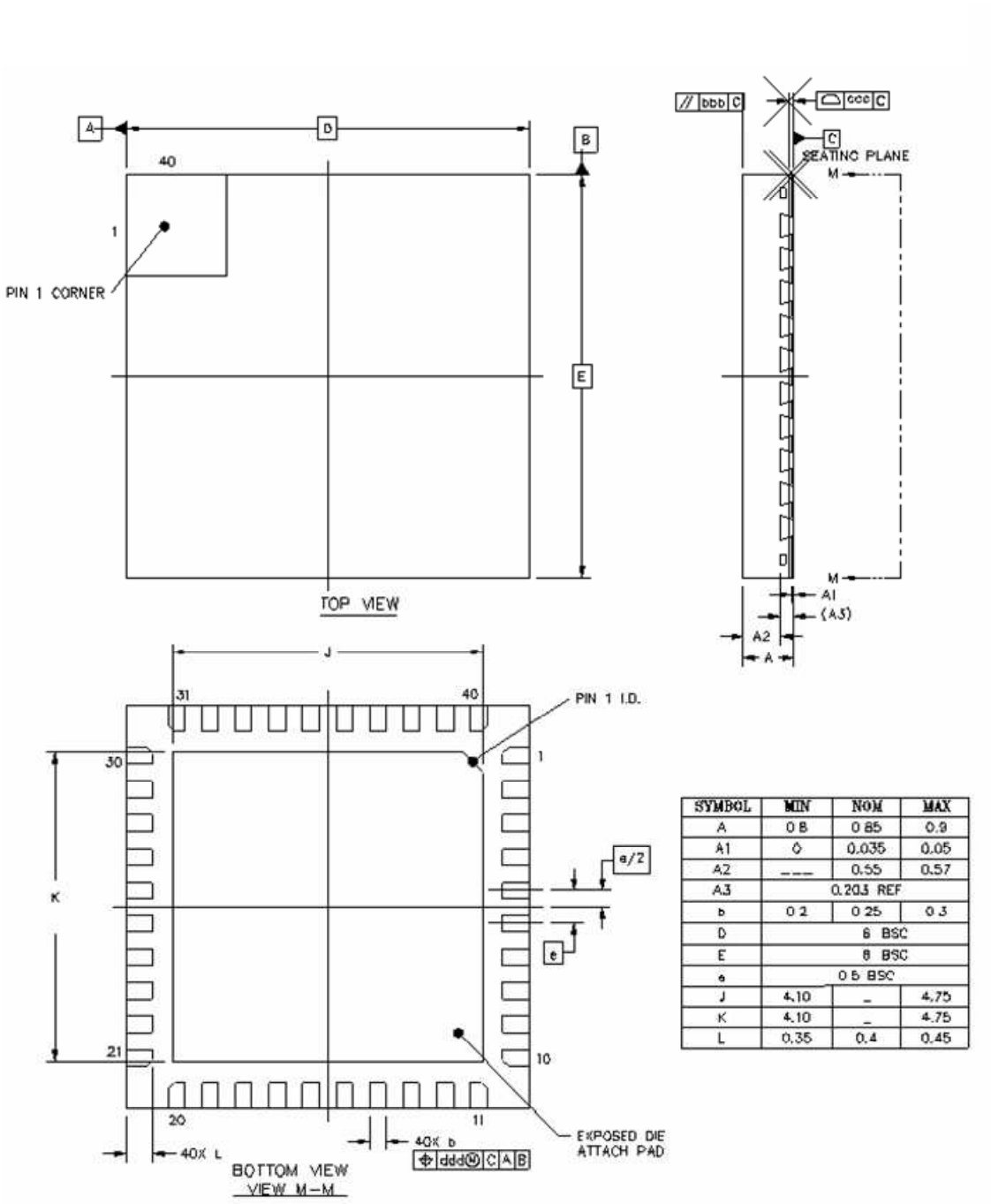
Table 17: Ordering Information

Application Circuit

Please contact MaxLinear Applications for more information.

Packaging

QFN40 package dimensions: 6x6x0.85 mm^3



SYMBOL	MIN	NOM	MAX
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	---	0.65	0.67
A3		0.203 REF	
b	0.2	0.25	0.3
D		6 BSC	
E		6 BSC	
e		0.5 BSC	
J	4.10	-	4.75
K	4.10	-	4.75
L	0.35	0.4	0.45

Revision History

Rev 1.0, July 23, 2009

1. First release

Rev 1.0, July 23, 2009

1. Update Table 10: Current Consumption
2. Update Table 8: Digital IO Operating Condition
3. Modify Supply Voltage Ramp-up Rules
4. Update Table 13: Timing Specifications

Rev 2.1, May 27, 2010

1. Added OOB specifications

Rev 2.2, June 21, 2010

1. Updated the limits of all the parameters

Rev 2.3, October 4, 2010

1. Update Table 11: Current Consumption
2. Add ESR and Frequency Accuracy specifications: Table 13: Crystal Requirements
3. Remove 27MHz XTAL support: Table 12: Supported Crystal Frequencies

Rev 2.4, October 11, 2010

1. Update footnote and revision table date to October 11, 2010