MXD86C2

DP12T Switch with MIPI for LTE TRX Application

General Description

The MXD86C2 is a low loss, high isolation DP12T switch for antenna TRX application.

The MXD86C2 is compatible with MIPI control, which is a key requirement for many cellular transceivers. This part is packaged in a compact 2.0mm x 2.4mm, 18-pin, LGA package which allows for a small solution size with no need for external DC blocking capacitors (when no external DC is applied to the device ports).

Features

- Excellent insertion loss
  - 0.50 dB Insertion Loss at 2.7GHz
- P0.1dB @ 35dBm
- Multi-Band operation 400MHz to 3800MHz
- RFFE serial control interface
- Compact 2.0mm x 2.4mm in LGA-18 package
- No DC blocking capacitors required (unless external DC is applied to the RF ports)

Applications

- 3G/4G multimode cellular handsets (UMTS and CDMA2000)
- Carrier aggregation diversity

Functional Block Diagram and Pin Function

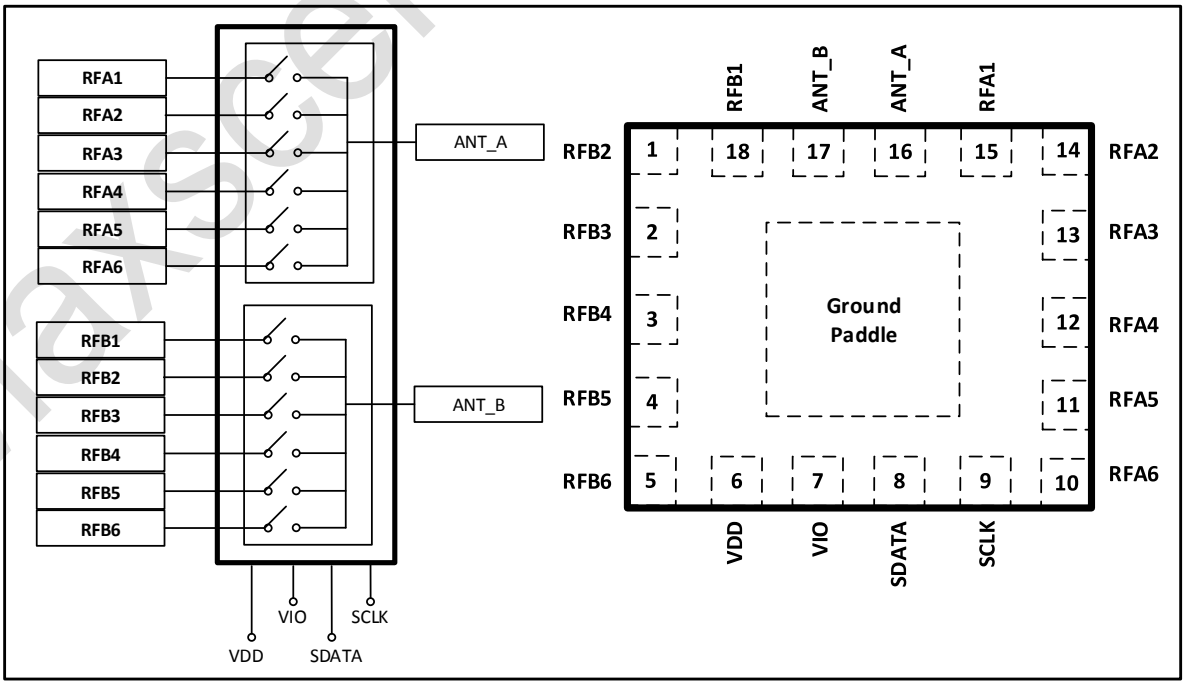


Figure 1 Functional Block Diagram and Pinout (Top View)

Application Circuit

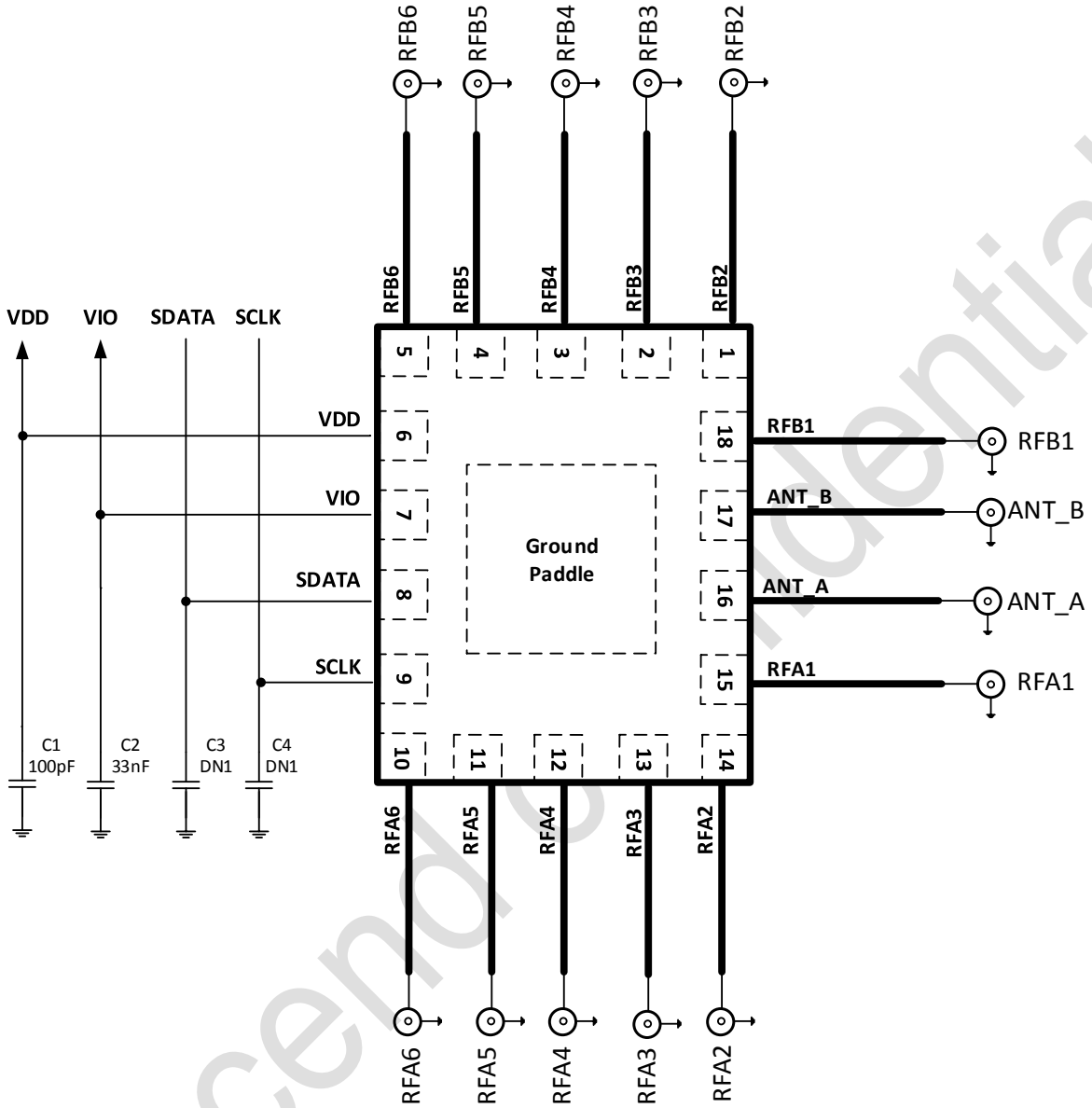


Figure 2 Evaluation Board Schematic

Table 1. Pin Description

Pin No.	Name	Description	Pin No.	Name	Description
1	RFB2	RF port B2	10	RFA6	RF port A6
2	RFB3	RF port B3	11	RFA5	RF port A5
3	RFB4	RF port B4	12	RFA4	RF port A4
4	RFB5	RF port B5	13	RFA3	RF port A3
5	RFB6	RF port B6	14	RFA2	RF port A2
6	VDD	Power supply	15	RFA1	RF port A1
7	VIO	Supply voltage for MIPI	16	ANT_A	Antenna port A
8	SDATA	MIPI data input/output	17	ANT_B	Antenna port B
9	SCLK	MIPI clock	18	RFB1	RF port B1
Ground Paddle	GND	Ground			

Note: Bottom ground paddles must be connected to ground.

Truth Table

Table 2. Register_0 Truth Table (ANT_B)

State	Mode	Register_0							
		D7	D6	D5	D4	D3	D2	D1	D0
1	ISO	x	x	x	0	0	0	0	0
2	RFB1	x	x	x	0	0	0	0	1
3	RFB2	x	x	x	0	0	0	1	0
4	RFB3	x	x	x	0	0	0	1	1
5	RFB4	x	x	x	0	0	1	0	0
6	RFB5	x	x	x	0	0	1	0	1
7	RFB6	x	x	x	0	0	1	1	0
8	RFB6+RFB5	x	x	x	0	0	1	1	1
9	RFB6+RFB4	x	x	x	0	1	0	0	0
10	RFB6+RFB3	x	x	x	0	1	0	0	1
11	RFB6+RFB2	x	x	x	0	1	0	1	0
12	RFB6+RFB1	x	x	x	0	1	0	1	1
13	RFB5+RFB4	x	x	x	0	1	1	0	0
14	RFB5+RFB3	x	x	x	0	1	1	0	1
15	RFB5+RFB2	x	x	x	0	1	1	1	0
16	RFB5+RFB1	x	x	x	0	1	1	1	1
17	RFB4+RFB3	x	x	x	1	0	0	0	0
18	RFB4+RFB2	x	x	x	1	0	0	0	1
19	RFB4+RFB1	x	x	x	1	0	0	1	0
20	RFB3+RFB2	x	x	x	1	0	0	1	1
21	RFB3+RFB1	x	x	x	1	0	1	0	0
22	RFB2+RFB1	x	x	x	1	0	1	0	1
23	ISO	x	x	x	1	0	1	1	0
24	ISO	x	x	x	1	0	1	1	1
25	ISO	x	x	x	1	1	0	0	0
26	ISO	x	x	x	1	1	0	0	1
27	ISO	x	x	x	1	1	0	1	0
28	ISO	x	x	x	1	1	0	1	1
29	ISO	x	x	x	1	1	1	0	0
30	ISO	x	x	x	1	1	1	0	1
31	ISO	x	x	x	1	1	1	1	0
32	ISO	x	x	x	1	1	1	1	1

Table 3. Register_1 Truth Table (ANT_A)

State	Mode	Register_1							
		D7	D6	D5	D4	D3	D2	D1	D0
1	ISO	x	x	x	0	0	0	0	0
2	RFA1	x	x	x	0	0	0	0	1
3	RFA2	x	x	x	0	0	0	1	0
4	RFA3	x	x	x	0	0	0	1	1
5	RFA4	x	x	x	0	0	1	0	0
6	RFA5	x	x	x	0	0	1	0	1
7	RFA6	x	x	x	0	0	1	1	0
8	RFA6+RFA5	x	x	x	0	0	1	1	1
9	RFA6+RFA4	x	x	x	0	1	0	0	0
10	RFA6+RFA3	x	x	x	0	1	0	0	1
11	RFA6+RFA2	x	x	x	0	1	0	1	0
12	RFA6+RFA1	x	x	x	0	1	0	1	1
13	RFA5+RFA4	x	x	x	0	1	1	0	0
14	RFA5+RFA3	x	x	x	0	1	1	0	1
15	RFA5+RFA2	x	x	x	0	1	1	1	0
16	RFA5+RFA1	x	x	x	0	1	1	1	1
17	RFA4+RFA3	x	x	x	1	0	0	0	0
18	RFA4+RFA2	x	x	x	1	0	0	0	1
19	RFA4+RFA1	x	x	x	1	0	0	1	0
20	RFA3+RFA2	x	x	x	1	0	0	1	1
21	RFA3+RFA1	x	x	x	1	0	1	0	0
22	RFA2+RFA1	x	x	x	1	0	1	0	1
23	ISO	x	x	x	1	0	1	1	0
24	ISO	x	x	x	1	0	1	1	1
25	ISO	x	x	x	1	1	0	0	0
26	ISO	x	x	x	1	1	0	0	1
27	ISO	x	x	x	1	1	0	1	0
28	ISO	x	x	x	1	1	0	1	1

29	**ISO**	x	x	x	1	1	1	0	0
30	**ISO**	x	x	x	1	1	1	0	1
31	**ISO**	x	x	x	1	1	1	1	0
32	**ISO**	x	x	x	1	1	1	1	1

Recommended Operation Range

Table 4. Recommended Operation Condition

Parameters	Symbol	Min	Typ	Max	Units
Operation Frequency	f1	0.4	-	3.8	GHz
Power supply	V_{DD}	2.5	2.8	3.0	V
Power supply for MIPI	V_{IO}	1.65	1.8	1.95	V
MIPI Control Voltage High	V_H	0.8*VIO	1.8	1.95	V
MIPI Control Voltage Low	V_L	0	0	0.3	V

Specifications

Table 5. Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
DC Specifications						
Supply voltage	V_{DD}		2.5	2.8	3.0	V
Supply current	I_{DD}			55	90	uA
V_{IO} supply voltage	V_{IO}		1.65	1.8	1.95	V
V_{IO} Supply current	I_{IO}			4	10	uA
SDATA, SCLK control voltage: High Low	V_{CTL_H} V_{CTL_L}		0.8* V_{IO} 0	V_{IO} 0	1.95 0.3	V V
Switching Speed, one RF to another		10% to 90% RF		1	2	uS
RF Specifications						
Insertion loss (ANT_A pin to RFA1/2/3/4/5/6 pins; ANT_B pin to RFB1/2/3/4/5/6 pins)	IL	0.1 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 2.7 GHz 3.4 to 3.8 GHz		0.40 0.45 0.50 0.70	0.50 0.60 0.65 0.90	dB dB dB dB
Isolation (ANT_A pin to RFA1/2/3/4/5/6 pins; ANT_B pin to RFB1/2/3/4/5/6 pins)	Iso	0.1 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 2.7 GHz 3.4 to 3.8 GHz	30 28 22 18	45 35 28 22		dB dB dB dB
Input return loss (ANT_A pin to RFA1/2/3/4/5/6 pins; ANT_B pin to RFB1/2/3/4/5/6 pins)	RL	0.1 to 1.0 GHz 1.0 to 2.0 GHz 2.0 to 2.7 GHz 3.4 to 3.8 GHz	20 15 12 10	25 20 15 13		dB dB dB dB
0.1 dB Compression Point (ANT_A pin to RFA1/2/3/4/5/6 pins; ANT_B pin to RFB1/2/3/4/5/6 pins)	$P_{0.1dB}$	0.4 GHz to 3.8 GHz	+34	+35		dBm

MIPI Read and Write Timing

MIPI supports the following Command Sequences:

• Register Write

• Register_0 Write

• Register Read

Figures 3 and 4 provide the timing diagrams for register write commands and read commands, respectively. Figure 5 shows the Register 0 Write Command Sequence. Refer to the MIPI Alliance Specification for RF Front-End Control Interface (RFFE), v1.10 (26 July 2011) for additional information on MIPI USID programming sequences and MIPI bus specifications.

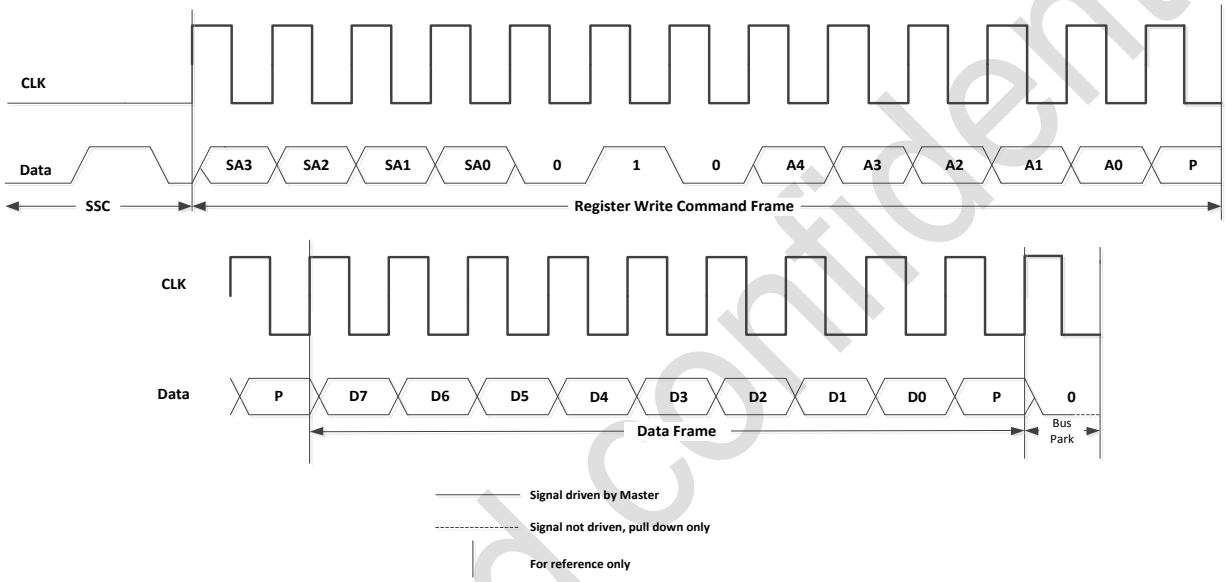


Figure 3 Register Write Command Sequence

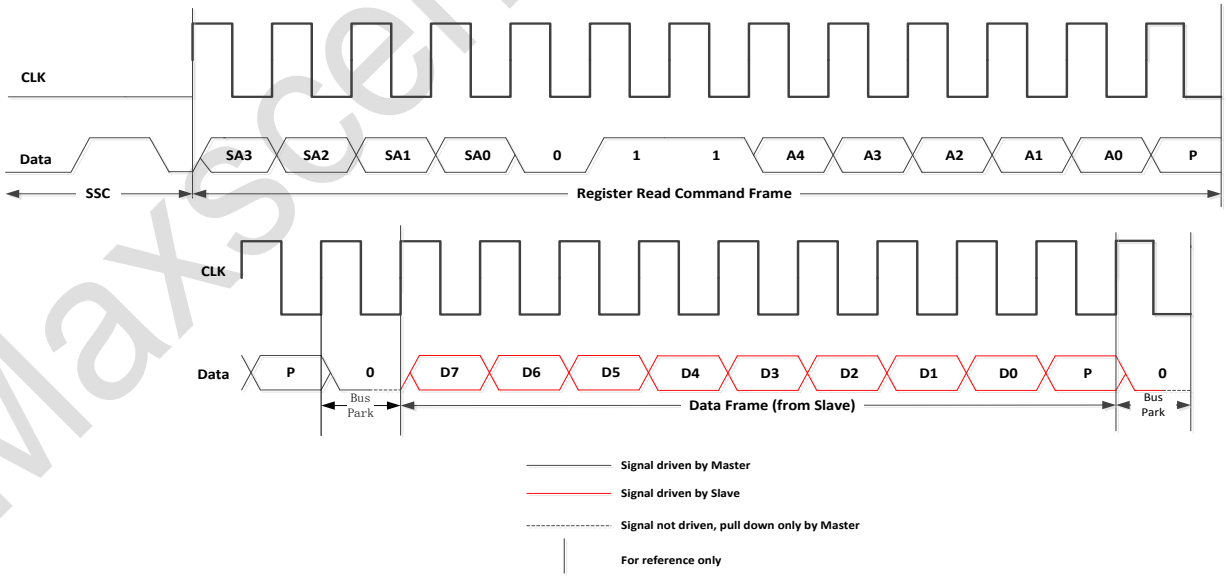


Figure 4 Register Read Command Sequence

In the timing figures, SA[3:0] is slave address. A[4:0] is register address. D[7:0] is data. “P” is odd parity bit.

Register 0 Write Command Sequence

Figure shows the Register 0 Write Command Sequence. The Command Sequence starts with an SSC, followed by the Register 0 Write Command Frame containing the Slave address, a logic one, and a seven bit word to be written to Register 0. The Command Sequence ends with a Bus Park Cycle.

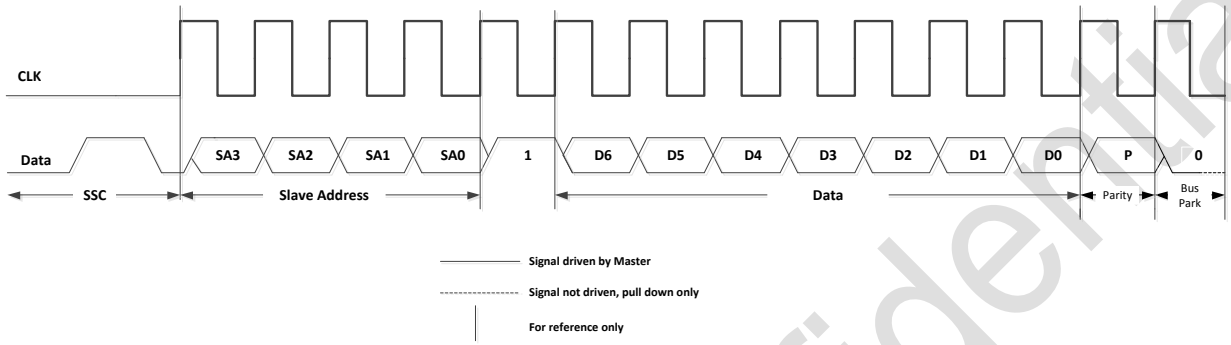


Figure 5 Register 0 Write Command Sequence

Register definition

Table 6. Register definition table

Register Address	Register Name	Data Bits	R/W	Function	Description	Default	BROADCAST_ID support	Trigger support
0x00	REGISTER_0	7:0	R/W	RF Control	Register_0 truth Table: Table 2	0x00	No	Yes
0x01	REGISTER_1	7:0	R/W	RF Control	Register_1 truth Table: Table 3	0x00	No	Yes
0x001B	GROUP_SID	7:4	R	RESERVED		0x0	No	No
		3:0	R/W	GSID	Group Slave ID	0x0	No	No
0x001C	PM_TRIG	7:6	R/W	PWR_MODE	00: Normal Operation (ACTIVE) 01: Reset all registers to default settings (STARTUP) 10: Low power (LOW POWER) 11: Reserved Note: Write PWR_MODE=2'h1 will reset all register, and puts the device into STARTUP state.	0b00	Yes	No
		5	R/W	Trigger_Mask_2	If this bit is set, trigger 2 is disabled	1	No	No
		4	R/W	Trigger_Mask_1	If this bit is set, trigger 1 is disabled	1	No	No
		3	R/W	Trigger_Mask_0	If this bit is set, trigger 0 is disabled Note: When all triggers are disabled, writing to a register that is associated with trigger 0, 1, or 2, causes the data to go directly to the destination register.	1	No	No
		2	W	Trigger_2	A write of a one to this bit loads trigger 2's registers	0	Yes	No
		1	W	Trigger_1	A write of a one to this bit loads trigger 1's registers	0	Yes	No
		0	W	Trigger_0	A write of a one to this bit loads trigger 0's registers Note: Trigger processed immediately then cleared. Trigger 0, 1, and 2 will always read as 0.	0	Yes	No
0x001D	PRODUCT_ID	7:0	R	PRODUCT_ID	Product Number	0x05	No	No
0x001E	MANUFACTURER_ID	7:0	R	MANUFACTURER_ID[7:0]	Lower eight bits of MIPI registered Manufacturer ID	0x81	No	No
0x001F	MAN_USID	7:6	R	RESERVED		0b00	No	No
		5:4	R	MANUFACTURER_ID[9:8]	Upper two bits of MIPI registered Manufacturer ID	0b11	No	No
		3:0	R/W	USID	USID of the device.	0xa	No	No

Absolute Maximum Ratings

Table 7. Maximum ratings

Parameters	Symbol	Minimum	Maximum	Units
Supply voltage	V_{DD}	+2.0	+3.3	V
Supply voltage for MIPI	V_{IO}	+1.0	+2.0	V
MIPI Control voltage (SDATA, SCLK)	V_{CTL}	0	+2.0	V
RF input power	P_{IN}		+36	dBm
Operating temperature	T_{OP}	–20	+85	℃
Storage temperature	T_{STG}	–40	+125	℃
Electrostatic Discharge Human body model (HBM), Class 1C Machine Model (MM), Class A Charged device model (CDM), Class III	 ESD_HBM ESD_MM ESD_CDM		 1500 150 500	 V

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device

Power ON and OFF sequence

Here is the recommendation about power-on/off sequence in order to avoid damaging the device.

Power ON

1) Apply voltage supply - V_{DD}

2) Apply logic supply - V_{IO}

3) Wait 10μs or greater and then apply MIPI bus signals – SCLK and SDATA

4) Wait 5μs or greater after MIPI bus goes idle and then apply the RF Signal

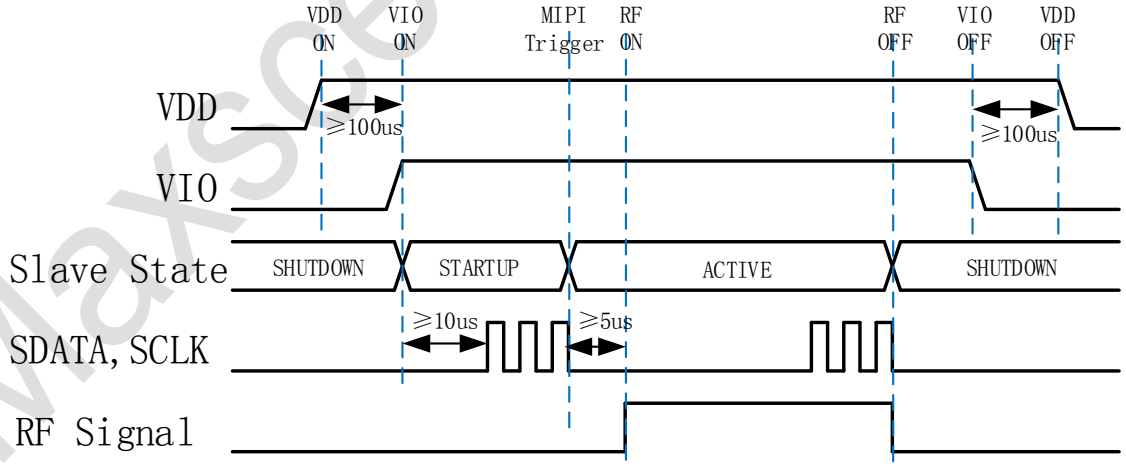
Power OFF

1) Remove the RF Signal

2) Remove MIPI bus – SCLK and SDATA

3) Remove logic supply - V_{IO}

4) Remove voltage supply - V_{DD}

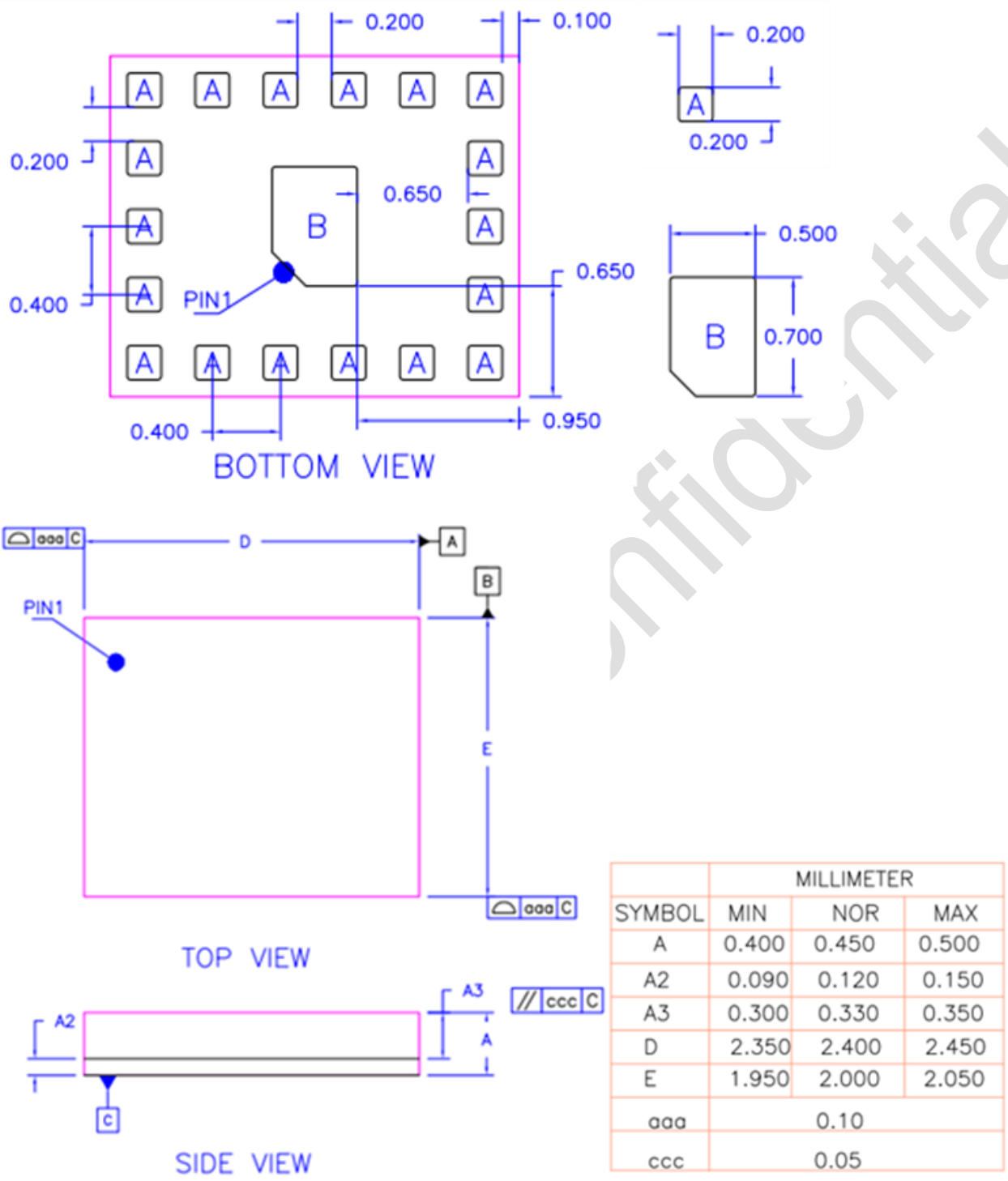


Note: VIO can be applied to the device before VDD or removed after VDD.

It is important to wait 10μs after VIO & VDD are applied before sending SDATA to ensure correction data transmission.

The minimum time between a power up and power down sequence (and vice versa) is ≥ 100us.

Package Outline Dimension



	MILLIMETER		
SYMBOL	MIN	NOR	MAX
A	0.400	0.450	0.500
A2	0.090	0.120	0.150
A3	0.300	0.330	0.350
D	2.350	2.400	2.450
E	1.950	2.000	2.050
aaa	0.10		
ccc	0.05		

Figure 6 package outline dimension

Reflow Chart

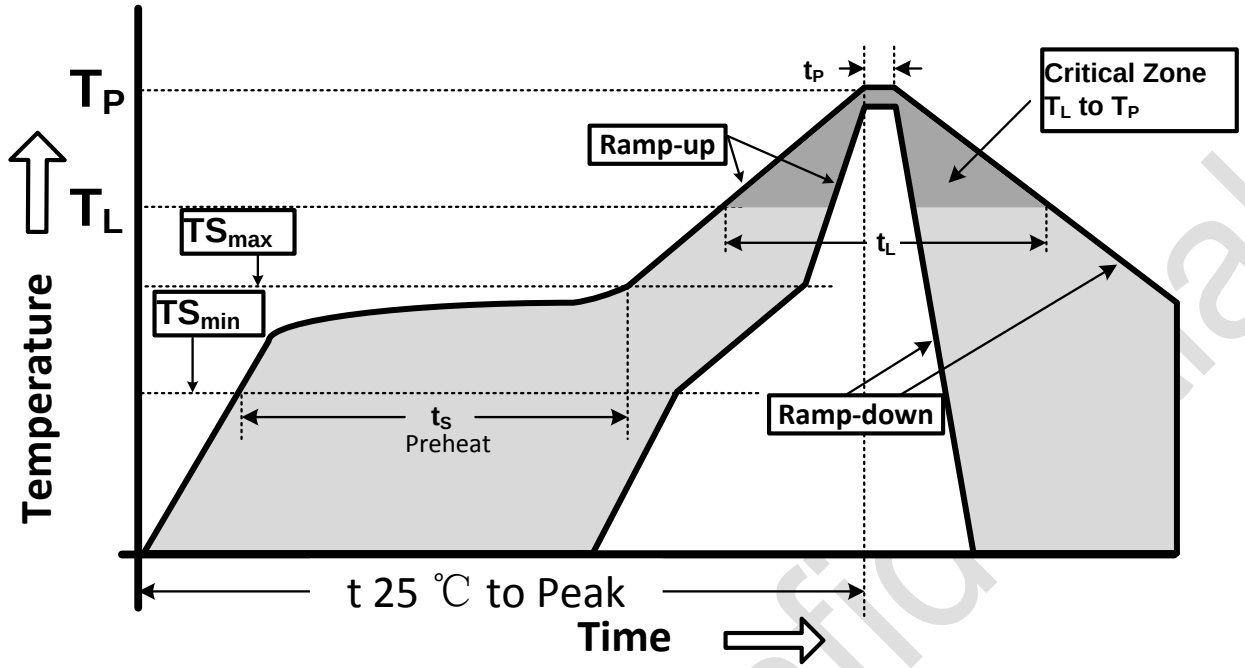


Figure 7 Recommended Lead-Free Reflow Profile

Table 7. Reflow condition

Profile Parameter	Lead-Free Assembly, Convection, IR/Convection
Ramp-up rate（TS_{max} to T_p）	3℃/second max.
Preheat temperature（TS_{min} to TS_{max}）	150℃ to 200℃
Preheat time（t_s）	60 - 180 seconds
Time above TL , 217℃（t_L）	60 - 150 seconds
Peak temperature（T_p）	260℃
Time within 5℃ of peak temperature(t_p)	20 - 40 seconds
Ramp-down rate	6℃/second max.
Time 25℃ to peak temperature	8 minutes max.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electric charge. Proper ESD protection techniques should be used when handling these devices.

RoHS Compliant

This product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE), and are considered RoHS compliant.