PRELIMINARY

MX98715A

SINGLE CHIP FAST ETHERNET NIC CONTROLLER

1. FEATURES

- A single chip solution integrates 100/10 Base-T fast Ethernet MAC, PHY and PMD
- Fully comply to IEEE 802.3u specification
- Operates over 100 meters of STP and category 5 UTP cable
- Fully comply to PCI spec. 2.1 up to 33MHz
- Fully comply to Advanced Configuration and Power Interface (ACPI) Rev 1.0
- Fully comply to PCI Bus Power Management Interface spec. Rev 1.0
- Support full and half duplex operations in both 100 Base-TX and 10 Base-T mode
- Magic Packet™ mode to support Remote-Wake-Up and Remote-Power-On
- 100/10 Base-T NWAY auto negotiation function
- Large on-chip FIFOs for both transmit and receive operations without external local memory
- Bus master architecture with linked host buffers delivers the most optimized performance
- 32-bit bus master DMA channel provides ultra low CPU utilization, best fit in server and windows application.
- Proprietary Adaptive Network Throughput Control (ANTC) technology to optimize data integrity and throughput
- Support up to 64K bytes boot ROM interface
- Three levels of loopback diagnositic capability
- Support a variety of flexible address filtering modes with 16 CAM address and 512 bits hash
- MicroWire interface to EEPROM for customer's IDs and configuration data
- Single +5V power supply, CMOS technology, 128-pin PQFP package/LQPF package

(Magic Packet Technology is a trademark of Advanced Micro Device Corp.)

2. GENERAL DESCRIPTIONS

The MX98715A controller is an IEEE802.3u compliant single chip 32-bit full duplex, 10/100Mbps highly integrated Fast Ethernet combo solution, designed to address high performance local area networking (LAN) system application requirements.

MX98715A's PCI bus master architecture delivers the optimized performance for future high speed and powerful processor technologies. In other words, the MX98715A not only keeps CPU utilization low while maximizing data throughput, but it also optimizes the PCI bandwidth providing the highest PCI bandwidth utilization. To further reduce maintenance costs the MX98715A uses drivers that are backward compatible with the original MXIC MX98713 series controllers.

The MX98715A contains a PCI local bus glueless interface, a Direct Memory Access (DMA) buffer management unit, an IEEE802.3u-compliant Media Access Controller (MAC), large Transmit and Receive FIFOs, and an on-chip 10 Base-T and 100 Base-TX transceiver simplifying system design and improving high speed signal quality. Full-duplex operation are supported in both 10 Base-T and 100 Base-TX modes that increases the controller's operating bandwidth up to 200Mbps. Equipped with intelligent IEEE802.3u-compliant auto-negotiation, the MX98715A-based adapter allows a single RJ-45 connector to link with the other IEEE802.3u-compliant device without re-configuration.

In MX98715A, an innovative and proprietary design "Adaptive Network Throughput Control" (ANTC) is built-in to configure itself automatically by MXIC's driver based on the PCI burst throughput of different PCs. With this proprietary design, MX98715A can always optimize its operating bandwidth, network data integrity and throughput for different PCs.

The MX98715A features Remote-Power-On and Remote-Wake-Up capability and is compliant with the Advanced Configuration and Power Interface version 1.0 (ACPI). This support enables a wide range of wake-up capabilities, including the ability to customize the content of specified packet which PC should be responded to, even when it is in a low-power state. PCs and workstations could take advantage of these capabilities of being waked up and served simultaneously over the network by remote server or workstation. It helps organizations reduce their maintenance cost of PC network.

The 32-bit multiplexed bus interface unit of MX98715A provides a direct interface to a PCI local bus, simplifing the design of an Ethernet adapter in a PC system. With its on-chip support for both little and big endian byte alignment, MX98715A can also address non-PC applications.

3. PIN CONFIGURATIONS

4. PIN DESCRIPTION (128 PIN PQFP)

(T/S : tri-state, S/T/S : sustended tri-state, I : input, O : output, O/D : open drain)

Pin Name	Type	Pin No	128 Pin Function and Driver
AD[31:0]	T/S	116, 117 119,120, 122,124, 125,127, 3,4,6,7,9, 10,12,13, 26,28,29, 31-33,35, 36,38,39, 41,42,44, 45,47,48	PCI address/data bus: shared PCI address/data bus lines. Little or big endian byte ordering are supported.
CBE[3:0]	T/S	128,14 25,37	PCI command and byte enable bus: shared PCI command byte enable bus, during the address phase of the transaction, these four bits provide the bus command. During the data phase, these four bits provide the byte enable.
FRAMEB	S/T/S	15	PCI FRAMEB signal: shared PCI cycle start signal, asserted to indicate the beginning of a bus transaction. As long as FRAMEB is asserted, data transfers continue.
TRDYB	S/T/S	18	PCI Target ready: issued by the target agent, a data phase is completed on the rising edge of PCICLK when both IRDYB and TRDYB are asserted.
IRDYB	S/T/S	17	PCI Master ready: indicates the bus master's ability to complete the current data phase of the transaction. A data phase is completed on any rising edge of PCICLK when both IRDYB and TRDYB are asserted.
DEVSELB	S/T/S	19	PCI slave device select: asserted by the target of the current bus access. When 98715A is the initiator of current bus access, the target must assert DEVSELB within 5 bus cycles, otherwise cycle is aborted.
IDSEL	I	1	PCI initialization device select: target specific device select signal for configuration cycles issued by host.
PCICLK	I	113	PCI bus clock input: PCI bus clock range from 16MHz to 33MHz.
RSTB	I	112	PCI bus reset: host system hardware reset.
LANWAKE	O	110	Power Management Event:When high indicating a power management event occures, such as detection of a Magic packet, a wake up frame, or link change.
INTAB	O/D	111	PCI bus interrupt request signal: wired to INTAB line.
SERRB	O/D	23	PCI bus system error signal: If an address parity error is detected and CFCS bit 8 is enabled, SERRB and CFCS's bit 30 will be asserted.
PERRB	S/T/S	22	PCI bus data error signal: As a bus master, when a data parity error is detected and CFCS bit 8 is enabled, CFCS bit 24 and CSR5 bit 13 will be asserted. As a bus target, a data parity error will cause PERRB to be asserted.

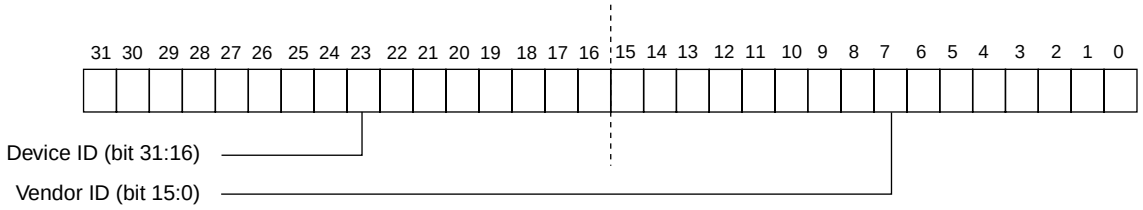
Pin Name	Type	Pin No	128 Pin Function and Driver
PAR	T/S	24	PCI bus parity bit: shared PCI bus even parity bit for 32 bits AD bus and CBE bus.
STOPB	S/T/S	20	PCI Target requested transfer stop signal: as bus master, assertion of STOPB cause MX98715A either to retry, disconnect, or abort.
REQB	T/S	115	PCI bus request signal: to initiate a bus master cycle request
GNTB	I	114	PCI bus grant acknowledge signal: host asserts to inform MX98715A that access to the bus is granted
BPA1 (EEDI)	O	61	Boot PROM address bit 1(EECS=0): together with BPA[15:0] to access external boot PROM up to 256KB. EEPROM data in(EECS=1): EEPROM serial data input pin.
BPA0 (EECK)	O	60	Boot PROM address bit 0(EECS=0): together with BPA[15:0] to access external boot PROM up to 256KB. EEPROM clock(EECS=1): EEPROM clock input pin
BPA[15:0]	O	78-76, 73-70, 68-60	Boot PROM address line.
BPD0 (EEDO)	T/S	58	Boot PROM data line 0(EECS=0): boot PROM or flash data line 0. EEPROM data out(EECS=1): EEPROM serial data outpin(during reset initialization).
BPD[7:0]	T/S	51-58	Boot PROM data lines: boot PROM or flash data lines 7-0.
EECS	O	59	EEPROM Chip Select pin.
BOEB	O	69	Boot PROM Output Enable.
RDA	O	83	Connecting an external resistor to ground, Resistor value=510 ohms
RTX	O	102	Connecting an external resistor to ground, Resistor value=510 ohms
RTX2EQ	O	101	No connection.
NC	I	100	No Connection.
RXIP	I	92	Twisted pair receive differential input: Support both 10 Base-T and 100 Base-TX receive differential input.
RXIN	I	91	Twisted pair receive differential input: Support both 10 Base-T and 100 Base-TX receive differential input
TXOP	O	98	Twisted pair transmit differential output: Support both 10 Base-T and 100 Base-TX transmit differential output
TXON	O	97	Twisted pair transmit differential output: Support both 10 Base-T and 100 Base-TX transmit differential output
CKREF	I	85	Reference clock: 25MHz oscillator clock input
LED0	O	79	Programmable LED pin 0: CSR9.28=1 Set the LED as Link Speed (10/100) LED. CSR9.28=0 Set the LED as Activity LED. Default is activity LED after reset.

Pin Name	Type	Pin No	128 Pin Function and Driver
LED1	O	80	Programmable LED pin 1: CSR9.29=1 Set the LED as Link/Activity LED. CSR9.29=0 Set the LED as Good Link LED. Default is Good Link LED after reset.
VDD	I	8,21,30,43, 49,74,81,84, 88,90,93,96, 103,106,108, 121	Power pins.
GND	I	2,5,11,16,27 34,40,46,50 75,82,86,87 89,94,95,99 104,105,107 109,118,123, 126	Ground pins.

5. PROGRAMMONG INTERFACE

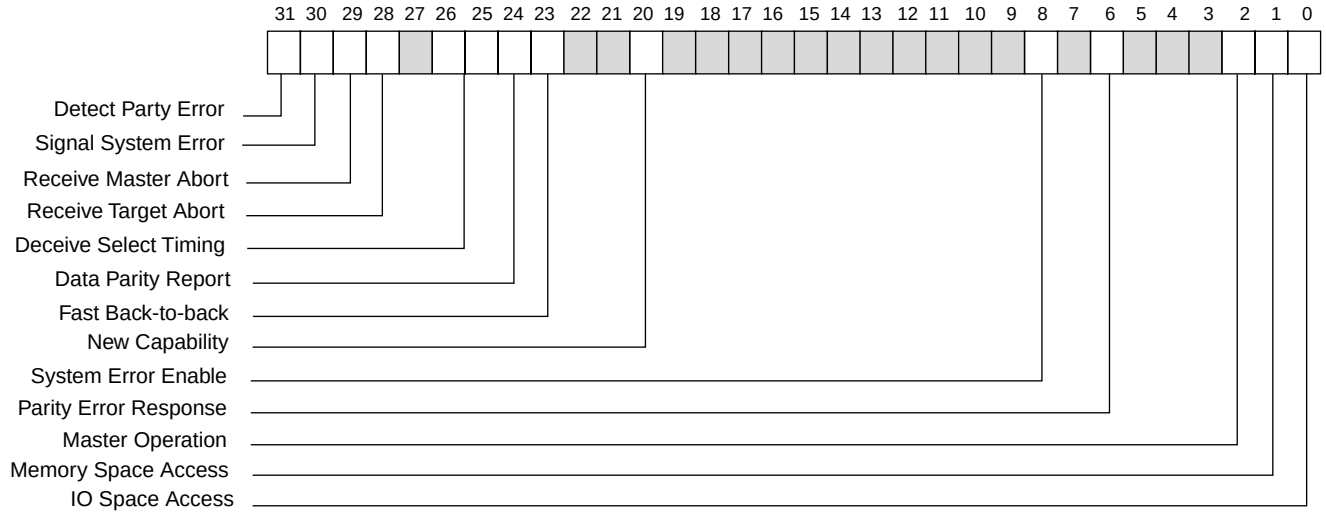
5.1 PCI CONFIGURATION REGISTERS:

5.1.1 PCI ID REGISTER (PFID) (Offset 03h-00h)



This register can be loaded from external serial EEPROM or use a MXIC preset value of "10D9" and "0531" for vendor ID and device ID respectively. Word location 3Eh and 3Dh in serial EEPROM are used to configure customer's vendor ID and device ID respectively. If location 3Eh contains"FFFF" value then MXIC'svendor ID and device ID will be set in this register, otherwise both 3Eh and 3Dh will be loaded into this register from serial EEPROM.

5.1.2 PCI COMMAND AND STATUS REGISTER (PFCS) (Offset 07h-04h)

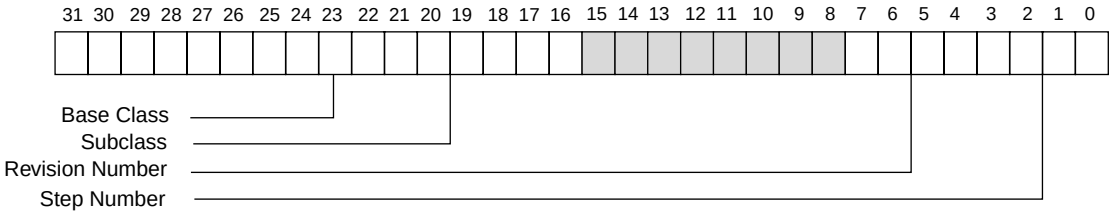


The bit content will be reset to 0 when a 1 is written to the corresponding bit location.

bit 0 : IO Space Access, set to 1 enable IO access
bit 1 : Memory Space Access, set to 1 to enable memory access
bit 2 : Master Operation, set to 1 to support bus master mode
bit 5-3 : not used
bit 6 : Parity Error Response, set to 1 to enable assertion of CSR<13> bit if parity error detected.
bit 7 : not used
bit 8 : System Error Enable, set to 1 to enable SERR# when parity error is detected on address lines and CBE[3:0].
bit 20 : New capability. Set to support PCI power management.
bit 22-bit19 : not used
bit 23 : Fast Back-to back, always set to accept fast back-to-back transactions that are not sent to the same bus device.

bit 24:Data parity Report, is set to 1 only if PERR# active and PFCS<6> is also set.
bit 26-25:Device Select Timing of DEVSELB pin.
bit 27:not used
bit 28:Receive Target Abort, is set to indicate a transaction is terminated by a target abort.
bit 29:Receive Master Abort, is set to indicate a master transaction with Master abort.
bit 30:Signal System Error, is set to indicate assertion of SERR#.
bit 31:Detected Parity Error, is set whenever a parity error detected regardless of PFCS<6>.

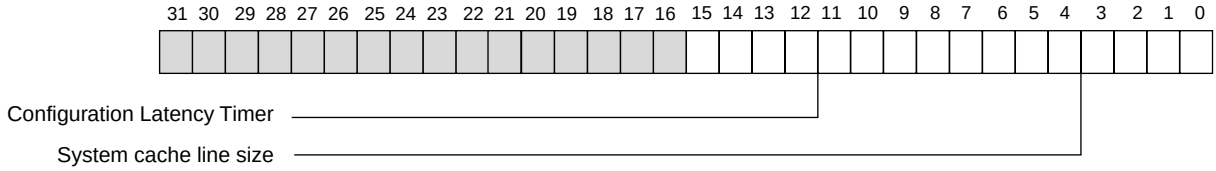
5.1.3 PCI REVISION REGISTER (PFRV) (Offset 0Bh-08h)



bit 3 - 0 : Step Number, range from 0 to Fh.
bit 7 - 4 : Revision Number, fixed to 2h for MX98715A
bit 15 - 8 : not used
bit 23 - 16 : Subclass, fixed to 0h.
bit 31 - 24 : Base Class, fixed to 2h.

5.1.4 PCI LATENCY TIMER REGISTER (PFLT) (Offset 0Fh-0Ch)

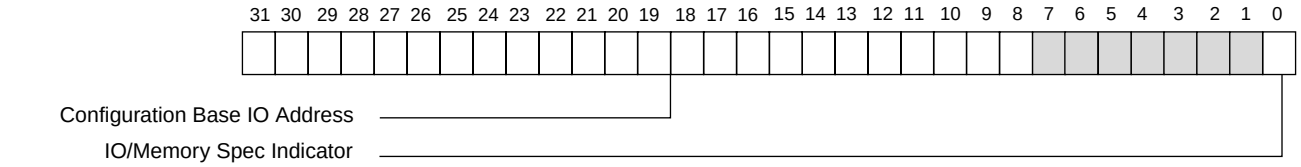
PFLT Register (0Fh-0Ch)



bit 0 - bit 7 : System cache line size in units of 32 bit word, device driver should use this value to program CSR0<15:14>.
bit 8 - bit 15 : Configuration Latency Timer, when MX98715A assert FRAME#, it enables its latency timer to count.

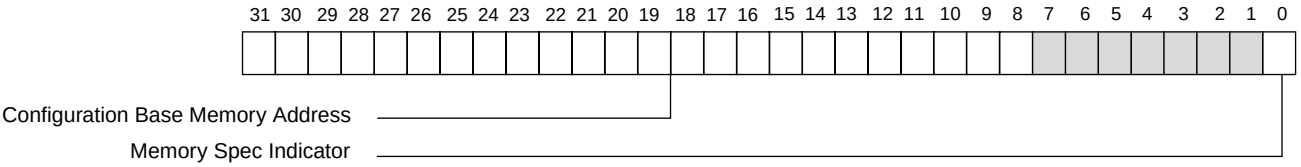
If MX98715A deasserts FRAME# prior to timer expiration, then timer is ignored. Otherwise, after timer expires, MX98715A initiates transaction termination as soon as its GNT# is deasserted.

5.1.5 PCI BASE IO ADDRESS REGISTER (PBIO) (Offset 13h-10h)



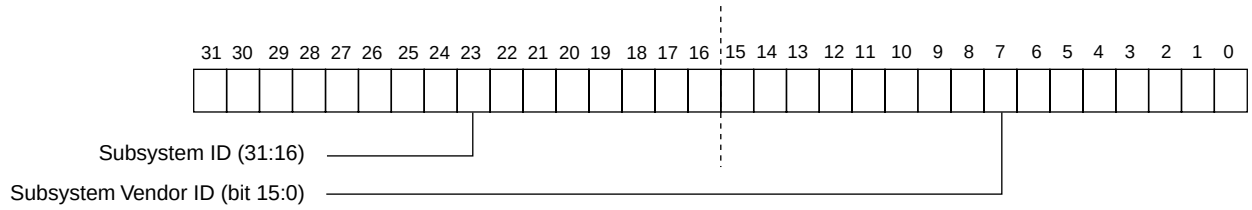
bit 0 : IO/Memory Space Indicator, fixed to 1 in this field will map into the IO space. This is a read only field.
bit 7 - 1 : not used, all 0 when read
bit 31 - 8 : Defines the address assignment mapping of MX98715A CSR registers.

5.1.6 PCI Base Memory Address Register (PBMA) (Offset 17h-14h)



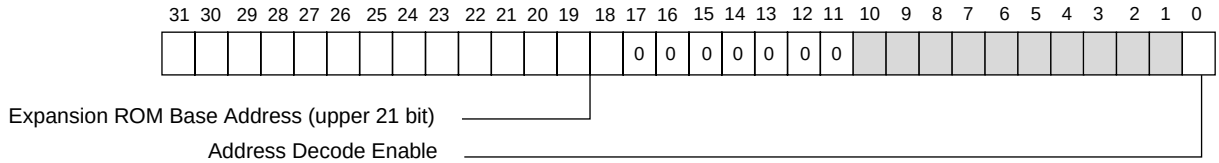
bit 0 : Memory Space Indicator, fixed to 0 in this field will map into the memory space. This is a read only field.
bit 6 - 1 : not used, all 0 when read
bit 31 - 7 : Defines the address assignment mapping of MX98715A CSR registers.

5.1.7 PCI SUBSYSTEM ID REGISTER (PSID) (Offset 2Ch-2Fh)



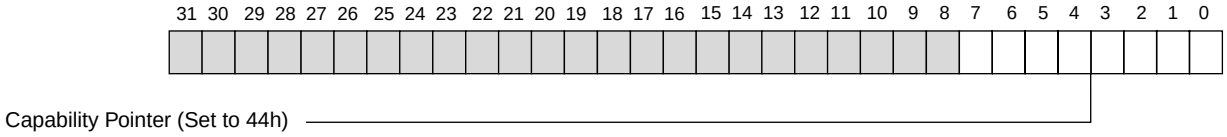
This register is used to uniquely identify the add-on board or subsystem where the NIC controller resides. Values in this register are loaded directly from external serial EEPROM after system reset automatically. Word location 36h of EEPROM is subsystem vendor ID and location 35h is sub-system ID.

5.1.8 PCI BASE EXPANSION ROM ADDRESS REGISTER (PBER) (Offset 33h-30h)



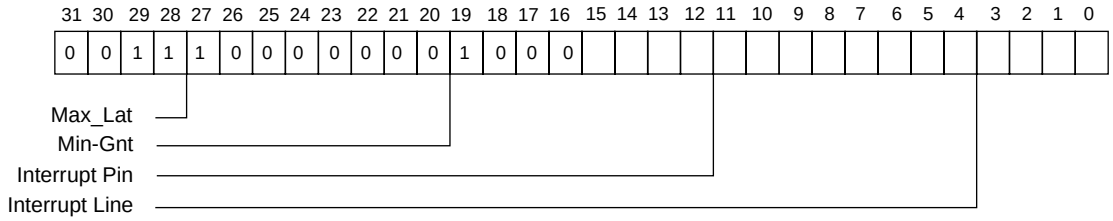
bit 0 : Address Decode Enable, decoding will be enabled if only both enable bit in PFCS<1> and this expansion ROM register are 1.
bit 10 - 1 : not use
bit 31 - 11 : Defines the upper 21 bits of expansion ROM base address.

5.1.9 PCI CAPABILITY POINTER REGISTER (PFCP) (Offset 37h-34h)



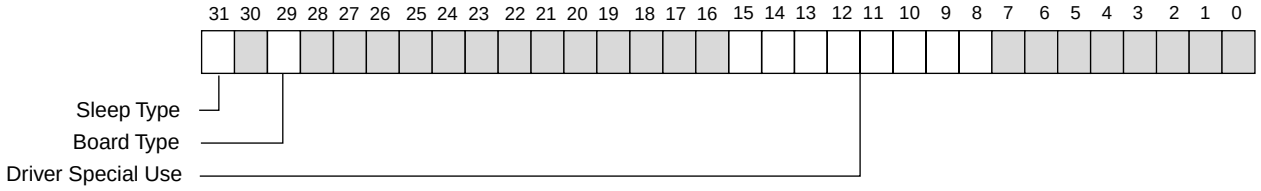
bit 7- 0 : Capability pointer (Cap_Ptr) is set to 44h if PMEB is connected to PCI bus, otherwise 00.
bit 31- 8 : reserved

5.1.10 INTERRUPT REGISTER (PFIT) (Offset 3Fh-3Ch)



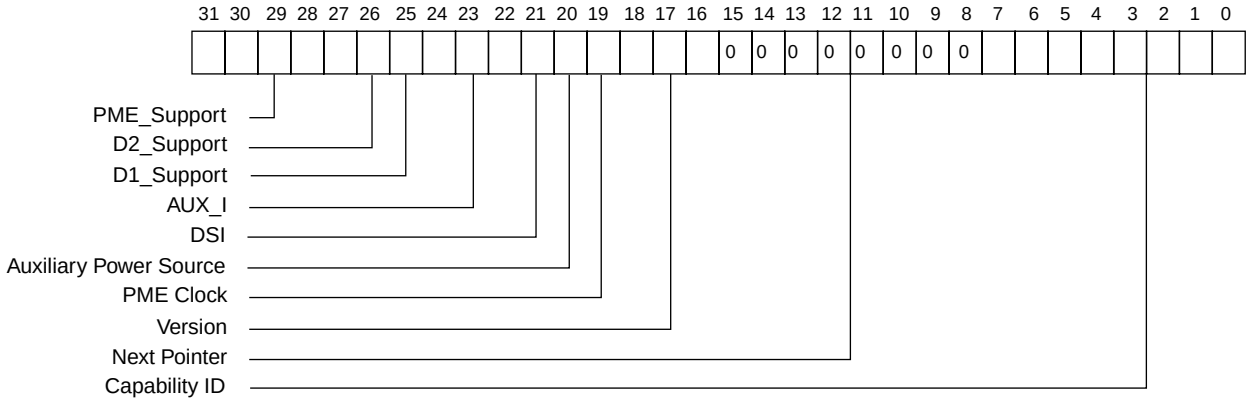
bit 7 - 0 : Interrupt Line, system BIOS will writes the routing information into this field, driver can use this information to determine priority and interrupt vector.
bit 15 - 8 : Interrupt Pin, fixed to 01h which use INTA#.
bit 31 - 24 : Max_Lat which is a maximum period for a access to PCI bus.
bit 23 - 16 : Min_Gnt which is the maximum period that MX98715A needs to finish a brust PCI cycle.

5.1.11 PCI DRIVER AREA REGISTER (PFDA) (43h-40h)



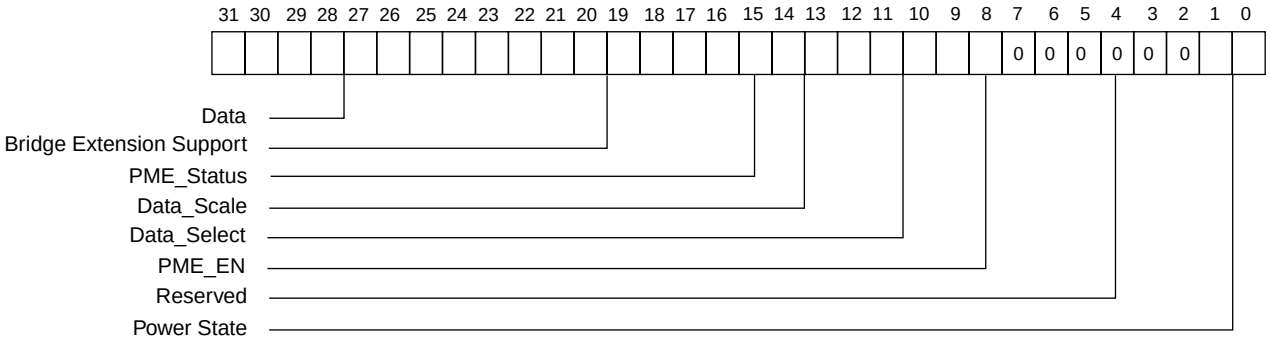
bit 31 : Sleep Mode, set to sleep mode which allows access to PCI configuration space, a hardware reset or reset to this bit can exit from sleep mode. Magic packet can be received under sleep mode if CSR<22> (Magic Packet Enable) is set.
bit 30 : not used
bit 29 : board type
bit 15 - 8 : driver is free to read and write this field for any purpose.
bit 7 - 0 : not used.

5.1.12 PCI POWER MANAGEMENT CAPABILITY REGISTER (PPMC) (47h-44h)



bit 31- 27 : PME_Support, read only indicates the power states in which the function may assert LANWAKE pin.
bit 31 ---- PME_D3cold (value=1)
bit 30 ---- PME_D3warm (value=1)
bit 29 ---- PME_D2 (value=1)
bit 28 ---- PME_D1 (value=1)
bit 27 ---- PME_D0 (value=1)
bit 26 : D2 mode support, read only, set to 1.
bit 25 : D1 mode support, read only, set to 1.
bit 24-22 : AUX_I bits. Auxiliary current field, set to 100.
bit 21 : DSI, read only, set to 0.
bit 20 : Auxiliary power source, set to 1. This bit only valid when bit 15 is a '1'.
bit 19 : PME Clock, read only, set to 0.
bit 18-16 : PCI power management version, set to 001, read only.
bit 15-8 : Next Pointer, all bits set to 0.
bit 7-0 : Capability ID, read only, a 1 indicates that the data structure currently being pointed to is the PCI power managment data structure.

5.1.13 PCI POWER MANAGEMENT COMMAND AND STATUS REGISTER (PPMCSR) (4Bh-48h)



bit 1-0 : Power_State, read/write, D0 mode is 00, D1 mode is 01, D2 mode is 10, D3 hot mode is 11.
bit7-2 : all 0. Reserved.
bit8 : PME_EN, set 1 to enable LANWAKE. Set 0 to disable LANWAKE assertion.
bit 12-9 : Data_Select for report in the Data register located at bit 31:24.
bit 14-13 : Data_Scale, read only.
bit 15 : PME_Status independent of the state of PME_EN.
When set, indicates a assertion of LANWAKE pin. (support D3 cold).
Write 1 to clear the LANWAKE signal. Write 0, no effect.
bit 21-16 : Reserved.
bit 22 : B2_B3#, B2_B3 support for D3 hot, meaningful only if BPCC_EN = 1, read only.
bit 23 : BPCC_EN, Bus Power/Clock Control Enable, read only.
bit 31-24 : Data, read only.

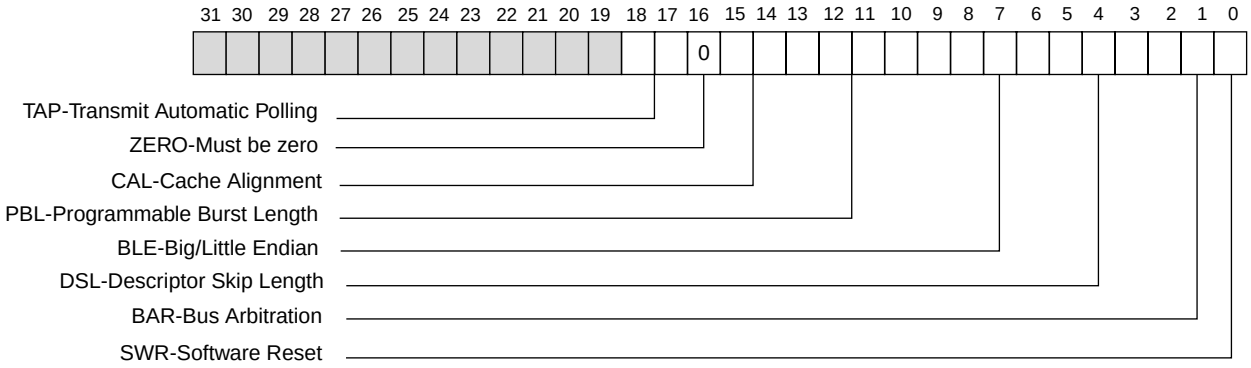
5.2 HOST INTERFACE REGISTERS

MX98715A CSRs are located in the host I/O or memory address space. The CSRs are double word aligned and 32 bits long. Definitions and address for all CSRs are as follows :

CSR Mapping

Register	Meaning	Offset from CSR Base Address (PBIO and PBMA)
CSR0	Bus mode	00
CSR1	Transmit poll demand	08h
CSR2	Receive poll demand	10h
CSR3	Receive list demand	18h
CSR4	Transmit list base address	20h
CSR5	Interrupt status	28h
CSR6	Operation mode	30h
CSR7	Interrupt enable	38h
CSR8	Missed frame counter	40h
CSR9	Serial ROM and MII management	48h
CSR10	Reserved	50h
CSR11	General Purpose timer	58h
CSR12	10 Base-T status port	60h
CSR13	SIA Reset Register	68h
CSR14	10 Base-T control port	70h
CSR15	Watchdog timer	78h
CSR16	Magic Packet Register	80h
CSR20	NWay Status Register	A0h

5. 2.1 BUS MODE REGISTER (CSR0)

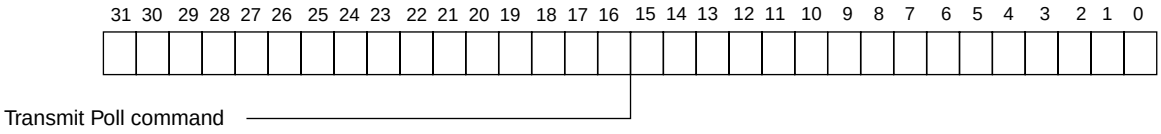


Field	Name	Description
0	SWR	Software Reset, when set, MX98715A resets all internal hardware with the exception of the configuration area and port selection.
1	BAR0	Internal bus arbitration scheme between receive and transmit processes. The receive channel usually has higher priority over transmit channel when receive FIFO is partially full to a threshold. This threshold can be selected by programming this bit. Set for lower threshold, reset for normal threshold.
6:2	DSL	Descriptor Skip Length, specifies the number of longwords to skip between two descriptors.
7	BLE	Big/Little Endian, set for big endian byte ordering mode, reset for little endian byte ordering mode, this option only applies to data buffers
13:8	PBL	Programmable Burst Length, specifies the maximum number of longwords to be transferred in one DMA transaction. default is 0 which means unlimited burst length, possible values can be 1,2,4,8,16,32 and unlimited .
15:14	CAL	Cache Alignment, programmable address boundaries of data burst stop, MX98715A can handle non-cache- aligned fragement as well as cache-aligned fragment efficiently.
18:17	TAP	Transmit Auto-Polling time interval, defines the time interval for MX98715A to performs transmit poll command automatically at transmit suspended state.

TABLE 5.2.0 TRANSMIT AUTO POLLING BITS

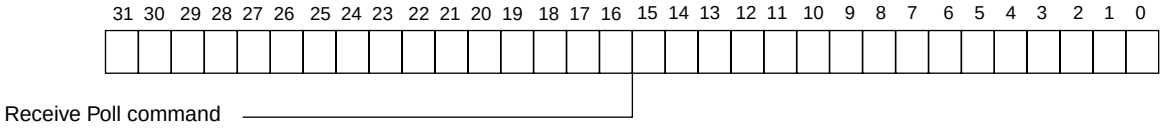
CSR<18:17>	Time Interval
00	No transmit auto-polling, a write to CSR1 is required to poll
01	auto-poll every 200 us
10	auto-poll every 800 us
11	auto-poll every 1.6 ms

5.2.2 TRANSMIT POLL COMMAND (CSR1)



Field	Name	Description
31:0	TPC	Write only, when written with any value, MX98715A read transmit descriptor list in host memory pointed by CSR4 and processes the list.

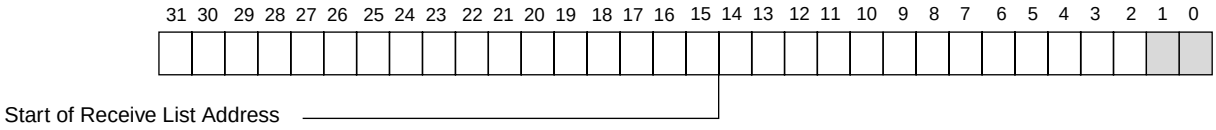
5.2.3 RECEIVE POLL COMMAND (CSR2)



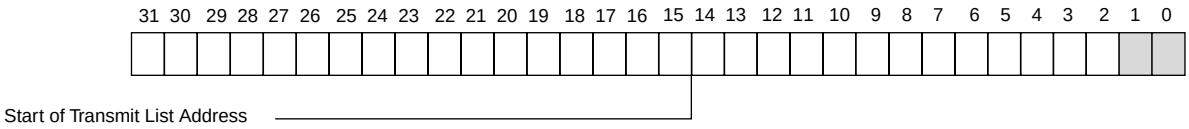
Field	Name	Description
31:0	RPC	Write only, when written with any value, MX98715A read receive descriptor list in host memory pointed by CSR4 and processes the list.

5.2.4 DESCRIPTOR LIST ADDRESS (CSR3, CSR4)

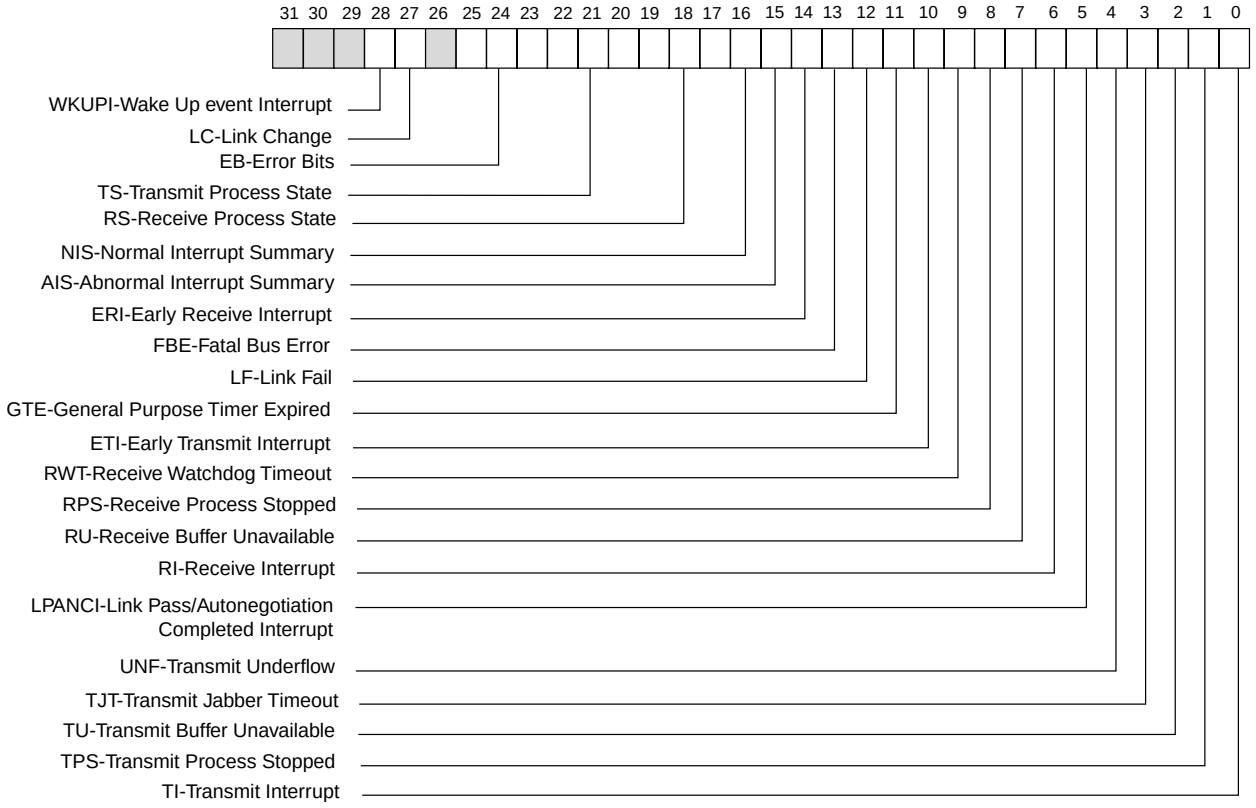
CSR3 Receive List Base Address



CSR4 Traansmit List Base Address



5.2.5 STATUS REGISTER (CSR5)



Field	Name	Description
28	WKUPI	Wake Up event interrupt. Valid only if CSR16<22> bit is set.
27	LC	100 Base-TX link status has changed either from pass to fail or fail to pass. Read CSR12<1> for 100 Base-TX link status.
25:23	EB	Error Bits, read only, indicating the type of error that casued fatal bus error.
22:20	TS	Transmit Process State, read only bits indicating the state of transmit process.
19:17	RS	Receive Process State, read only bits indicating the state of receive process.
16	NIS	Normal Interrupt Summary, is the logical OR of CSR5<0>, CSR5<2> and CSR5<6> and CSR5<28>.
15	AIS	Abnormal Interrupt Summary, is the logical OR of CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CAR5<10>, CSR5<11> and CSR5<13>, CSR5<27>.
14	ERI	Early receive interrupt, indicating the first buffer has been filled in ring mode, or 64 bytes has been received in chain mode.
13	FBE	Fatal Bus Error, indicating a system error occured, MX98715A will disable all bus access.
12	LF	Link Fail, indicates a link fail state in 10 Base-T port. This bit is valid only when CSR6<18>=0, CSR14<8>=1, and CSR13<3>=0.
11	GTE	General Purpose Timer Expired, indicating CSR11 counter has expired.

Field	Name	Description
10	ETI	Early Transmit Interrupt, indicating the packet to be transmitted was fully transferred to internal TX FIFO. CSR5<0> will automatically clears this bit.
9	RWT	Receive Watchdog Timeout, reflects the network line status where receive watchdog timer has expired while the other node is still active on the network.
8	RPS	Write only, when written with any value, MX98715A reads receive descriptor list in host memory pointed by CSR4 and processes the list.
7	RU	Receive Buffer Unavailable, the receive process is suspended due to the next descriptor in the receive list is owned by host. If no receive poll command is issued, the reception process resumes when the next recognized incoming frame is received.
6	RI	Receive Interrupt, indicating the completion of a frame reception.
5	UNF	Transmit Underflow, indicating transmit FIFO has run empty before the completion of a packet transmission.
4	LPANCI	When autonegotiation is not enabled (CSR14<7>=0), this bit indicates that the 10 Base-T link integrity test has completed successfully, after the link was down. This bit is also set as as a result of writing 0 to CSR14<12> (Link Test Enable). When Autonegotiation is enabled (CSR14<7> =1) , this bit indicates that the autonegotiation has completed (CSR12<14:12>=5). CSR12 should then be read for a link status report. This bit is only valid when CSR6<18>=0, i.e. 10 Base-T port is selected Link Fail interrupt (CSR5<12>) will automatically clears this bit.
3	TJT	Transmit Jabber Timeout, indicating the MX98715 has been excessively active. The transmit process is aborted and placed in the stopped state. TDES0<1> is also set.
2	TU	Transmit Buffer Unavailable, transmit process is suspended due to the next descriptor in the transmit list is owned by host.
1	TPS	Transmit Process Stopped.
0	TI	Transmit Interrupt. indicating a frame transmission was completed.

TABLE 5.2.1 FATAL BUS ERROR BITS

CSR5<25:23>	Process State
000	parity error for either SERR# or PERR#, cleared by software reset.
001	master abort
010	target abort
011	reserved
1XX	reserved

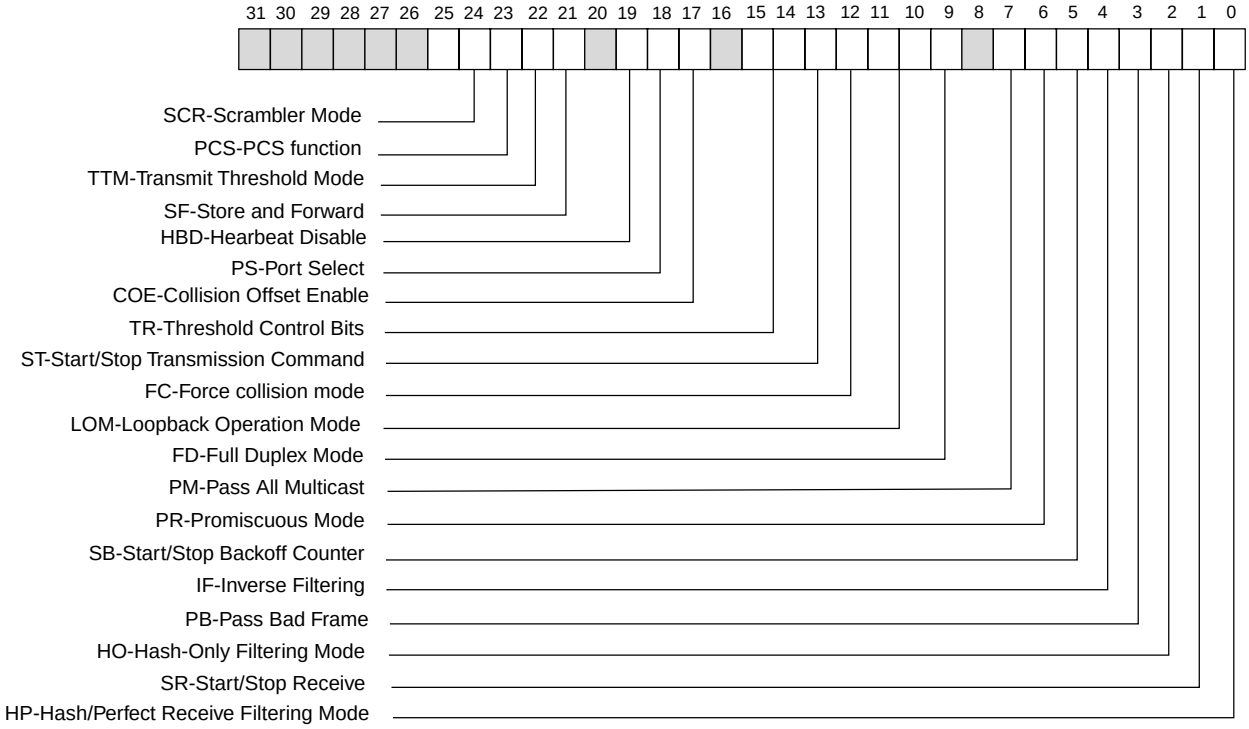
TABLE 5.2.2 TRANSMIT PROCESS STATE

CSR5<22:20>	Process State
000	Stopped- reset or transmit jabber expired.
001	Fetching transmit descriptor
010	Waiting for end of transmission
011	filling transmit FIFO
100	reserved
101	Setup packet
110	Suspended, either FIFO underflow or unavailable transmit descriptor
111	closing transmit descriptor

TABLE 5.2.3 RECEIVE PROCESS STATE

CSR5<19:17>	Process State
000	Stopped- reset or stop receive command. Fetching receive descriptor
010	checking for end of receive packet
011	Waiting for receive packet
100	Suspended, receive buffer unavailable
101	closing receive descriptor
110	Purging the current frame from the receive FIFO due to unavailable receive buffer
111	queuing the receive frame from the receive FIFO into host receive buffer

5.2.6 OPERATION MODE REGISTER (CSR6)



Field	Name	Description
24	SCR	Scrambler Mode, default is set to enable scrambler function. Not affected by software reset.
23	PCS	Default is set to enable PCS functions. CSR6<18> must be set in order to operate in symbol mode.
22	TTM	Transmit Threshold Mode, set for 10 Base-T and reset for 100 Base-TX.
21	SF	Store and Forward, when set, transmission starts only if a full packet is in transmit FIFO. the threshold values defined in CSR6<15:14> are ignored
19	HBD	Heartbeat Disable, set to disable SQE function in 10 Base-T mode.
18	PS	Port Select, deafult is 0 which is 10 Base-T mode, set for 100 Base-TX mode. A software reset does not affect this bit.
17	COE	Collision Offset Enable, set to enable a modified backoff algorithm during low collision situation, reset for normal backoff algorithm.
15:14	TR	Threshold Control Bits, these bits controls the selected threshold level for MX98715A's transmit FIFO, transmission starts when frame size within the transmit FIFO is larger than the selected threshold. Full frames with a length less than the threshold are also transmitted.

Field	Name	Description
13	ST	Start/Stop Transmission Command, set to place transmission process in running state and will try to transmit current descriptor in transmit list. When reset, transmit process is placed in stop state.
12	FC	Force Collision Mode, used in collision logic test in internal loopback mode, set to force collision during next transmission attempt. This can result in excessive collision reported in TDES0<8> if 16 or more collision.
11:10	LOM	Loopback Operation Mode, see table 5.2.6.
9	FD	Full-Duplex Mode, set for simultaneous transmit and receive operation, heart beat check is disabled, TDES0<7> should be ignored, and internal loopback is not allowed. This bit controls the value of bit 6 of link code word .
7	PM	Pass All Multicast, set to accept all incoming frames with a multicast destination address are received. Incoming frames with physical address are filtered according to the CSR6<0> bit.
6	PR	Promiscuous Mode, any incoming valid frames are accepted, default is reset and not affected by software reset.
5	SB	Start/Stop Backoff Counter, when reset, the backoff timer is not affected by the network carrier activity. Otherwise, timer will start counting when carrier drops.
4	IF	Inverse Filtering, read only bit, set to operate in inverse filtering mode, only valid during perfect filtering mode.
3	PB	Pass Bad Frames, set to pass bad frame mode, all incoming frames passed the address filtering are accepted including runt frames, collided fragments, truncated frames caused by FIFO overflow.
2	HO	Hash-Only Filtering Mode , read only bit, set to operate in imperfect filtering mode for both physical and multicast addresses.
1	SR	Start/Stop Receive, set to place receive process in running state where descriptor acquisition is attempted from current position in the receive list. Reset to place the receive process in stop state.
0	HP	Hash/Perfect Receive Filtering Mode, read only bit, set to use hash table to filter multicast incoming frames. If CSR6<2> is also set, then the physical addresses are imperfect address filtered too. If CSR6<2> is reset, then physical addresses are perfect address filtered, according to a single physical address as specified in setup frame.

TABLE 5.2.4 TRANSMIT THRESHOLD

CSR6<21>	CSR6<15:14>	CSR6<22>=0 (for 100 Base-TX)	CSR6<22>=1 (Threshold bytes) (for 10 Base-T)
0	00	128	72
0	01	256	96
0	10	512	128
0	11	1024	160
1	XX	(Store and Forward)	

TABLE 5.2.5 DATA PORT SELECTION

CSR14<7>	CSR6<18>	CSR6<22>	CSR6<23>	CSR6<24>	Port
1	0	X	X	1	Nway Auto-negotiation
0	0	1	X	0	10 Base-T
0	1	0	1	X	100 Base-TX

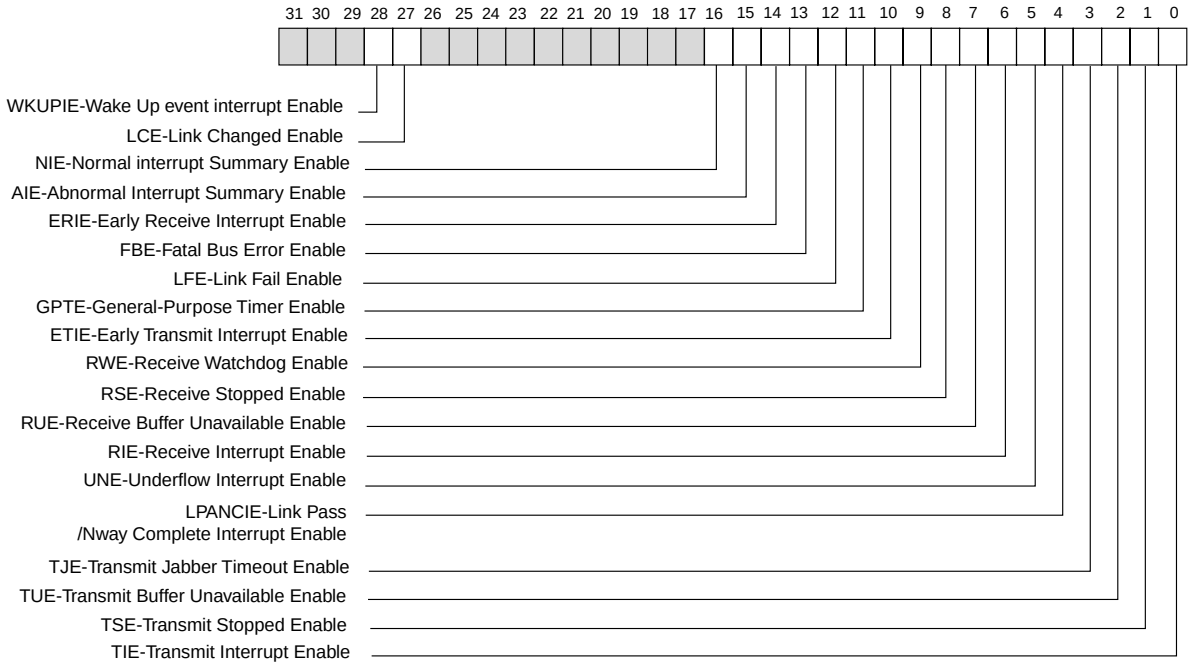
TABLE 5.2.6 LOOPBACK OPERATION MODE

CSR6<11:10>	Operation Mode
00	Normal
01	Internal loopback at FIFO port
11	Internal loopback at the PHY level
10	External loopback at the PMD level

TABLE 5.2.7 FILTERING MODE

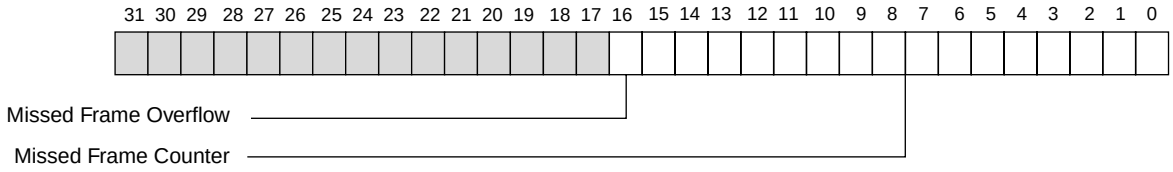
CSR6<7>	CSR6<6>	CSR6<4>	CSR6<2>	CSR6<0>	Filtering Mode
0	0	0	0	0	16 perfect filtering
0	0	0	0	1	512-bit hash + 1 perfect filtering
0	0	0	1	1	512-bit hash for multicast and physical addresses
0	0	1	0	0	Inverse filtering
X	1	0	0	X	Promiscuous
0	1	0	1	1	Promiscuous
1	0	0	0	X	Pass All Multicast
1	0	0	1	1	Pass All Multicast

5.2.7 INTERRUPT MASK REGISTER (CSR7)



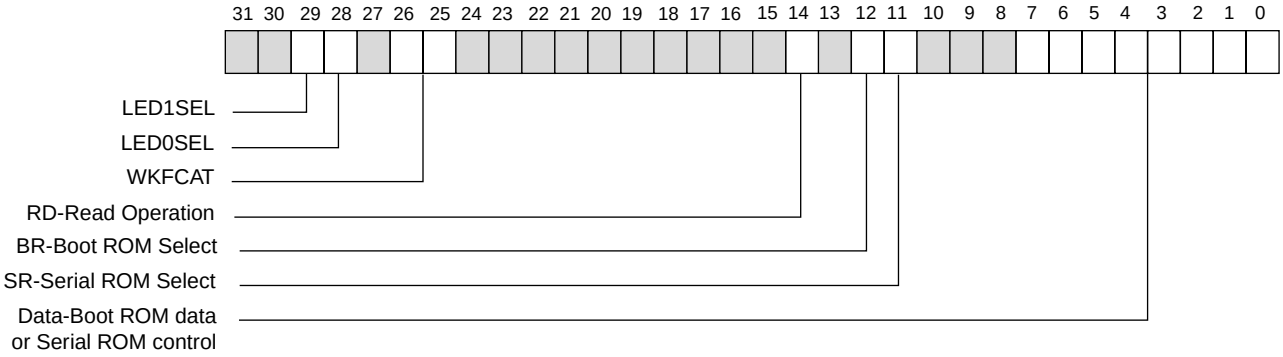
Field	Name	Description
28	WKUPIE	Wake Up Event Interrupt Enable, enables CSR5<28>.
27	LCE	Link Changed Enable, enables CSR5<27>.
16	NIE	Normal Interrupt Summary Enable, set to enable CSR5<0>, CSR5<2>, CSR5<6>.
15	AIE	Abnormal Interrupt Summary enable, set to enbale CSR5<1>, CSR5<3>, CSR5<5>, CSR5<7>, CSR5<8>, CSR5<9>, CSR5<11> and CSR5<13>.
14	ERIE	Early Receive Interrupt Enable
13	FBE	Fatal Bus Error Enable, set together with with CSR7<15> enables CSR5<13>.
12	LFE	Link Fail Interrupt Enable, enables CSR5<12>
11	GPTE	General Purpose Timer Enable, set together with CSr7<15> enables CSR5<11>.
10	ETIE	Early Transmit Interrupt Enable, enables CSR5<10>
9	RWE	Receive Watchdog Timeout Enable, set together with CSR7<15> enables CSR5<9>.
8	RSE	Receive Stopped Enable, set together with CSR7<15> enables CSR5<8>.
7	RUE	Receive Buffer Unavailable Enable, set together with CSR7<15> enables CSR5<7>.
6	RIE	Receive Interrupt Enable, set together with CSR7<16> enables CSR5<6>.
5	UNE	Underflow Interrupt Enable, set together with CSR7<15> enables CSR5<5>.
4	LPANCIE	Link Pass/Autonegotiation Completed Interrupt Enable
3	TJE	Transmit Jabber Timeout Enable, set together with CSR7<15> enables CSR5<3>.
2	TUE	Transmit Buffer Unavailable Enable, set together with CSR7<16> enables CSR5<2>.
1	TSE	Transmit Stop Enable, set together with CSR7<15> enables CSR5<1>.
0	TIE	Transmit Interrupt Enable, set together with CSR7<16> enables CSR5<0>.

5.2.8 MISSED FRAME COUNTER (CSR8)



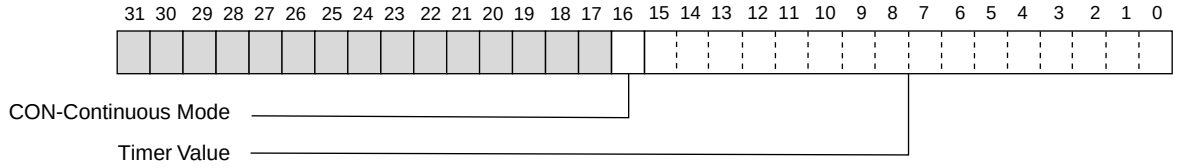
Field	Name	Description
16	MFO	Missed Frame Overflow, set when missed frame counter overflows, reset when CSR8 is read.
15:0	MFC	Missed Frame Counter, indicates the number of frames discarded because no host receive descriptors were available.

5.2.9 NON-VOLATILE MEMORY CONTROL REGISTER (CSR9)



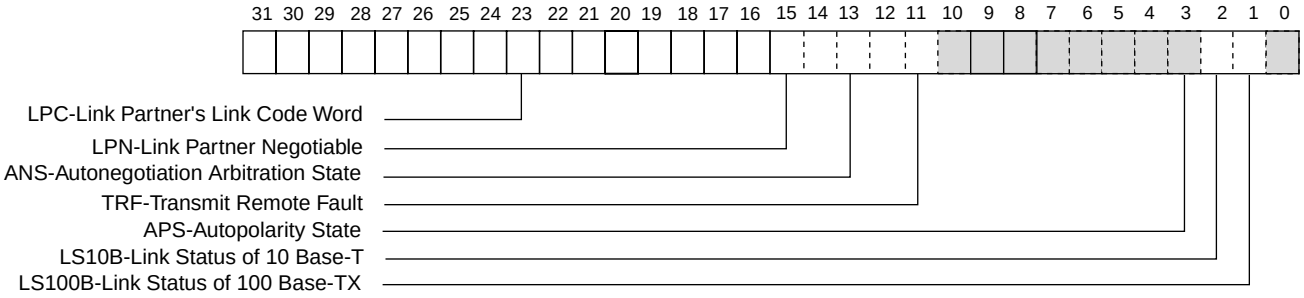
Field	Name	Description
29	LED1SEL	0:Default value. Set LED1 as Good Link LED. 1: Set LED1 as Link/Activity LED.
28	LED0SEL	0:Default value. Set LED0 as Activity LED. 1: Set LED0 as Link Speed (10/100) LED.
14	RD	Boot ROM read operation when boot ROM is selected.
12	BR	Boot ROM Select, set select serial ROM only if CSR9<11>=0.
11	SR	Serial ROM Select, set to select serial ROM for either read or write operation.
7:0	Data	If boot ROM is selected (CSR9<12> is set), this field contains the data to be read from and written to the boot ROM. If serial ROM is selected, CSR9<3:0> are defined as follows: Warning : CSR9<11> and CSR9<12> should be mutually exclusive for correct operations.

5.2.10 GENERAL PURPOSE TIMER (CSR11)



Field	Name	Description
16	CON	When set,the general purpose timer is in continuous operating mode. When reset, the timer is in one-shot mode.
15:0	Timer	Value contains the timer value in a cycle time of 204.8us.

5.2.11 10 BASE-T STATUS Port (CSR12)

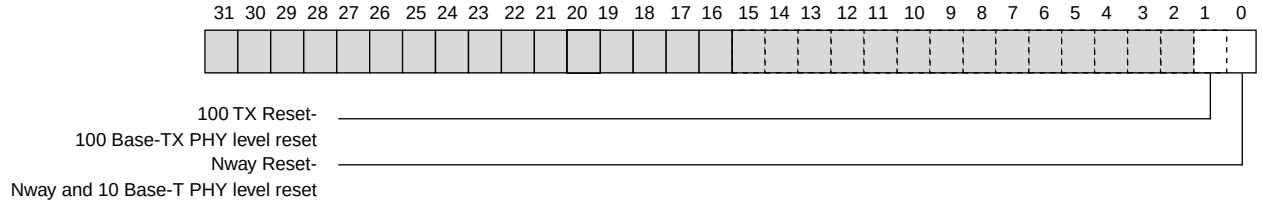


*Software reset has no effect on this register

Field	Name	Decription
31:16	LPC	Link Partner's Link Code Word, where bit 16 is S0 (selector field bit 0) and bit31 is NP (Next Page). Effective only when CSR12<15> is read as a logical 1.
15	LPN	Link Partner Negotiable, set when link partner support NWAY algorithm and CSR14<7> is set.
14:12	ANS	Autonegotiation Arbitration State, arbitration states are defined 000 = Autonegotiation disable 001 = Transmit disable 010 = ability detect 011 = Acknowledge detect 100 = Complete acknowledge detect 101 = FLP link good; autonegotiation complete 110 = Link check When autonegotiation is completed, an ANC interrupt (CSR5<4>) is generated, write 001 into this field can restart the autonegotiation sequence if CSR14<7> is set. Otherwise, these bits should be 0.

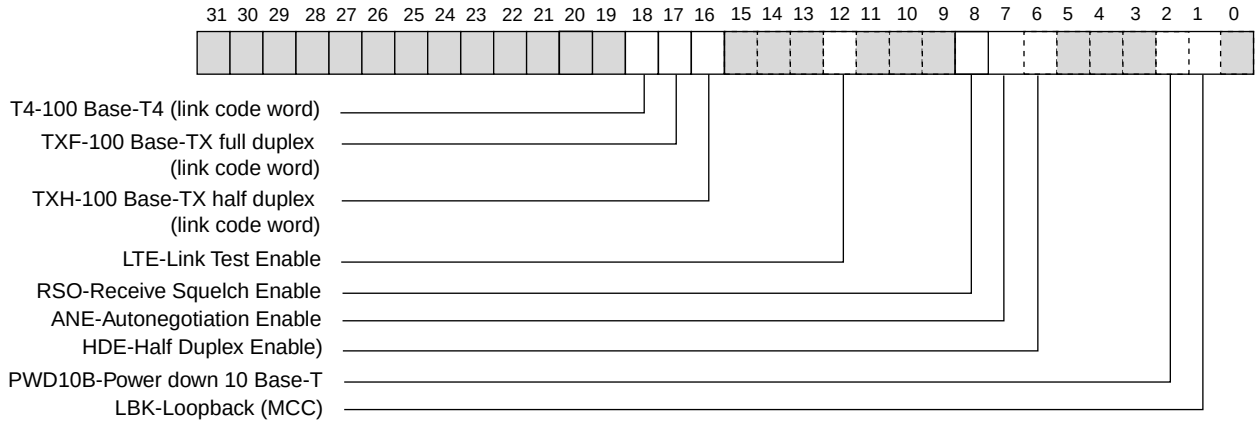
Field	Name	Decription
11	TRF	Transmit Remote Fault
3	APS	Autopolarity State, set when polarity is positive. When reset, the 10Base-T polarity is negative. The received bit stream is inverted by the receiver.
2	LS10B	Set when link status of 10 Base-T port link test fail. Reset when 10 Base-T link test is in pass state.
1	LS100B	Link state of 100 Base-TX, this bit reflects the state of SD pin, effective only when CSR6<23>= 1 (PCS is set). Set to indicate a fail condition .i.e. SD=0.

5.2.12 SIA Reset Register (CSR13)



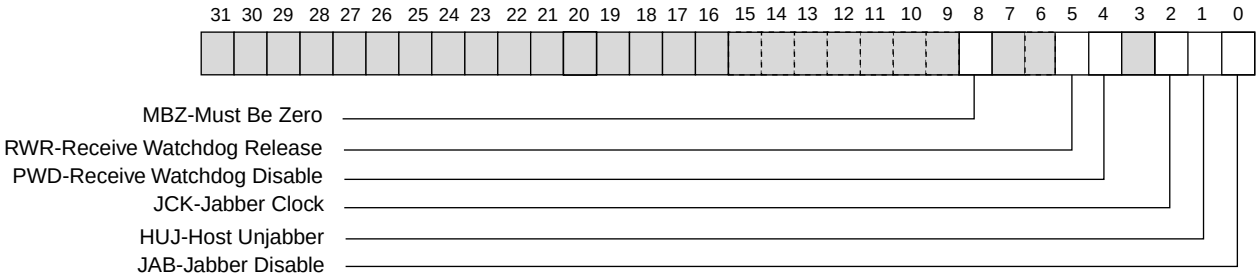
Field	Name	Decription
0	Nway Reset	While writing 0 to this bit, resets the CSR12 & CSR14.
1	100Base-TX Reset	Write a 1 will reset the internal 100 Base-TX PHY module

5.2.13 10 Base-T Control PORT (CSR14)



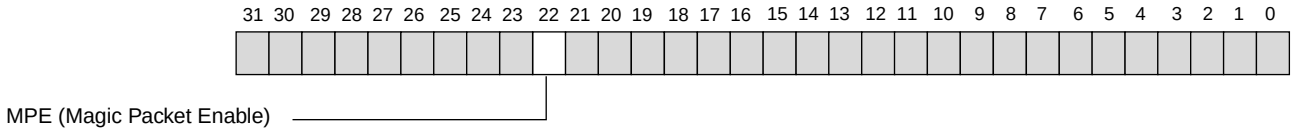
Field	Name	Decription
18	T4	Bit 9 of link code word for T4 mode.
17	TXF	Bit 8 of link code word for 100 Base-TX full duplex mode.
16	TXH	Bit 7 of link code word for 100 Base-TX half duplex mode. Meaningful only when CSR14<7> (ANE) is set.
12	LTE	Link Test Enable, when set the 10 Base-T port link test function is enabled.
8	RSQ	Receive Squelch Enable for 10 Base-T port. Set to enable.
7	ANE	Autonegotiation Enable, .
6	HDE	Half-Duplex Enable, this is the bit 5 of link code word, only meaningful when CSR14<7> is set.
2	PWD10B	Reset to power down 10 Base-T module, this will force both TX and RX port into tri-state and prevent AC current path. Set for normal 10 Base T operation.
1	LBK	Loop back enable for 10 Base-T MCC.

5.2.14 WATCHDOG TIMER (CSR15)



Field	Name	Description
5	RWR	Defines the time interval no carrier from receive watchdog expiration until reenabling the receive channel. When set, the receive watchdog is release 40-48 bit times from the last carrier deassertion. When reset, the receive watchdog is released 16 to 24 bit times from the last carrier deassertion.
4	RWD	When set, the receive watchdog counter is disable. When reset, receive carriers longer than 2560 bytes are guaranted to cause the watchdog counter to time out. Packets shorter than 2048 bytes are guaranted to pass.
2	JCK	When set, transmission is cut off after a range of 2048 bytes to 2560 bytes is transmitted,
		When reset, transmission for the 10 Base-T port is cut off after a range of 26 ms to 33ms. When reset, transmission for the 100 Base-TX port is cut off after a range of 2.6ms to 3.3ms.
1	HUJ	Defines the time interval between transmit jabber expiration until reenabling of the transmit channel. When set, the transmit channel is released immediately after the jabber expiration. When reset, the jabber is released 365ms to 420 ms after jabber expiration for 10 Base-T port. When reset, the jabber is released 36.5ms to 42ms after the jabber exporation for 100 Base-TX port.
0	JBD	Jabber Disable, set to disable transmit jabber function.

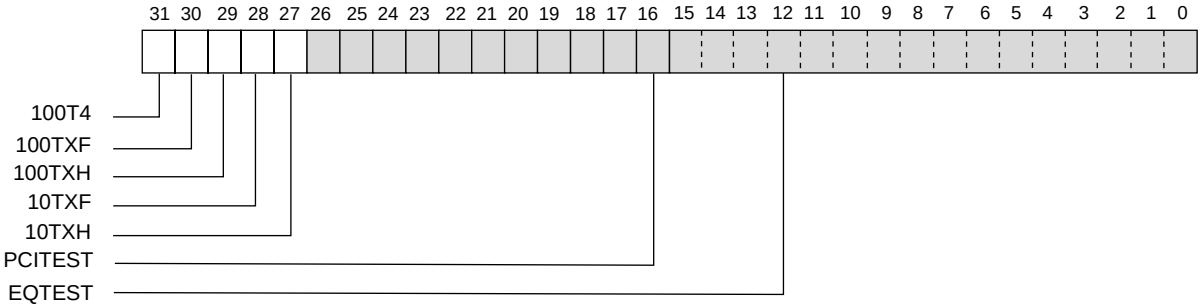
5.2.15 Magic Packet Register (CSR16)



Field	Name	Description
bit 31:23	reserved	
bit 15:0	reserved	
bit 22	MPE	Magic Packet Enable, set to enable Magic Packet Mode

Sleep mode and MPE mode can be used seperately. When Sleep and MPE are both set, the Sleep mode dominate MPE, i.e. no magic packet can be detected since both TX and RX channel are shut off in sleep mode. On the detection of magic packet, the MPI interrupt bit at CSR5<28> can be set to generate a PCI interrupt if CSR7<28> MPIE is set.

5.2.16 Nway Status Register (CSR20)



Field	Name	Description
31	T4	T4 mode is accepted, read only
30	100TXF	100Base-TX full duplex is accepted, read only
29	100TXH	100Base-TX half duplex is accepted, read only
28	10TXF	10Base-T duplex is accepted, read only
27	10TXH	10Base-T half duplex is accepted, read only
16	PCITEST	Default is 0 after Power-on reset. Reserved for PCI bus test purpose, must be set 1 by software for normal operation.
12	EQTEST	Default is 0 after Power-on reset. Reserved for tranceiver equalization test purpose, must be set 1 by software for normal operation.

5.3 Power Management Functions :

MX98715A complies to ACPI Version 1.0, supports D3cold state to generate PMEB. There are basically 3 power saving modes supported, namely Remote Power-On, Remote Wake-Up, and Sleep mode. By default, MX98715A will enable ACPI function with the following registers setup :

PFCS<20> (New Capability)=1
PFCP<7:0> (Capability Pointer)=44h
PPMC<7:0> (Capability ID)=1h

Please refer to PCI configuration registers for more details.

5.3.1 Remote Power-On Mode :

When AC power cord of PC is plugged into the wall outlet, MX98715A will load the network ID from EEPROM and enter itself into Remote Power-On mode automatically. The host and PCI bus has no power at this stage. As soon as a Magic packet addressed to this network adaptor, PMEB will be asserted low to power on the PC.

To set up the Remote Power-On (PRO) mode, as long as a 5.0V standby VDD is connected into the adaptor's isolated VDD and MX98715A will set up itself to detect Magic packet. No registers needed to be programmed. Simply turn off the power switch or plug in the AC power cord of the PC that support RPO and everything else is set automatically.

5.3.2 Remote Wake-Up Mode :

When the PC is still turned on regardless of the status of CPU and system's ststus, a Magic packet can be detected if enabled. As soon as a Magic packet addressed to the network adaptor is detected, both INTA# and PMEB can be asserted low if registers set up as follows :

CSR16<22> (PME)=1 and
PPMCSR<8> (PME_EN)=1
to enable PMEB assertion.

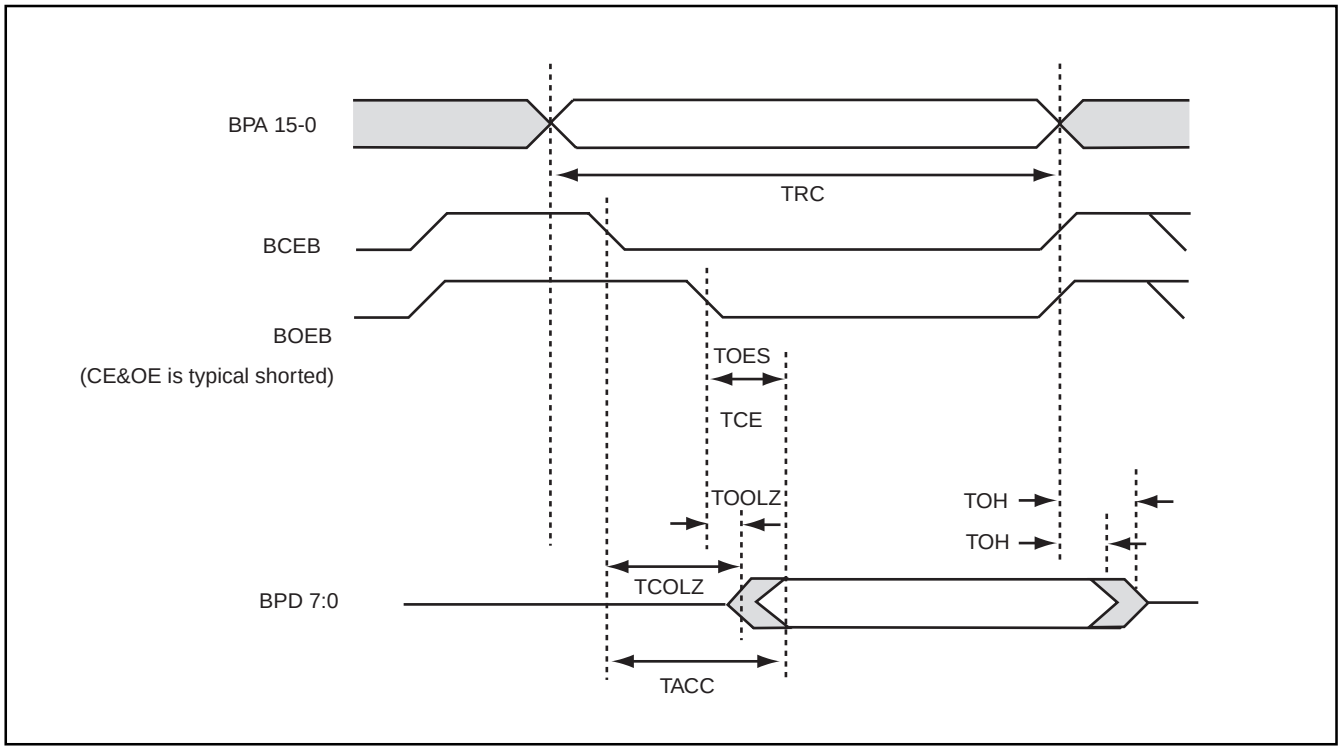
CSR16<22> (PME)=1 and
CSR7<28> (MPIE)=1 to enable INTA# assertion

5.3.3 Sleep Mode :

Set PFDA<31> (Sleep)=1 will enter the chip into a sleep mode where no TX nor RX activities can be processed. Only PCI configuration can be accessed.

6. AC/DC CHARACTERISTICS

6.1 BOOT ROM READ TIMING



6.2 AC CHARACTERISTICS

SYMBOL	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNITS
TRC	Read Cycle	8	-	-	PCI Cycle
TCE	Chip Enable Access Time	-	-	7	PCI Cycle
TACC	Address Access Time	-	-	7	PCI Cycle
TOES	Output Enable Access Time	-	-	7	PCI Cycl
TOH	Output Hold from Address, CEB, or OEB	0	-	-	ns

PCI cycle range:66ns (16MHz)~25ns (40MHz)

6.3 ABSOLUTE OPERATION CONDITION

Supply Voltage (VCC)	-0.5V to +7.0V
DC Input Voltage (Vin)	4.75V to 5.25V
DC Output Voltage (Vout)	-0.5V to VCC + 0.5V
Storage Temperature Range (Tstg)	-55℃ to +150℃
Operating Temperature Range	0℃ to 70℃
Power Dissipation (PD)	750mW (Typ.)
Lead Temp. (TL) (Soldering, 10 sec)	260℃
ESD Rating (Rzap = 1.5k, Czap = 100pF)	1.0kV
Clamp Diode Current	20mA

6.4 DC CHARACTERISTICS

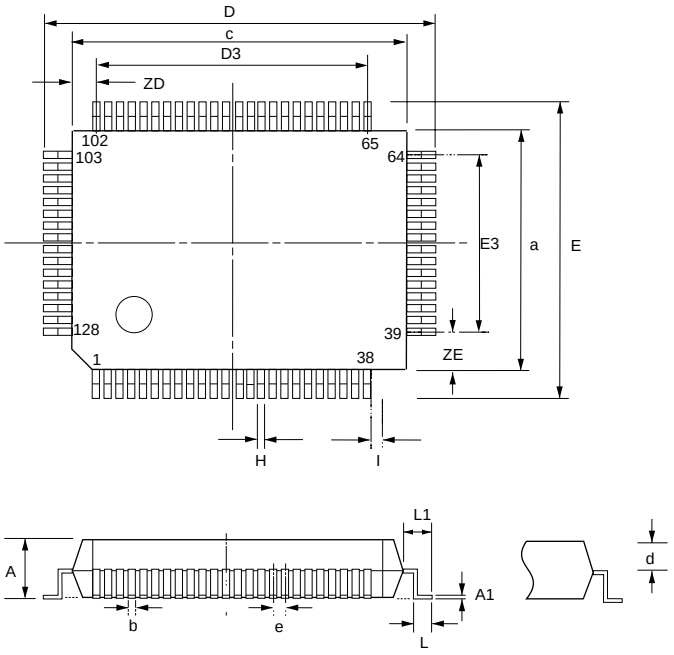
Symbol	Parameter	Conditions	Min	Max	Units
TTL/PCI Input/Output					
Voh	Minimum High Level Output Voltage	Ioh = -3mA	2.4		V
Vol	Maximum Low Level Output Voltage	Iol = +6mA		0.4	V
Vih	Minimum High Level Input Voltage		2.0		V
Vil	Maximum Low Level Input Voltage			0.8	V
Iin	Input Current	Vi = VCC or GND	- 1.0	+ 1.0	uA
Ioz	Minimum TRI-STATE Output Leakage Current	Vout = VCC or GND	-10	+10	uA
LED output Driver					
Vlol	LED turn on Output Voltage	Iol = 16mA		0.4	V
Supply					
Idd	Average Supply Current	CKREF =25MHz PCICLK = 33MHz	130	170	mA
Vdd	Average Supply Voltage		4.75V	5.25V	V

7.0 PACKAGE INFORMATION

128-Pin Plastic Quad Flat Pack

ITEM	MILLIMETERS	INCHES
a	14.00±05	5.512±002
b	.20 [Typ.]	.08 [Typ.]
c	20.00±05	7.87±002
d	1.346	.530
e	.50 [Typ.]	.20 [Typ.]
L1	1.60±1	.63±04
L	.80±1	.31±04
ZE	.75 [Typ.]	.30 [Typ.]
E3	12.50 [Typ.]	4.92 [Typ.]
E	17.20±2	6.77±08
ZD	.75 [Typ.]	.30 [Typ.]
D3	18.50 [Typ.]	7.28 [Typ.]
D	23.20±2	9.13±08
A1	.25±1 min.	.01±04 min.
A	3.40±1 max.	1.34±04 max.
Note	Short Lead	Short Lead

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



REVISION HISTORY

Revision	Destription	Page	Date
1.1	(1) revise PFRV register bit 31-24 to be 2h	P7	SEP/15/1998
	(2) exchange description for PFIT register bit 7-0 and bit 15-8	P9	
	(3) revise ESD rating in Section 6.3 from 1.5KV to 1.0KV	P29	
	(4) add Power Dissipation in Section 6.3 to be 750mW (typ)	P29	
	(5) add Idd value in Section 6.4 to be 130mA to 170mA	P29	
1.2	Change NWAY Status Register	P26	FEB/24/1999

MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-8888
FAX:+886-3-578-8887

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-747-2309
FAX:+65-748-4090

TAIPEI OFFICE:
TEL:+886-3-509-3300
FAX:+886-3-509-2200

MACRONIX AMERICA, INC.

TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com