MX86251

1.Introduction

A graphics subsystem using the MX86251 and 3Dfx Interactive Voodoo Rush™ combines industry leading 3D performance with the proven performance and compatibility of an industry standard 2D Windows accelerator. This union creates an extremely cost effective and uncompromising multimedia solution. The MX86251 provides a PCI system interface and high performance VGA, 2D, and Video features in a low cost 2D chip while the Voodoo Rush™ delivers 3D graphics processing power. The MX86251 connects to Voodoo Rush™ through the high performance 64-bit VR interface. The VR interface supports the render/refresh operation of the 2D/3D engines and the system control of the 3D devices. The MX86251 supports not only the basic Double Buffer Scheme, but also Triple and Quad buffer swap for super smooth animation and 3D stereo glasses applications. The STATUS signal provides 3D status to the PCI host through the MX86251.

The MX86251 is based on proven MX86250 2D/Video window accelerator technology, while adding many enhancements to the base functionality. All processing engines on the chip are running on a faster clock, up to 75 MHz which means 600 MB/sec peak memory bandwidth. Higher bandwidth means higher 2D performance and higher frame rate Video. The Linear Frame Buffer write cycle from the PCI bus is now executed in one clock cycle. That is, the CPU now has much greater write bandwidth into frame buffer memory. The on chip RAMDAC is enhanced to 160 MHz to enable many high resolution video modes. Contrast and Brightness adjustments are added to the Video Processor so that dark MPEG-1 videos will look much better on the screen. ALL these features of the MX86251 combines to make a powerful graphics experience for multimedia.

1.1 Features

Interface to 3Dfx VOODOO RUSH™ 3D graphic chipset

- Provide industry leading price / performance in 2D and Video
- Enable the add-in of advanced 3Dfx Interactive Voodoo Rush™ 3D texture mapping and pixel rendering engines
- 4MB frame buffer enables higher resolution 3D graphics
- Double, Triple and Quad buffer swap
- Optimized LFB PCI write cycles with packing FIFO for most efficient usage of frame buffer bandwidth

Very high bandwidth, up to 600 MB/sec

- Achieves single clock cycle EDO DRAM access in Graphics Co-processor, Video Processor and Display Processor
- Delivers 600 MB/sec bandwidth with -35 EDO DRAM running at 75 MHz
- Provides 400 MB/sec memory bandwidth using lower cost -50 EDO DRAM chips

High Performance 64-bit Graphics Co-processor

- High performance graphics engine with 64 bit wide data path and memory data bus
- Uniformly accelerated graphics operations in all pixel formats: 256 color, High color and True color
- Optimized graphics engine for BitBLTs, rectangle fill, pattern fill, line draw, color expansion, text transfer, and clipping
- Advanced 3 operand BitBLT ALU executes all 256 Raster Operations (ROPs)
- On chip 8x8x32 pattern memory achieves highest throughput in the most common BitBLT in Windows -- the Pattern BLT
- Deep on-chip Source and Destination FIFOs for sustained burst cycles in BitBLTs
- Double buffered Co-processor registers allow concurrent processing with CPU
- Built in hardware cursor
- Arbitrary X-Stride for efficient offscreen memory allocation

Motion Video Codec Acceleration

- Contrast brightness adjustment
- YUV/YCrCb conversion of industry standard YUV 4.2.2 formats
- Video window zoom in both X and Y direction with arbitrary ratio
- Interpolation with Bi-linear filters in both Horizontal and Vertical dimensions
- Color Key supports video overlay
- Video window is double buffered
- Video is always played in True Color

Media Port interface to MPEG decoder chips or Video Capture front-end

- Glueless interface to VMI (Video Module Interface)

connector for
- hardware MPEG-2 decoder using plug-in daughter card
- Glueless interface to Phillips 7110 for live video input
- Interlaced video can be captured either one field only or converted to higher resolution non-interlaced frame
- Built in FIFO and flexible decimator

High speed PCI local bus interface
- Support zero wait state PCI burst cycles for maximum CPU write bandwidth
- Single clock cycle PCI write to frame buffer memory
- level command and data FIFO

Flexible Display Memory configuration
- 1, 2, or 4 MB display memory
- 256K x 4, 256K x 8, and 256K x 16 dual CAS or dual WE DRAM
- Fast-page and EDO

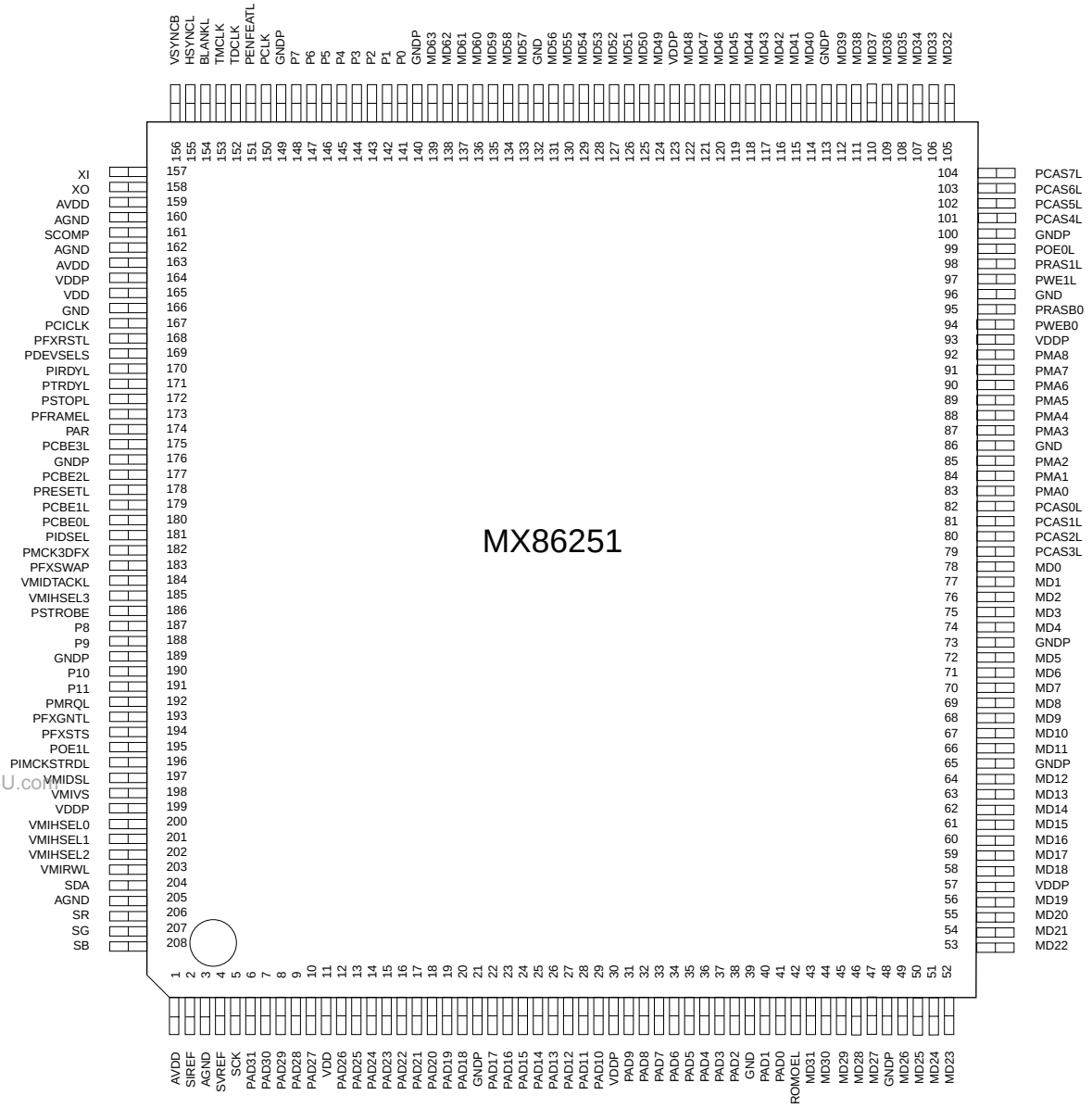
Fully Integrated for lower system cost
- Integrated 24 bit True Color RAMDAC supports 160 MHz pixel rate and 256x18 look-up table with High Color and True color bypass
- Dual integrated clock synthesizers
- VESA Display Data Channel (DDC-1/2AB) protocol support
- Support I^2C channel interface
- General purpose I/O pins

"Green PC" power management
- Support VESA DPMS (Display Power Management) standard
- Built in advanced power management techniques such as internal DAC power down mode and clock idle modes

Complete Hardware compatibility
- Windows 95 Plug and Play compliant
- VGA hardware, register, and BIOS level 100% compatible
- PCI revision 2.1 compatible

MX86251

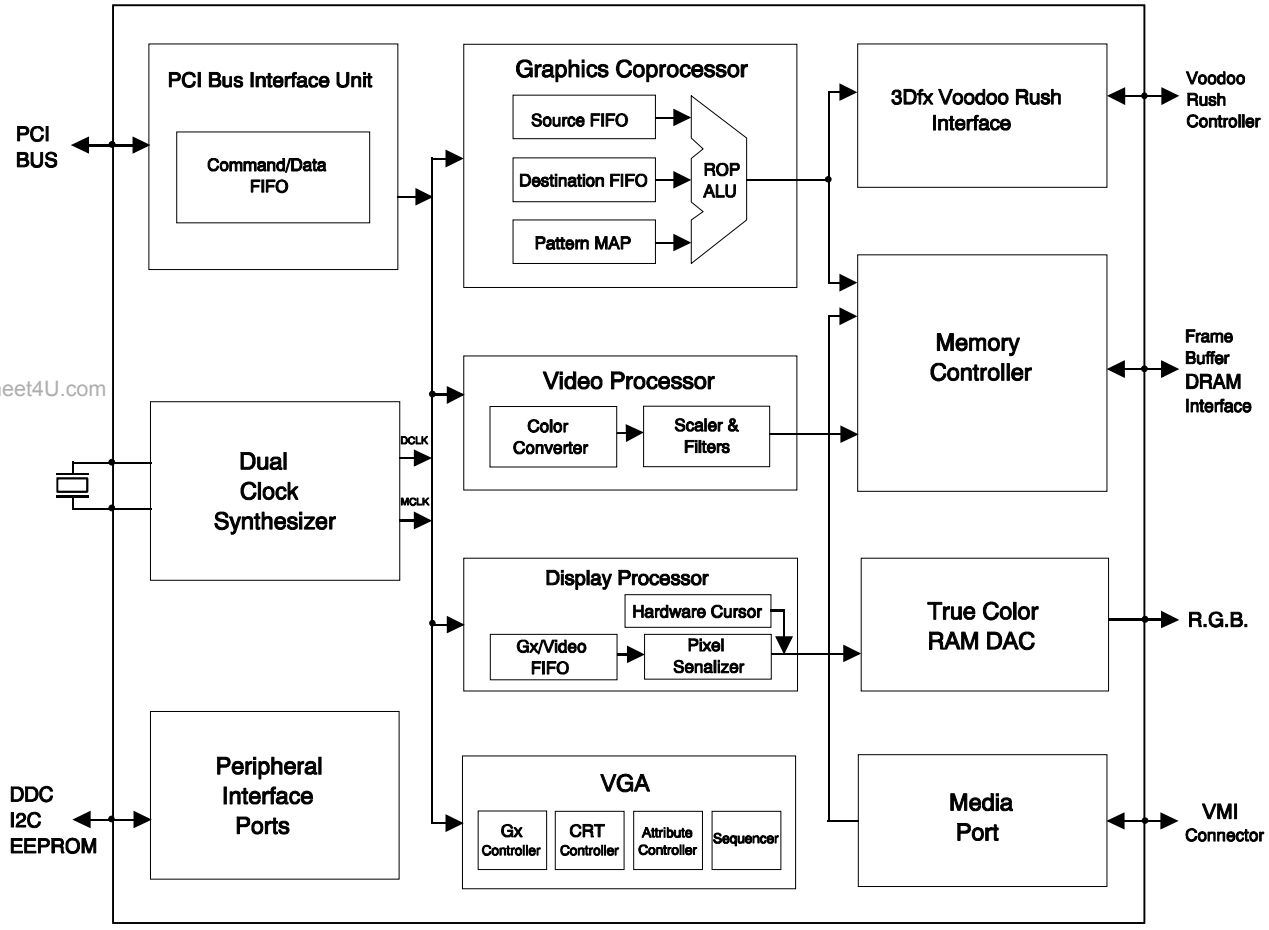
208PIN PQFP PACKAGE



2.Functional Description

The MX86251 is a new generation of fully integrated graphics and video accelerator with the high performance VR interface to 3Dfx's Voodoo Rush chip set to achieve the leading-edge 3D effect. On a single chip, it integrates a 64-bit graphics CoProcessor, a true-color video processor, 160MHz RAMDAC and dual programmable clock synthesizer. The MX86251 not only delivers extreme high performance in 3D/2D graphics acceleration, it also provides very rich functionality for motion video applications. The MX86251 true color video processor allows full screen full motion playback of AVI and MPEG video from software based Codec's such as MPEG, Cinepak and Indeo. For even higher quality MPEG video playback, the MX86251 Media port supports the VMI connector linking to an external MPEG-1 decoder chip. The Media port also provides for playback and capture of live video input from TV tuner or video camera.

2.1 MX86251 chip function block diagram



2.2 64-bit Graphics Co-processor

The MX86251 Graphics Co-processor accelerates common Graphics User Interface drawing functions , including Bitblt, Rectangle Fill, Pattern Fill, Bresenham Line Draw, and Text Transfer. Hardware clipping and hardware cursor further reduce software driver overhead, including Bitblt, Rectangle Fill, Pattern Fill, Bresenham Line Draw, and Text Transfer. Hardware clipping and hardware cursor further reduce software driver overhead to the minimum.

The Graphics Co-processor supports scrardware cursor further rr further reduce software driver overhead to the minimum.

The Graphics Co-processor supports screen widths of 640, 800, 1024, 1152, 1280, 1600 and 2048. Pixel depth can be 8, 16, and 32 bits. The display memory size can be 1,2 or 4 megabytes. All Co-processor drawing operations are programmed with 32 bit registers in a linear address aperture.

Three Operand Bitblt

The Graphics Co-processor executes Bitblt operations between three operands: the Source bitmap, the Destination bitmap, and the Pattern bitmap. There are 256 operations on bitmaps, called Raster Operations (ROP). An ALU with three operand inputs is implemented to execute any of the 256 RO P 's in a single cycle, unlike earlier generation GUI chips which used only two operands and implemented only 16 ROPs. This forced the software driver to decompose those 3-operand bitblt into two or three 2-operand BitBLTs significantly slowing down the drawing process.

Source/Destination FIFOs

The three inputs to the Bitblt ALU are from the Source FIFO, the Destination FIFO and the Pattern Map Buffer. The Source and Destination FIFO are 64 bit wide and 8 levels deep. They allow the fetch cycles for Source and Destination pixels to be run in page mode cycles. By having Destination FIFO, the MX86251 can run Destination read-modify-write operations in page mode reads followed by page mode writes which is substantially faster than the read-modify-write cycles in an EDO-DRAM based system.

Pattern Map Buffer

The most common Bitblt operation in Windows is the PatBlt which means painting a large window background using a brush which is an 8 by 8 pattern bitmap. Many GUI chips store the brush pattern bitmap in offscreen memory. During Patblt, the pattern are fetched repeatedly.

To accelerate Patblt, the MX86251 has on-chip memory to store a full 8 by 8 pattern bitmap. Unlike others which can only store 8-bit pixels, The MX86251 can store pixel maps of 8, 16, and 32 bit pixels. This complete implementation of Pattern Map, enables the MX86251 to execute the Patblts at peak memory bandwidth using a long burst of page mode writes and thus achieving the best drawing performance.

Text / Font drawing acceleration

Drawing text characters or fonts are another very common Windows drawing operation. The fonts are monochrome bitmaps that get expanded into color pixel maps in the Graphics Co-processor. The MX86251 optimizes this process in several ways.

Font bitmaps can be stored in system memory and transferred to the Co-processor for color expansion.The MX86251 provides a screen port to facilitate this memory to screen transfer. The screen port is mapped in a linear address aperture of 64K bytes. The monochrome font pixels are buffered in the Source FIFO so that concurrent operations are enabled for font transfer from system memory and color expansion in the Co-processor. The display driver can also cache font bitmaps in offscreen memory using the so called font-cache scheme. The MX86251 provides direct support of offscreen packed monochrome bitmap to color map expansion. This operation greatly accelerates the performance of font cache.

Windows 95 Direct Draw acceleration

Windows 95 Direct Draw is aimed to turn the Windows GUI environment into a Game platform with high speed sprite animation. The key to sprite animation is Transparent Blt. The MX86251 implements a flexible Color Key mechanism to enable high speed Transparent Blt. A Transparent Blt writes to screen a source bitmap, that is, a sprite, which is in an irregular shape such as a cartoon figure. The background pixels which should not be overwritten are coded in the special Key color. The Color Com-

pare function block in the Graphics Co-processor checks each pixel against the Key color. If a match is found, the pixel is not written, preserving the background around the sprite. Thus, an irregular shape is BLTed using a fast rectangle draw.

In the MX86251, the Color Key can be in the Source or the Destination bitmap. Transparent Blt uses Source Color Key. The Destination Color Key can be used to protect screen areas. A mask register is defined to allow the key color be a range of color values instead of a single value.

2.3 Memory Controller

The MX86251 Memory Controller module interfaces to the frame buffer DRAM chips which can operate in either fast page mode, or Extended Data Out (EDO) mode. The frame buffer size can be 1, 2, or 4 Megabytes. Industry standard 256K by 4, by 8, or by 16 DRAM chips are supported. The Memory Controller performs the page mode cycle in either 2 clock cycle or 1 clock cycle, depending on the DRAM types being used. The highest bandwidth is delivered using -50 EDO DRAM with 20 ns page cycle time and a 50 MHz memory clock, yielding a 400MB peak bandwidth. The MX86251 is capable of even higher Memory clock speed. As faster EDO DRAM (-35 with 15ns page mode cycle time) enters volume production, the MX86251 will deliver 533 MB/sec bandwidth which is comparable to premium priced DRAMs such as 66 Mhz SGRAM / SDRAM, or RAMBUS RDRAM.

The center of the Memory Controller is an intricate arbiter which receives memory access requests from the Graphics Co-processor for Bitblt cycles, the Display controller for screen fetch, the Video Processor for video playback, the PCI Bus interface for CPU access, the Hardware Cursor for cursor bitmap fetch, and the DRAM refresh cycle request. The arbiter allocates memory cycles according to priority. For example, the Display Processor has higher priority than the Graphics Co-processor.

A 32-level 64-bit FIFO is implemented to buffer the pixels fetched from display memory for the screen refresh and video playback. The FIFO entries can be flexibly allocated between three different processors: Graphics, Video line 1 and Video line 2. This flexibility works to optimize performance across various screen resolutions and video playback operations.

The Memory Controller generates all DRAM cycles. Its logic is carefully designed to optimize DRAM cycle timing parameters. For example, the DRAM entry cycle which is the time from RAS precharge to the end of first CAS cycle is optimized to the minimum of 4 clock cycles, versus the commonly seen 5 or 6 clock cycles in other GUI chips. Another example is that of EDO DRAM read cycle. The MX86251 eliminates the one extra clock cycle at the end of page mode cycles.

Unified Memory Architecture

The MX86251 fully supports the VESA Unified Memory Architecture (VUMA) standard. The Memory Controller implements the VUMA standard RQ/GNT state machine which supports two request priorities. Bus parking is provided to minimize bus switch overhead. DRAM read and write operations in UMA mode can have programmable number of wait states to accommodate the wide variation in main system DRAM module access speed. In addition, the DRAM interface drivers have programmable drive strength to work with wide range of DRAM interface loading on system motherboards.

2.4 PCI Bus Interface Unit

The MX86251 Bus Interface Unit (BIU) implements a glueless connection to industry standard PCI local bus which is compliant with Windows 95 Plug'n'Play requirement.

PCI bus speed can be up to 33 MHz. For peak transfer rate between host CPU and the MX86251, zero wait state PCI burst cycles are supported. The resultant 133 MB per second bandwidth greatly enhances the performance level of Graphics intensive software such as Windows GUI and AutoCAD that do lots of direct accesses to video memory.

The BIU has an 8 level command and data FIFOs to buffer host transfers and enables concurrent operations of the host CPU, the graphics engine and the Video Processor. The PCI Rev. 2.1 disconnect and retry protocol is fully supported eliminating the delays of host CPU polling for BIU FIFO status.

2.5 Video Processor

The MX86251 Video Processor accelerates the playback of AVI or MPEG video decoded by a software Codec such as Cinepak, Indeo, or MPEG-1. Profiling of the task load

showed that about one third time each is spent in decompression, color conversion and pixel transfer to screen. The Video Processor implements the color conversion and pixel transfer in hardware, leaving only the decompression task to CPU. Thus, the video play frame rate which used to be 8 to 10 fps from software Codec is approximately tripled to the full motion rate of 30 fps by the MX86251.

Video clips are typically in QCIF or CIF format which are relatively small when viewed on the SVGA display. It is very desirable to scale up the video window to at least 640x480 or even full screen at 1024x768. The scale up can be just duplicating the pixels (Zoom) which produces blocky pictures. In high end broadcast quality video processing, a smoothing filter is typically used to remove the blocky artifacts. The MX86251 Video Processor implements both Scaler and smoothing Filters so that full motion video can play in full screen without degradation.

Horizontal and Vertical interpolation

The Video Processor performs the filtering in both Horizontal and Vertical dimension. While most first generation Video chips only have one horizontal filter. The MX86251 provides three filters to fit the particular needs of different video decoders. The vertical interpolation filter further enhances the appearance of video images by eliminating staircasing diagonal lines and illegible text commonly seen in video played by 1st generation video chips.

Pixel formats

The Video Processor supports many pixel formats. The Video pixels can be in RGB formats such as KRGB-1.5.5.5, RGB-5.6.5, XRGB-8.8.8. The KRGB has 1 key bit which works as a color key. More likely, the video pixels are in YUV format such as YUV-16 (4:2:2), YUV-8 (2:1:1), or YCbCr-16 (4:2:2). The YUV format pixel has a range of value from 0 to 255, while the YCbCr format pixel values are in the range of 16 to 240.

Direct Draw feature support

The Video Processor fully support Windows 95 Direct Draw with features such as Chroma Key, Page flipping and Blending.

The Chroma key is designed for Blue Screen video which is very useful in games where video sprites are employed. The new Indeo 4.0 transparency feature also makes heavy use of the Chroma key mechanism.

The video window can be double-buffered to avoid tearing. The Video Processor executes page flipping in synchronization with Vertical blanking. A status bit is provided to inform software of the completion of page flipping.

Edge Blending

The MX86251 "edge blending" is an unique new feature. It is implemented to enhance the edge quality of Chroma keyed video sprites. DirectDraw does provide API calls which support the use of edge blending.

The Blending feature provides 16 levels of alpha mixing of the video and graphics window. This can be used to do a very smooth dissolve or fade which are popular visual effects often used in edutainment titles.

2.6 Media Port

The Media Port is a direct interface to MPEG and Video decoders. A MX86251 based graphics card can deliver very extensive multimedia functionality by fully utilizing the Media Port. An MPEG-1 decoder chip can be incorporated on board to deliver higher quality MPEG video. Video Front end such as the Philips SA7110 can be built in for Video Capture and live TV window.

The Media Port can accept pixel data streams from either the pixel port or the PCI bus interface. The pixel data stream pass through a FIFO before it gets written into the frame buffer. A flexible decimation unit can be used to reduce the input video frame size – usually required for capturing camera input.

The video window for Media Port video stream is also double buffered for anti-tearing. Interlaced video input can be captured in two ways: one field only, or converted to non-interlaced frame.

VMI connector

To support a wide variety of Video and MPEG decoders, the Media Port supports the VMI (Video Module Inter-

face) standard. The VMI specifies a 40-pin connector which, in addition to the VGA connector, contain an 8-bit YUV pixel bus and an 8-bit Host data bus. The pixel bus transfers 8-bit packed format YUV pixels from Video decoders to the Media port. The host bus transfers compressed MPEG data stream from the Media Port to the MPEG decoder chip. A small daughter card carrying the decoder chip plugs into the 40 and 26 pin connectors.
To support the Philips 7110 chip 16-bit YUV pixel format. the MX86251 Media Port has a special mode where the VMI host bus pins are used for the upper 8 bits of YUV pixels.

2.7 True Color RAMDAC

The MX86251 internal 24 bit RAMDAC provides three 256-entry 6-bit word color look-up table (LUT) RAMs feeding three 8-bit DACs for 8-bit per pixel modes. A clock doubled mode is also provided. A 24 bit LUT bypass is used in High Color (15/16 bits/pixel) and True Color (24 bits/pixel) modes.

The RAMDAC works at pixel clock rate up to 160 MHz. Many high resolution display modes are possible at this high pixel clock rate. For example, with a 2 MB card, the following video mode provides flicker free displays,

1280x1024, 256 color, @80 Hz
1024x768, 64K color, @120 Hz
800x600, 16M color, @120 Hz

2.8 Dual Clock Synthesizers

The MX86251 contains two phase locked loop (PLL) frequency synthesizers. They generate the dot clock (DCLK) for display logic and memory clock (MCLK) for memory controller and graphics engine.

Each PLL scales the input reference frequency to a programmed clock frequency. The reference frequency comes from either the crystal oscillator across the XIN and Xout pin or from a clock input from XIN pin.

The PLL generate its output clock frequency based on two programmed values, the M and N value, and according to the following formula :

$$f_{OUT} = f_{REF} * (M+2) / (N+2) * 2^R$$

where R is the 2 bit scale value.

2.9 Peripheral Interface ports

The MX86251 has interface ports designed to support the VESA DDC monitor interface, the I^2C channel, and serial EEPROM.

VESA DDC standard

The VESA DDC (Display Data Channel) standard specifies a two pin serial channel between the display monitor and the graphics controller. The display monitor sends its capability and configuration datum to the graphics controller chip for the display driver to set up video display mode accordingly. Windows 95 Plug'n'Play interface for display monitors is based on the DDC standard. The MX86251 provides fully compliant implementation of the DDC using the DD0 and DD1 pin.

I^2C and EEPROM support

The I^2C channel is also a two pin serial bus as defined by Philips. Many video components such as the SA7110 video decoder relies on the I^2C channel. The MX86251 provides the SCK and SDA pin for interface to I^2C channel.

Some graphics cards are designed to store certain card configuration or setup information in non-volatile memory storage. The MX86251 can support such a card using serial EEPROM. The DD0 and DD1 pin can be programmed to form an interface to serial EEPROM chips.

2.10 Power-on Reset Strapping

There are 18 pins, MD[17:0] reserved for strapping. These MD pins have internal pull-downs.

PFXSWAP, used for 3DFX existence detection, however, has internal pull-up. If 3DFX is connected, it will drive PFXSWAP low during reset time. Otherwise, PFXSWAP will be set to 1 by the internal pull-up.

The function of each power-on strap pin can also be done through I/O programming. They are defined in registers 3?5/28, 31, and 3FH.

MD5: Reserved

MD6: DIFFIDEN. Bit 3 of register 3?5/3FH.
0--PCI bus device ID is read as "8626"
1--If 3DFX is detected, PCI device ID is read as "8627" Otherwise read as"8626".

MD7: PUMA. Bit 0 of register 3?5/28H.
0--PUMA off (default 250MD)
1--PUMA on.
Issue request for MD bus from 3DFX to execute ROM cycle. PUMA on/off also can be programmed by software at 3D4/28 bit 0.

MD[11:10]:Reserved

MD12: EXTMCLK
0--Use internal MCLK
1--Use external MCLK

MD13: Reserved

MD[15:14]: Reserved.

MD20: DEBUGMD. Bit 0 of register 3?5/31H.
0--Disable debug mode.
1--Enable debug mode.

PFXSWAP: EN3DFX. Bit 2 of register 3?5/3FH
0--3DFX connected
1--3DFX disconnected

2.11 Pin Description

PCI Bus Interface Pins:

Pin Name	Pin No.	Type	Description
PRESET#	178	I	This input is PCI bus RESET#, it is an active low signal used to initialize the GUI to a known state. The trailing edge of this input loads the power on strapping inputs through MD0 to MD17 and PFXSWAP.
PCICLK	167	I	This input is the PCI bus clock. It is an 1X clock of 33MHz.
FRAME#	173	I	This input is FRAME#, it is low to indicate the GUI that a valid address is present on the PCI address bus and a New bus cycle or Burst bus cycles are starting. When sampling this signal low, GUI would latch the address and bus commands.
IRDY#	170	I	This input is Initiator RDY#, it is generated from an PCI Bus Master. When it is low, IRDYB indicates that the Initiator is able to complete the current bus trans action if and only if the TRDY# is also low.
TRDY#	171	STO	This output is Target RDY#, it is generated by GUI if the current bus cycle belongs to the GUI. When it is low, TRDY# indicates that the GUI is able to complete the current bus transaction which already targeted onto it if and only if the IRDY# is also low. It remains low until this current cycle ends,then goes into high for one PCI clock cycle, after that then goes into tri-state.
DEVSEL#	169	STO	This output is DEVSEL#. When driven low, it indicates that GUI will respond to the current cycle. It remains low until this current cycle ends, then goes into high for one PCI clock cycle, after that then goes into tri-state.
STOP#	172	STO	This output is STOP#. When driven low, it indicates that GUI will request the current bus master to stop the current bus transfer. There are two configurations about this signal. One is called disconnect. Under this configuration, GUI will complete the current transaction as the last one. In this case, STOP# will be active at the same time that TRDY# is active. The other configuration is called retry. In this case, GUI just request the bus master to terminate the current cycle and retry again. TRDY# will not be generated in this cycle. Once asserted, it remains low until this current cycle ends then goes into high for one PCI clock cycle, after that then goes into tri-state.
PAR	174	TO	This output is PAR. It is only driven during PCI bus master doing read accesses from GUI. When driven, it will provide an even parity across the AD[31:0], and C/BE#[3:0]. This signal is an tri-state output.

PCI Bus Interface Pins:(Continued)

Pin Name	Pin No.	Type	Description
INTR#	168	TO	This output is INTA#. It is and interrupt request signal to system interrupt controller. This signal always hard wired to the PCI bus INTA# signal pin. It is an open drained output. This pin is typically unused in display subsystem design, but may be connected to IRQ9 via PCI configuration register.
IDSEL	181	I	This input is IDSEL. It is used as an Initialization Device Select during PCI bus Auto-configuration cycles. When high, it indicates that GUI is now selected as a target for PCI bus configuration cycles.
CBE0#	180	I	This multiplexed input is part of a PCI bus Command's definition or a Byte Enable for byte lane 0. During address phase of a PCI bus transaction, it defines the Command. During data phase of a PCI bus transaction, it defines if byte lane 0 is engaged in the transfer or not.
CBE1#	179	I	This is bit 1 of bus command and byte enable.
CBE2#	177	I	This is bit 2 of bus command and byte enable.
CBE3#	175	I	This is bit 3 of bus command and byte enable. The PCI bus Commands supported are listed below: C\BE[3:0]# PCI bus Command Type 0000 (Interrupt Acknowledge) 0001 (Special Cycle) 0010 I/O Read 0011 I/O Write 0100 reserved 0101 reserved 0110 Memory Read 0111 Memory Write 1000 reserved 1001 reserved 1010 Configuration Read 1010 Configuration Write 1100 Memory Read Multiple 1101 (Dual Address Cycle) 1110 Memory Read Line 1111 Memory Write and Invalidate

PCI Bus Interface Pins:(Continued)

Pin Name	Pin No.	Type	Description
AD0	41	I/O	AD[31:0] is the multiplexed Address and Data bus for PCI, which 32-bit wide.
AD1	40		
AD2	38		
AD3	37		
AD4	36		
AD5	35		
AD6	34		
AD7	33		
AD8	32		
AD9	31		
AD10	29		
AD11	28		
AD12	27		
AD13	26		
AD14	25		
AD15	24		
AD16	23		
AD17	22		
AD18	20		
AD19	19		
AD20	18		
AD21	17		
AD22	16		
AD23	15		
AD24	14		
AD25	13		
AD26	12		
AD27	10		
AD28	9		
AD29	8		
AD30	7		
AD31	6		

DRAM Interface Pins:

Pin Name	Pin No.	Type	Description
RAS0#	95	TO	This output is RAS0#. It is configured in two ways. When 3DFX is not connected, it is the RAS address strobe for bank 0, i.e. the first 2MB of 4MB frame buffer memory. Dual CAS or dual WE of fast page or EDO DRAM can be supported. When 3DFX is connected, it is the RAS address strobe for the whole 4MB frame buffer. Only dual CAS EDO DRAM is supported. Memory access are done through PUMA interface. This output will be tristated if GUI is not granted to access the memory bus.
RAS1#	98	TO	This output is RAS1#. It is configured in two ways. When 3DFX is not connected, it is the RAS address strobe for bank 1, i.e. the second 2MB of 4MB frame buffer memory. When 3DFX is connected, it is the RAS address strobe for the 3DFX MMIO and texture memory space, which occupies the upper 4MB above the 4MB frame buffer memory. Through PUMA interface, this output will be tristated if GUI is not granted to access the memory bus. Memory refresh cycle of this bank is not generated I this case. The RAS/WE/OE connecctions for bank control can be outlined below: When 3DFX is not connected:

Content	Memory Space	RAS#	WE#	OE#
Frame Buffer	0MB - 2MB	RAS0#	WE0#	OE0#
Frame Buffer	2MB - 4MB	RAS1#	WE1#	OE0#

When 3DFX is connected:

Content	Memory Space	RAS#	WE#	OE#
Frame Buffer	0MB - 2MB	RAS0#	WE0#	OE0#
Frame Buffer	2MB - 4MB	RAS0#	WE1#	OE1#
3DFX MMIO	4MB - 6MB	RAS1#	WE0#	OE0#
3DFX texture	6MB - 8MB	RAS1#	WE1#	OE1#

CAS0#	82	TO	For dual CAS DRAM type configuration, this output is CAS0#. It is the CAS address strobe of byte lane 0. For dual WE DRAM type configuration, this output is WE0#, it is the WE# control signal of byte lane 0. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.

DRAM Interface Pins: (Continued)

Pin Name	Pin No.	Type	Description
CAS1#	81	TO	For dual CAS DRAM type configuration, this output is CAS1#. It is the CAS address strobe of byte lane 1. For dual WE DRAM type configuration, this output is WE1#, it is the WE# control signal of byte lane 1. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.
CAS2#	80	TO	For dual CAS DRAM type configuration, this output is CAS2#. It is the CAS address strobe of byte lane 2. For dual WE DRAM type configuration, this output is WE2#, it is the WE# control signal of byte lane 2. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.
CAS3#	79	TO	For dual CAS DRAM type configuration, this output is CAS3#. It is the CAS address strobe of byte lane 3. For dual WE DRAM type configuration, this output is WE3#, it is the WE# control signal of byte lane 3. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.
CAS4#	101	TO	For dual CAS DRAM type configuration, this output is CAS4#. It is the CAS address strobe of byte lane 4. For dual WE DRAM type configuration, this output is WE4#, it is the WE# control signal of byte lane 4. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.
CAS5#	102	TO	For dual CAS DRAM type configuration, this output is CAS5#. It is the CAS address strobe of byte lane 5. For dual WE DRAM type configuration, this output is WE5#, it is the WE# control signal of byte lane 5. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.
CAS6#	103	TO	For dual CAS DRAM type configuration, this output is CAS6#. It is the CAS address strobe of byte lane 6. For dual WE DRAM type configuration, this output is WE6#, it is the WE# control signal of byte lane 6. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.

DRAM Interface Pins: (Continued)

Pin Name	Pin No.	Type	Description
CAS7#	104	TO	For dual CAS DRAM type configuration, this output is CAS7#. It is the CAS address strobe of byte lane 7. For dual WE DRAM type configuration, this output is WE7#, it is the WE# control signal of byte lane 7. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.
WE0#	94	TO	For dual CAS DRAM type configuration, this output is WE0#. It is the WE# control signal of bank 0. For dual WE DRAM type configuration, this output is CAS0#, it is the CAS address strobe of bank 0. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.
WE1#	97	TO	For dual CAS DRAM type configuration, this output is WE1#. It is the WE# control signal of bank 1. For dual WE DRAM type configuration, this output is CAS1#, it is the CAS address strobe of bank 1. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus. If GUI is granted, this has the above function when MA9OUTSE is 1. If MA9OUTSE is 0, it is the MA9, which is necessary for asymmetrical DRAM.
OE#	99	TO	This output is OE#. It is the OE# control signal for both banks of frame buffer memory when 3DFX is not connected. It controls access of the lower 2MB of frame buffer or 3DFX MMIO otherwise. In PUMA interface, this output will be tristated if GUI is not granted to access the memory bus.
MA0	83	TO	The outputs MA[8:0] is the DRAM memory address bus for both banks.
MA1	84		It is used to pass the RAS address and CAS address to DRAMs.
MA2	85		In PUMA interface, these outputs will be tristated if GUI is not granted to access
MA3	87		the memory bus.
MA4	88		
MA5	89		
MA6	90		
MA7	91		
MA8	92		

DRAM Interface Pins: (Continued)

Pin Name	Pin No.	Type	Description
MD0	78	I/O	MD[7:0] is the DRAM data bus of memory plane 0 of bank 0 or bank 1.
MD1	77		In BIOS ROM accesses, these are the data inputs[7:0] of external ROM.
MD2	76		They are also served as power-on strapping inputs.
MD3	75		
MD4	74		
MD5	72		
MD6	71		
MD7	70		
MD8	69	I/O	MD[15:8] is the DRAM data bus of memory plane 1 of bank 0 or bank 1.
MD9	68		They are also served as power-on strapping inputs.
MD10	67		
MD11	66		
MD12	64		
MD13	63		
MD14	62		
MD15	61		
MD16	60	I/O	MD[23:16] is the DRAM data bus of memory plane 2 of bank 0 or bank 1.
MD17	59		MD[17:16] are also used as power-on strapping inputs.
MD18	58		
MD19	56		
MD20	55		
MD21	54		
MD22	53		
MD23	52		
MD24	51	I/O	MD[31:24] is the DRAM data bus of memory plane 3 of bank 0 or bank 1.In
MD25	50		BIOS ROM accesses, MD[31:16] are the address outputs[15:0] for external ROM.
MD26	49		
MD27	47		
MD28	46		
MD29	45		
MD30	44		
MD31	43		

DRAM Interface Pins: (Continued)

Pin Name	Pin No.	Type	Description
MD32	105	I/O	MD[39:32] is the DRAM data bus of memory plane 4 of bank 0 or bank 1.
MD33	106		
MD34	107		
MD35	108		
MD36	109		
MD37	110		
MD38	111		
MD39	112		
MD40	114	I/O	MD[47:40] is the DRAM data bus of memory plane 5 of bank 0 or bank 1.
MD41	115		
MD42	116		
MD43	117		
MD44	118		
MD45	119		
MD46	120		
MD47	121		
MD48	122	I/O	MD[55:48] is the DRAM data bus of memory plane 6 of bank 0 or bank 1.
MD49	124		
MD50	125		
MD51	126		
MD52	127		
MD53	128		
MD54	129		
MD55	130		
MD56	131	I/O	MD[63:56] is the DRAM data bus of memory plane 7 of bank 0 or bank 1.
MD57	133		
MD58	134		
MD59	135		
MD60	136		
MD61	137		
MD62	138		
MD63	139		

UMA Interface Pins:

Pin Name	Pin No.	Type	Description
SMURQ#	182	O	This is the MREQ# signal for VESA UMA interface. GUI uses this signal to request memory accesses on UMA.
SMGNT#	183	I	This is the MGNT# signal from VESA UMA interface. GUI will drive DRAM interface signals when this signal is active in UMA configuration.

ROM BIOS Interface Pins:

Pin Name	Pin No.	Type	Description
ROMOE#	42	O	This output is ROMOE#. It may be connected to either one or both of the BIOS ROM chip select and output enable pins directly.

Internal VCG Related Interface Pins:

Pin Name	Pin No.	Type	Description
XI	157	I	This input is used as a Reference Frequency Input for internally imple mented oscillator. An external crystal or oscillator of 14.318Mhz may be used. If an external crystal is used, it must be connected between XIN and XOUT. If an external oscillator is used, it must connect to XIN. In this case, the XOUT must be left open.
XO	158	O	This is used as a Reference Frequency output for internally implemented oscillator. If an external crystal is used, it must be connected between XIN and XOUT. If an external oscillator is used, the XOUT must be left open.

Internal RAMDAC Related Interface Pins:

Pin Name	Pin No.	Type	Description
SVREF	4	I	This pin is the Voltage Reference of 1.2V for internal DAC and Monitor Sence logic. It must be connected with a 0.1u capacitor to AVCC of RAMDAC.
SCOMP	161	I	This pin is the Compensation input for internal DAC. It must be connected with a 0.1u capacitor to AVCC of RAMDAC.
SIREF	2	I	This pin is the Current Reference.
SR	206	O	This pin is the analog output of the pixel color Red component to monitor. It has a voltage level of 0.0V(blank) to 0.7V(full scale) when terminated with 75 ohm double loads.
SG	207	O	This pin is the analog output of the pixel color Green component to monitor. It has a voltage level of 0.0V(blank) to 0.7V(full scale) when terminated with 75 ohm double loads.
SB	208	O	This pin is the analog output of the pixel color Blue component to monitor. It has a voltage level of 0.0V(blank) to 0.7V(full scale) when terminated with 75 ohm double loads.

3Dfx Related Interface Pins:

Pin Name	Pin No.	Type	Description
PRXRST#	168	O	This is the hardware reset signal for 3CFX interface. It is connected directly to HRESET# input of 3DFX reset will be reflected on this pin. Software reset pin SRESET# of 3DFX can be tighten to VDD.
PMCK3DFX	182	O	This is the PUMA clock for 3DFX interface. GUI sends this signal to the input clock pin of 3DFX.
PFXSWAP	183	I	This is the SWAP request from 3DFX. GUI is notified by it to swap CRT or VP double buffers. It is also used to detect 3DFX's existence during power-on reset. When receiving low, it means 3DFX is connected. Otherwise, 3DFX is not connected.
PMRQ#	192	IO	This is a multi-function pin. If VMI is used, it is used as bit 4 of the host data bus, which is bidirectional. It is an output pin for pixel data 12 (p12) if PIXTEST is on. Otherwise, it's used as an output pin of the PUMA request for 3DFX interface. GUI uses this signal to request memory accesses through PUMA.
PFXGNT#	193	IO	This is a multi-function pin. If VMI is used, it is bit 5 of the host data bus. It is an output pin for pixel data 13 (P13) if PIXTEST is on. Otherwise, it's used as an input pin of the PUMA grant for 3DFX interface. GUI will drive DRAM interface signals when this signal is active.
PFXSTS	194	IO	This is a multi-function pin. If VMI is used, it is bit 6 of the host data bus. It is an output pin for pixel data 14 (P14) if PIXTEST is on. Otherwise, it's used as an input of the serial status from 3DFX. GUI will accumulate it to a 16 bit MMIO register.
POE1#	195	IO	This is a multi-function pin. If VMI is used, it is bit 7 of the host data bus. It is an output pin for pixel data 15 (P15) if PIXTEST is on. Otherwise, it's used as the output pin OE#1, which is the OE# control signal for high bank of DRAM.

Media Port and Feature Connector Related Interface Pins:

Pin Name	Pin No.	Type	Description
P0	141	IO	P[7:0] is the pixel or video data bus from/to external Feature Connector or Video Module Interfaces. For 8-bit Feature Connector, this is a bi-directional pixel data bus. When PENFEATL is low, it functions as inputs. The pixel data from external display or video card will be passed to the internal RAMDAC for display. If PENFEATL is high, the internal RAMDAC uses pixel data internally generated for display. In this case, if PA output control for DPMS, which is defined in bit 3 of register 3?5/26, is set to normal operation, GUI will drive out pixel data. Otherwise, it will tristate the output. If VMI is used, P[7:0] is the video data inputs. This chip supports SAA7110 video decoder and CL480 MPEG decoder interfaces. For SAA7110 interfaces, P[7:0] is the lower byte of the 16-bit video data inputs. For CL480 interfaces, it's the 8-bit video data inputs.
P1	142		
P2	143		
P3	144		
P4	145		
P5	146		
P6	147		
P7	148		
P8	187	IO	P[15:8] is the pixel data bus from/to external Feature Connector or host data bus from/to VMI. If VMI is used, P(15:8) is used as the host data bus, which is bi-directional. Through this bus, CPU can access the VMI module. For SAA7110 interfaces, P(15:8) is the higher byte of the 16-bit video data inputs. For CL480, it's the 8-bit host data bus, which is inputs in read cycles, and outputs in write cycles. Otherwise, P(15:8) functions as pixel output or video input. When PENFEATL is low, it is used for video input, which will be passed to the internal RAMDAC for display . If PENFEATL is high, the internally generated pixel data will be driven out to video card if PA output control for DPMS is set to normal operation.
P9	188	IO	
P10	190	IO	
P11	191	IO	
PCLK	150	IO	This is the pixel clock input/output pin. For 8-bit Feature Connector, it's an input when PENFEATL# is low. In this case, it is used for internal RAMDAC display. When PENFEATL# is high, the internally generated pixel clock is driven out through this pin. For VMI connection, PCLK is always put in tri-state. RAMDAC use internal pixel clock for display. If external DCLK is used, only 8-bit Feature Connector configuration is allowed, i.e. other video interfaces are not applicable.
PENFEAT#	151	I	This is the EVIDEO# pin used as bidirection control for 8-bit Feature Connector. When set to 1, GUI will drive P[15:0], BLANK#, HSYNC, VSYNC and PCLK to the Feature Connector. When set to 0, all of these signal pins are tri-stated. If video interface is enabled, i.e. either SAA7110 or CL480 is used for video data input, this pin loses its function.

Media Port and Feature Connector Related Interface Pins:(Continued)

Pin Name	Pin No.	Type	Description
TDCLK	152	I	It is a dual-function pin. If external VCG is selected, it is used as DCLK input. Otherwise, it is the video input pin for video interface.
TMCLK	153	I	It is a dual-function pin. If external VCG is selected, it is used as MCLK input. Otherwise, it is the CFLEVEL input from CL480 or ODD from SAA7110. When used as the CFLEVEL from CL480, it indicates that the CL480 Coded Data FIFO for compressed data is going to be exhausted. GUI will generate the interrupt signal to inform the software to put more compressed data into CL480. When used as the ODD signal from SAA7110, it is an odd/even field indication for interlaced video. When high, it is odd field, otherwise, even field. GUI uses this to determine the memory location for incoming video data.
BLANK#	154	IO	This is a multi-function pin. For 8-bit Feature Connector, when PENFEATL# is high, the internal BLANK# signal is output to control RAMDAC display. When PENFEATL# is set to 0, it's an input from Feature Connector. GUI uses it to control RAMDAC display. For VMI or SAA7110, it's the HREF input. And for CL480 it's the HSYNC# input. In either case, it indicates that video data of a scanline is coming in.
HSYNC#	155	TO	It's the HSYNC# output pin, which is the horizontal sync to analog monitor. For 8-bit Feature Connector, it is enabled when PENFEATL# is high or either SAA7110 or CL480 is selected. Otherwise, it is tristated.
VSYNC#	156	TO	I t 's the HSYNC# output pin, which is the horizontal sync to analog monitor. For 8-bit Feature Connector, it is enabled when PENFEATL# is high or either SAA7110 or CL480 is selected. Otherwise, it is tristated.
VMIVS	198	IO	If external VCG is selected, this pin is used as one of the MCLK select output, MCSEL1. MCSEL[2:0] is used to select MCLK frequency from external VCG. If internal VCG is used, it is an input pin for video interface. It's the VREF for VMI, VS for SAA7110 and VSYNC# for CL480. Either one indicates that it's the frame start of input video data.
SCK	5	IO	It's the I^2CCLK input/output pin for both SAA7110 interface or DDC2 monitor control. As an input, the I^2C CLK value can be monitored by reading bit 2 of the memory-mapped register port at offset 31C or bit 2 of the I/O register at 3?5/50. To generate clock pulses, software can just program either bit 0 of the above memory-mapped register or bit 5 of the IO register at 3C4/1E. If 0 is programmed, this pin is pulled low. If 1 is programmed, this pin is tri-stated. With the external pull-up, it makes I^2CCLK go to high state. In this way, clock pulses are generated.

Media Port and Feature Connector Related Interface Pins:(Continued)

Pin Name	Pin No.	Type	Description
SDA	204	IO	This is a multi-function pin. If external VCG is selected, this pin is used as of the MCLK select output, MCSEL2. Otherwise, it is the serial data input/ouput pin for I^2C bus. As an input, it can be monitored by reading bit 3 of the memory-mapped register at offset 31C, or of the I/O port at 3?5/50. To generate data, software can program either bit 1 of the above memory-mapped register or bit 6 of the I/O register at 3C4/1E.
VMIHSEL0	200	O	This is a dual-function pin. If external DCLK is selected, this pin is used as one of the DCLK select output, VCKSEL0. VCKSEL[3:0] is used to select DCLK frequency from external VCG. Otherwise, it is used as HA0 for VMI or HSEL0 for CL480. HA[3:0] and HSEL[3:0] are the host address bus for VMI and CL480 individually.
VMISEL1	202	O	This is a dual-function pin. If external DCLK is selected, this pin is used as one of the DCLK select output, VCKSEL1. Otherwise, it is used as HA1 for VMI or HSEL1 for CL480.
VMISEL2	202	O	This is a dual-function pin. If external DCLK is selected, this pin is used as one of the DCLK select output, VCKSEL2. Otherwise, it is used as HA2 for VMI or HSEL2 for CL480.
VMISEL3	202	O	This is a dual-function pin. If CL480 or VMI interface is enabled, it is HA3 or HSEL3 output, the address for host I/O accesses. It is also a general data input / output pin. As an input, it can be read through bit 1 of IO port 3?5/50. Otherwise, it is driven out as an general data output. Bit 4 of register 3C5/1E is selected as its output value.
VMIRW#	203	IO	This is a dual-function pin. If external DCLK is selected, this pin is used as one of the DCLK select output, VCKSEL3. Otherwise, it is used as R/W# for VMI or CL480. In that case, it controls the host read/write with them. For read cycles, it is driven high, for write cycles, it is driven low.
VMIDS#	197	O	It is a dual-function pin. If external VCG is selected, it is used as one of the MCLK select output, MCSEL0. Otherwise, it is used as DS# for VMI or CL480. GUI pulls it low to select VMI target or CL480 for read/write operation.

Media Port and Feature Connector Related Interface Pins:(Continued)

Pin Name	Pin No.	Type	Description
VMIDTACK#	184	IO	It is a dual-function pin. If CL480 or VMI interface is enabled, it is the DTACK# input, which is the host data acknowledge from them. When set to 0, it indicates that CL480 or VMI target is ready for data receiving or output. GUI can thus complete the cycle. If not the above case, it is a general data I/O pin. It can be read through bit 0 of IO port 3?5/50. As an output, it'in tristate normally. Write to I/O register 3C2, 3C5/1D or 3C5/1E will enable it. Bit 3 of 3C5/1E is selected as its output value.
PSTROBE	186	O	This is the data write strobe for external devices when VMIHSEL3 or VMIDTACKB is used as general data input/output pins. It is used to latch VMIHSEL3 and VMIDTACKB driven by GUI. It is high when I/O registers 3C2, 3C5/1D or 3C5/1E is written or power-on reset completes. If external VCG is used, it is used to latch VCKSEL[3:0]. The external VCG will use these values to generate expected frequencies of DCLK.
PIMCKSTRD#	196	O	This is the data read enable for external devices when VMIHSEL3 or VMIDTACKB is used as general data input/output pins. The external devices should drive VMIHSEL3 and VMIDTACKB when this signal is low. Otherwise, put them to tri-state.

POWER PINS:

PIN NAME	PIN TYPE	PIN NO.	DRIVE(ma)	C_LOAD(pf)
VDDP	-	11,57,123,164,199,	-	-
GNDP	-	21,48,65,73,100,113, 140,149,176, 189	-	-
VDD	-	30,93,165,		
GND	-	39,86,96,132,166,	-	-
AVDD	-	1,159, 163		
AVSS	-	3,160, 162,205		

4.0 ELECTRICAL CHARACTERISTICS

4.1 Absolute Maximum Ratings

RATONG	VALUE
DC Supply Voltage (VCC)	4.75V to 5.25V
DC Input/Output Voltage (Vin/Vout)	-0.5V to VCC+0.5V
Ambient Temperature (TA)	0 to 70 Celsius
Storage Temperature (TSTG)	-40 to 125 Celsius
ESD rating (Rzap=1.5K, Czap=100pF)	2000V
Power Dissipation (PD)	1.75W

Table 4-1 Absolute Maximum Ratings

4.2 DC CHARACTERISTICS

SYMBOL	Description	MIN	MAX	Test Conditions
VIL	Input Low Voltage	-	0.8V	
VIH	Inout High Voltage	2.4V	-	
VOL	Output Low Voltage	-	VSS+0.4V	I=2/4/8/24 mA
VOH	Output High Voltage	2.4V	-	I=-2/-4/-8/-10 mA
ICC	Power Supply Current	-	350mA	VCC=5V, 1024x768x256Cx75HZ
IIL	Input Low Current	-10uA	10uA	VCC=5.25V, Vin=0V
IIH	Input High Current	-	10uA	Vin=VCC
IDD	Static IDD Current	-	600uA	
IOZ	Output Tri-state Leakage Current	-10uA	10uA	
Cin	Input Capacitance	-	10pF	
Cout	Output Capacitance	-	10pF	

Table 4-2 DC Characteristics of MX86251

4.3 AC Characteristics

4.3.1 Clock TiminG

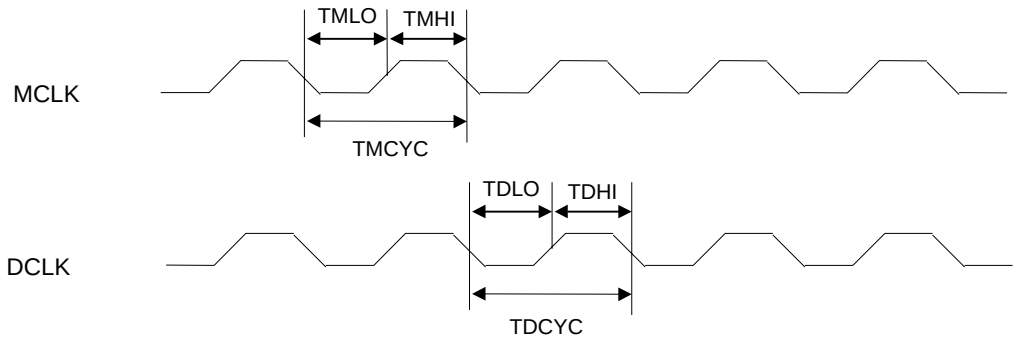


Figure 4-1. Clock Timing Diagram

SYMBOL	PARAMETER	MIN	MAX	UNITS
TMCYC	MCLK Period	14	-	ns
TMLO	MCLK Low Time	7	-	ns
TMHI	MCLK	7	-	ns

Table 4-3 MCLK Timings

SYMBOL	PARAMETER	MIN	MAX	UNITS
TDCYC	DCLK Period	6.67	-	ns
TDLO	DCLK Low Time	3.34	-	ns
TDHI	DCLK High Time	3.34	-	ns

Table 4-4. DCLK Timings

4.3.2 Reset Timings

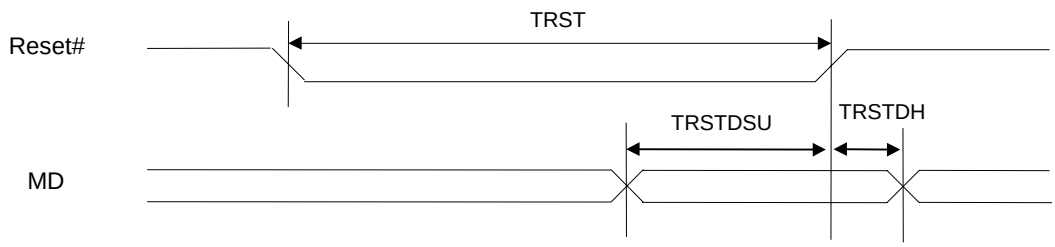


Figure 4-2. Reset Timing Diagram

SYMBOL	PARAMETER	MIN	MAX	UNITS
TRST	RESET# Pulse Width	150	-	ns
TRSTDSU	Power-on Strap Data Setup Time	15	-	ns
TRSTDH	Power-on Strap Data Hold Time	10	-	ns

Table 4-5. RESET Timings

4.3.3 PCI Interface Timing

4.3.3.1 PCI Write Timings

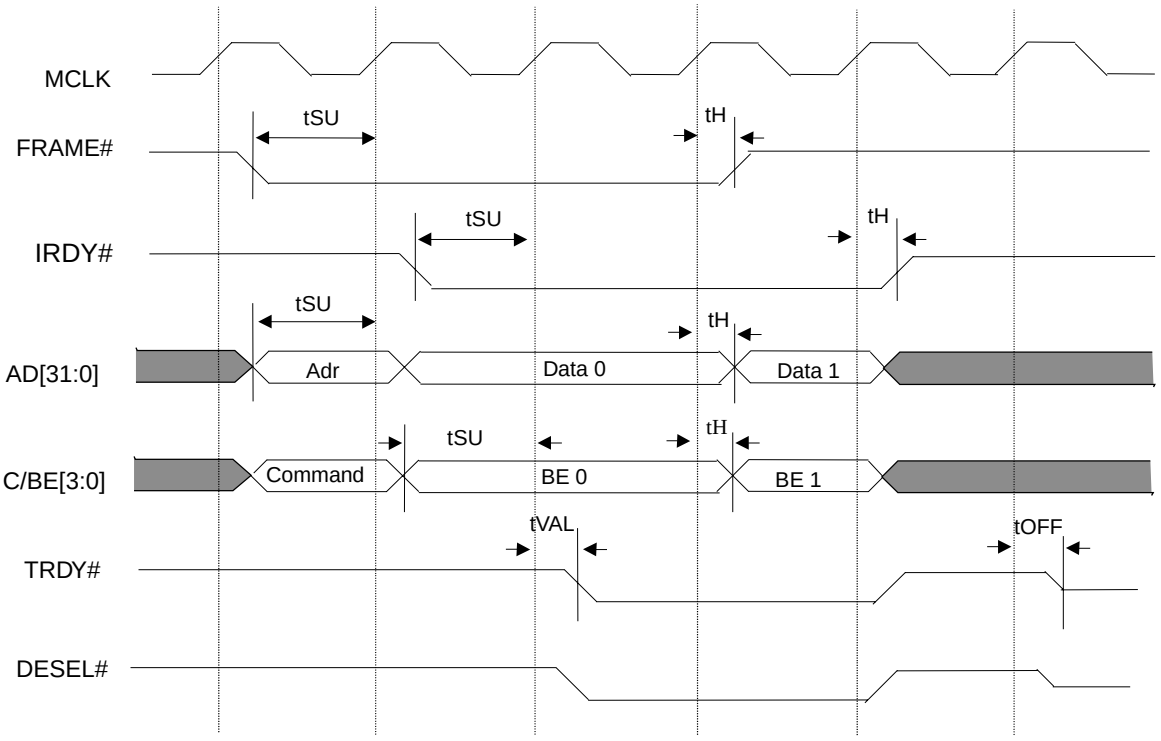


Figure 4-3. PCI Write Timing Diagram

SYMBOL	PARAMETER	MIN	MAX	UNITS
tSU	Input Setup Time from CLK	7	-	ns
tH	Input Hold Time from CLK	0	-	ns
tVAL	Output Valid Time to PCICLK	-	12	ns
tOFF	CLK to Tri-state Delay	2	-	ns

Table 4-6. PCI Write Timings

4.3.3.2 PCI Read Timings

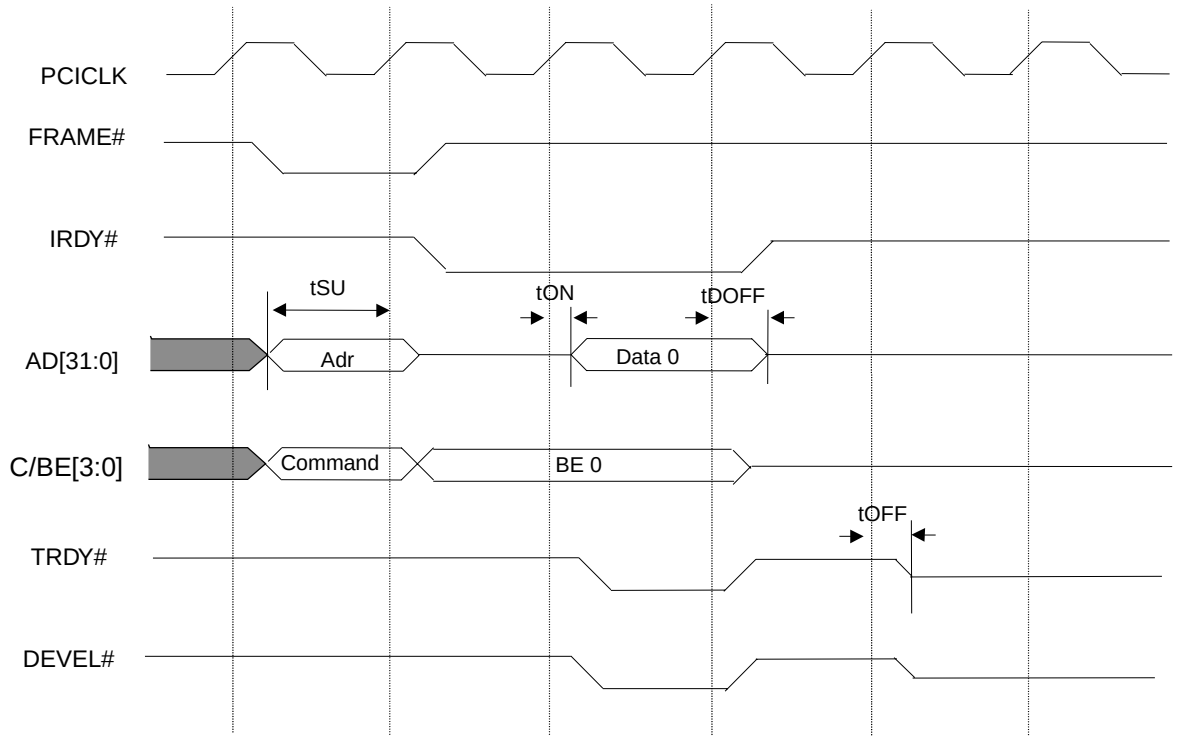


Figure 4-4. PCI Read Timing Diagram

SYMBOL	PARAMETER	MIN	MAX	UNITS
tON	AD output active from float	2	-	ns
tDOFF	AD output float from CLK Delay	2	-	ns
tOFF	CLK to Tri-state Delay	2	-	ns

Table 4-7. PCI Read Timings

4.3.3.3 PCI Disconnect Timings

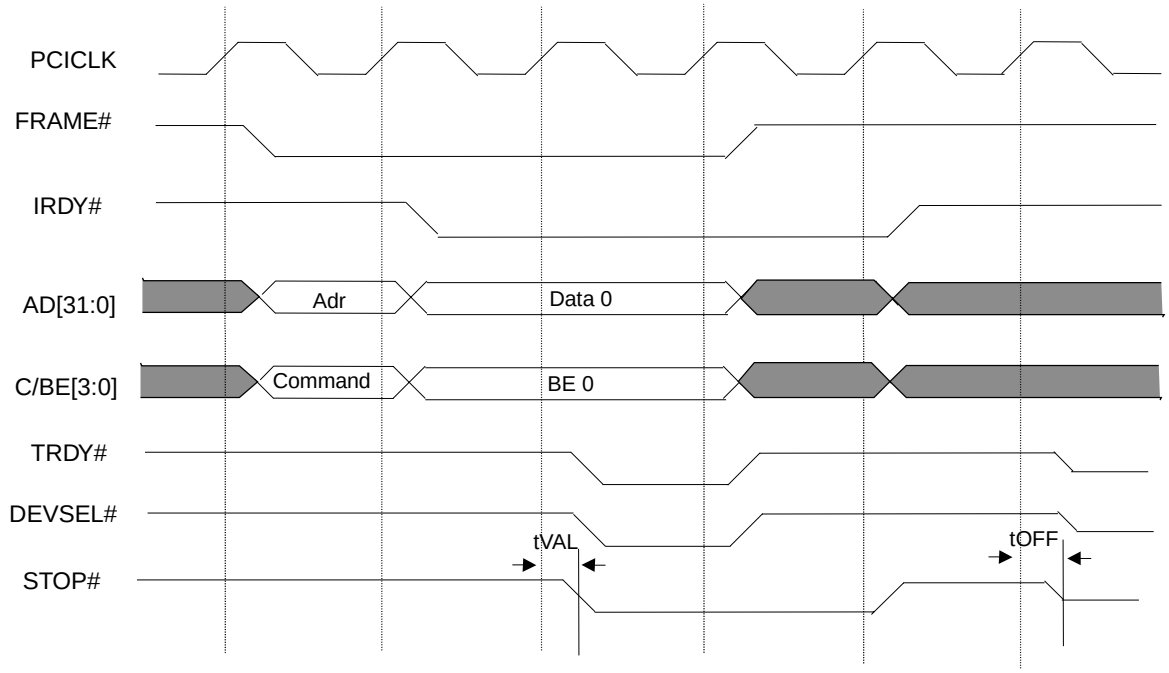
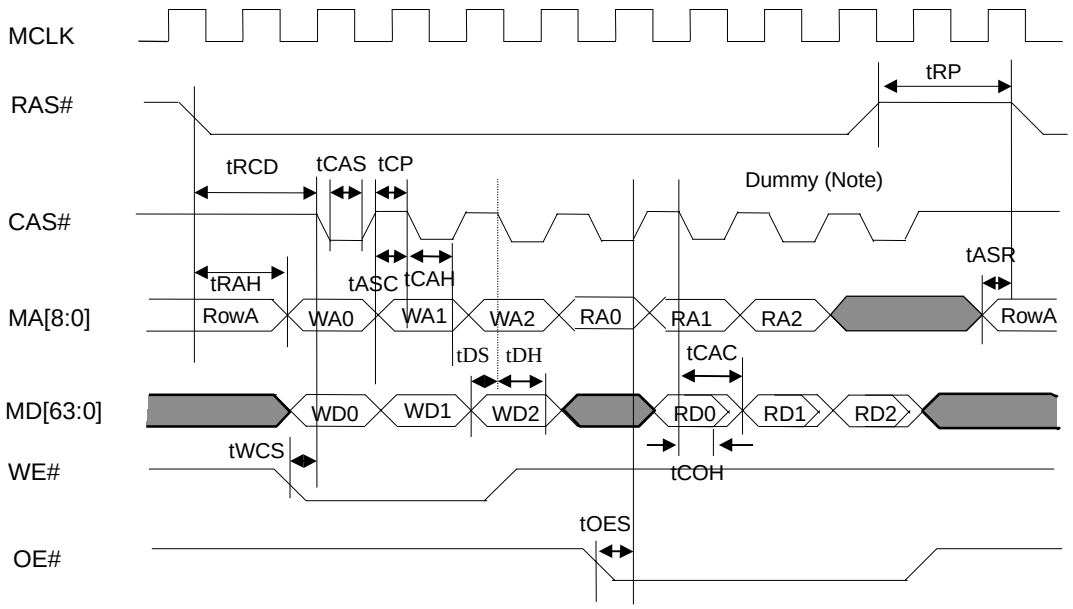


Figure 4-5. PCI Disconnect Timing Diagram

4.3.4 DRAM TIMINGS



Note:Read Dummy cycle is optional.

Figure 4-6. EDO DRAM Read/Erite Timings

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
tRP	RAS# Precharge Time	2	4.5	MCLK	1
tRCD	RAS# to CAS# Delay Time	1.5	5	MCLK	1
tASR	Row Address Setup Time	4	-	ns	2,3
tRAH	Row Address Hold Time	15	-	ns	
tCAS	CAS# pulse width	7	-	ns	2,4
tCP	CAS# Precharge Time	7	-	ns	2
tWCS	WE# to CAS# Setup Time	5	-	ns	2,4,5
tOES	OE# Low to CAS# High Setup Time	5	-	ns	2,4,7
tASC	Column Address Setup Time	7	-	ns	2,3,4
tCAH	Column Address Hold Time	6	-	ns	2,3,4
tDS	Write Data to CAS# Setup Time	4	-	ns	2,4,6
tDH	Write Data Hold Time	5	-	ns	2,4,6
tCAC	Read Data Access Time From CAS#	-	10	ns	
tCOH	Raed Data Hold Time After CAS# Low	3	-	ns	

Table 4-8. EDO DRAM Timings

Notes:
1.tRP and tRCD can be programmed through CRTC register 1AH.
2.MCLK period=15ns, i.e. 65MHZ.
3.Test under MA loading 30pF.
4.Test under CAS# loading 15pF.
5.Test under WE# loading 20pF.
6.Test under MD loading 15pF.
7.Test under OE# loading 20pF.

4.4 ESD Protection Capability

- MIL mode : 1500V
- EIAJ mode : 300V

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