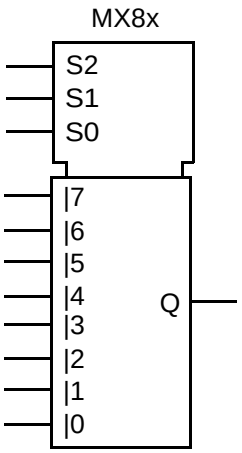
AMERICAN MICROSYSTEMS, INC.

AMI5HG 0.5 micron CMOS Gate Array

Description

MX8x is a family of eight-to-one digital multiplexers.

Logic Symbol



Truth Table

S2	S1	S0	Q
L	L	L	I0
L	L	H	I1
L	H	L	I2
L	H	H	I3
H	L	L	I4
H	L	H	I5
H	H	L	I6
H	H	H	I7

HDL Syntax

Verilog ..... MX8x *inst_name* (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

VHDL..... *inst_name*: MX8x port map (Q, I0, I1, I2, I3, I4, I5, I6, I7, S0, S1, S2);

Pin Loading

Pin Name	Equivalent Loads			
	MX81	MX82	MX84	MX86
I0	1.0	1.0	1.0	1.0
I1	1.0	1.0	1.0	1.0
I2	1.0	1.0	1.0	1.0
I3	1.0	1.0	1.0	1.0
I4	1.0	1.0	1.0	1.0
I5	1.0	1.0	1.0	1.0
I6	1.0	1.0	1.0	1.0
I7	1.0	1.0	1.0	1.0
S0	5.6	5.9	5.9	5.9
S1	3.3	3.5	3.5	3.5
S2	2.2	2.1	3.3	3.3

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX81	19.0	TBD	34.8
MX82	26.0	TBD	47.5
MX84	27.0	TBD	46.1
MX86	28.0	TBD	42.7

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		**1**	**4**	**8**	**13**	**17 (max)**
MX81	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.89 0.92	1.01 1.06	1.12 1.20	1.25 1.34	1.33 1.44
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.08 1.15	1.18 1.29	1.30 1.43	1.44 1.56	1.55 1.66
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
MX82	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.99 0.92	1.05 1.02	1.10 1.10	1.13 1.18	1.17 1.27
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.22 1.20	1.27 1.27	1.31 1.35	1.36 1.42	1.41 1.50
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
MX84	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.02 1.05	1.15 1.22	1.26 1.33	1.34 1.42	1.41 1.50
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.24 1.24	1.40 1.45	1.48 1.58	1.54 1.68	1.58 1.78
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
MX86	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	1.07 1.08	1.22 1.28	1.31 1.41	1.39 1.51	1.46 1.60
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	1.27 1.32	1.42 1.55	1.52 1.67	1.59 1.76	1.67 1.85

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

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Logic Schematic