



## MX573BBA156M250

Ultra-low Jitter 156.25MHz LVPECL XO

ClockWorks™ FUSION

### General Description

The MX573BBA156M250 is an ultra-low phase jitter XO with LVPECL output optimized for high line rate applications.

### Applications

- 10/40/400 Gigabit Ethernet
- Fibre Channel 10G/12G SERDES

### Absolute Maximum Ratings

Supply Voltage (VIN).....+3.6V  
Lead Temperature (soldering, 10s).....260°C  
Storage Temperature (T<sub>g</sub>).....125°C  
ESD Rating (HBM).....2kV

### Features

- 156.25MHz LVPECL
- Typical phase noise:  
-80fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 7mm x 5mm LGA package

### Operating Ratings

Supply Voltage (VIN).....+2.375V to +3.63V  
Ambient Temperature (TA).....-40°C to +85°C

### Electrical Characteristics

VDD = 2.375 - 3.63V, TA = -40°C to +85°C, outputs terminated with 50 Ohms to VDD - 2.<sup>1</sup>

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
IDD	Supply Current				120	mA
F0	Center Frequency			156.25		MHz
	Frequency Stability	Note 2			±50	ppm
Øj	Phase Noise	Integration Range (12kHz to 20MHz) Integration Range (1.875MHz to 20MHz)		175 80		fsRMS
Tstart	Start-Up Time				20	ms
TR/TF	Rise/Fall time		300			ps
	Duty Cycle		45		55	%
VOH	Output High Voltage	LVPECL output levels	VDD - 1.35	VDD - 1.01	VDD - 0.8	V
VOL	Output Low Voltage	LVPECL output levels	VDD - 2.0	VDD - 1.78	VDD - 1.6	V
Vswing	Peak to Peak Output Voltage Swing		0.65	0.77	0.95	V

#### Notes:

1. Guaranteed after thermal equilibrium.
2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration from -40°C to +85°C.

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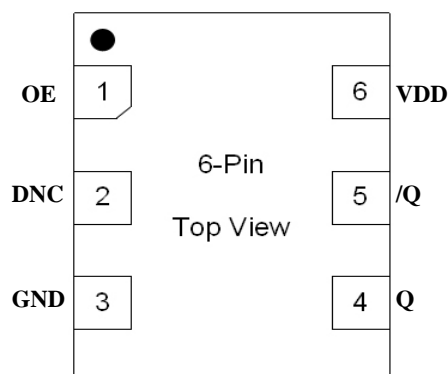
Revision 1.0  
[tcghelp@micrel.com](mailto:tcghelp@micrel.com) or (408) 955-1690

## Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX573BBA156M250	MX573BB	A156M250	Tube	6-Pin 7mm x 5mm LGA
MX573BBA156M250 TR	MX573BB	A156M250	Tape and Reel	6-Pin 7mm x 5mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

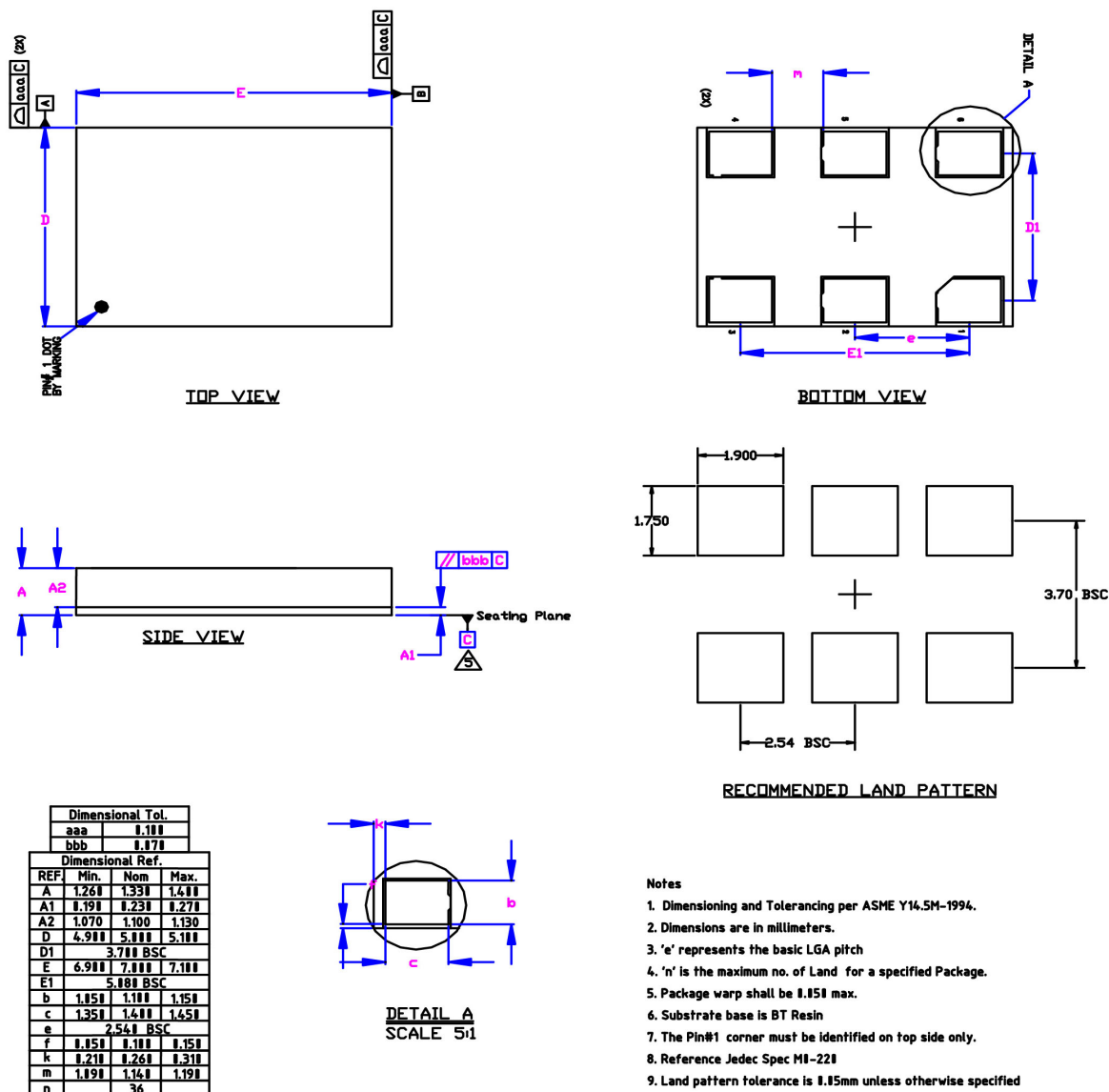
## Pin Configuration



## Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVC MOS	Output Enable, disables output to tri-state, 0 = Disabled, 1 = Enabled, 50k Ohms Pull-Up
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, /Q	O, Diff	LVPECL	Clock Output Frequency = 156.25MHz
6	VDD	PWR		Power Supply

## Package Information and Recommended Land Pattern for 6-Pin LGA<sup>3</sup>



### 6-Pin LGA (7x5mm)

#### Note:

3. Package information is correct as of the publication date. For updates and most current information, go to [www.micrel.com](http://www.micrel.com).

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