MULTIPLEXED, Burst Mode, Flash Memory

MX29NS320E/640E/128E

Contents

1. FEATURES

Characteristics

Burst Length

- Continuous linear burst
- 8/16 word linear burst length with wrap around

Sector Architecture

- Single bank Architecture.
- Four 8 Kword sectors in upper-most address range (MX29NS320E/640E)
- Four 16Kword sectors in upper-most address range (MX29NS128E)
- MX29NS320E: Sixty-three 32 KWord
- MX29NS640E: One hundred twenty-seven 32 Kword sectors
- MX29NS128E: One hundred twenty seven 64 Kword sectors

Power Supply Operations

- 1.8V for read, program and erase operations (1.70V to 1.95V)
- Deep power down mode

Performance

High Performance

- 40 µs - Word programming time
- 9.4 µs - Effective word programming time utilizing a 32 word Write Buffer at VCC level
- 4.8 µs - Effective word programming time of utilizing a 32 word Write Buffer at ACC level

Sector Erase Time

- 600 ms for 32 Kword sectors
- 800 ms for 64 Kword sectors

VI/O Feature

- Generates data output voltages and tolerates data input voltages as determined by the voltage on the VI/O pin
- 1.8V compatible I/O signals

Read Access Time

- Burst access times: 7 ns (at industrial temperature range)
- 80 ns of Asynchronous random access times
- 80 ns of Synchronous random access times

Secured Silicon Sector Region

- 256 words accessible through a command sequence
- 128 words for the factory secured silicon sector
- 128 words for the customer secured silicon sector

Power Dissipation

- Typical values: 8 bits switching, CL = 10 pF at 108 MHz, CIN excluded
- 32 mA for Continuous burst read mode
- 20 mA for Program/Erase Operations
- 40 uA for Standby mode

Program/Erase Cycles

- 100,000 cycles typical

Data Retention

- 20 years

Hardware Features

- Supports multiplexing data and address for reduced I/O count.
- A15–A0 multiplexed as Q15–Q0 Sector Architecture

Hardware Sector Protection

- WP# protects two highest sectors
- All sectors locked when ACC = VIL

Package

- 56-Ball Thin FBGA (Fine-Pitch Ball Grid Array)
- REACH SVHC Free and RoHS Compliant

Handshaking Feature

- Allows system to determine the read operation of burst data with minimum possible latency by monitoring RDY.

Data# Polling and Toggle Bits

- Provides a software method of detecting and sending signals to indicate the completion of program and erase operations.

Erase Suspend/Erase Resume

- Erase operation will be halted when the device receives an Erase Suspend command. And will be restarted when the device receives the Erase Resume command.

Program Suspend/Program Resume

- Program operation will be halted when the device receives a Program Suspend command. It will be restarted when the device receives the Program Resume command.

Electronic Identification

- Software command set compatible with JEDEC 42.4 standards
- Common Flash Interface (CFI) supported

Software Features

Advanced Security Features

- Volatile Sector Protection
- A command sector protection method that protects individual sectors from being programmed or erased.
- Sectors can be locked or unlocked in-system at VCC level.

2. GENERAL INFORMATION

2-1. Operating Speeds

Clock Speed	Burst Access (ns)	Synch. Initial Access (ns)	Asynch. Initial Access (ns)	Output Loading
108 MHz	7	80	80	10 pF

The operating temperature range is -40°C to +85°C.

2-2. Ordering Information

Part Number	Access Time (ns)	Package	Remark
MX29NS320E XJI-80G MX29NS640E XJI-80G MX29NS128EXJI-80G	80	56 TFBGA	VI/O=VCC

NOTES:

1. *MX29NS320/640/128E have been pre-released and in mass production.*
2. *MX29NS128E is for the validation of MCP products. Please contact Macronix local sales for discrete product support.*

2-3. Part Name Description

MX 29 NS 640 E XJ I - 80 G

G: RoHS Compliant

Speed:
80: 80ns

Temperature Range:
I: Indsustrial
-40°C ~ +85°C

Package:
XJ: TFBGA

Revision: E

Density & Mode:
128: 128Mb;
640: 64Mb
320: 32Mb

NS: 1.8V Burst Mode

Device:
29: Flash

Brand:
MX

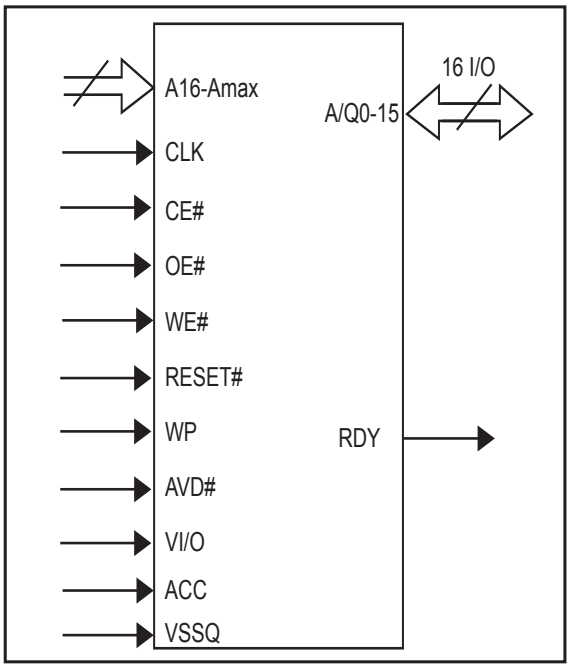
3. PIN CONFIGURATION / SYMBOL DESCRIPTION

56-Ball Thin FBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	A1 NC													A14 NC
B														
C			C3 NC	C4 NC			C7 NC	C8 NC			C11 NC	C12 NC		
D			D3 RDY	D4 A21	D5 V_{SS}	D6 CLK	D7 V_{CC}	D8 WE#	D9 ACC	D10 A19	D11 A17	D12 A22		
E			E3 $V_{I/O}$	E4 A16	E5 A20	E6 AVD#	E7 NC	E8 RESET#	E9 WP#	E10 A18	E11 CE#	E12 V_{SSQ}		
F			F3 VSS	F4 A/Q7	F5 A/Q6	F6 A/Q13	F7 A/Q12	F8 A/Q3	F9 A/Q2	F10 A/Q9	F11 A/Q8	F12 OE#		
G			G3 A/Q15	G4 A/Q14	G5 V_{SSQ}	G6 A/Q5	G7 A/Q4	G8 A/Q11	G9 A/Q10	G10 $V_{I/O}$	G11 A/Q1	G12 A/Q0		
H			H3 NC	H4 NC			H7 NC	H8 NC			H11 NC	H12 NC		
J														
K	K1 NC													K14 NC

NOTE: *A22 is for MX29NS128E;*
A21 is for MX29NS640E.

3-1. Logic Symbol



3-2. Pin Descriptions

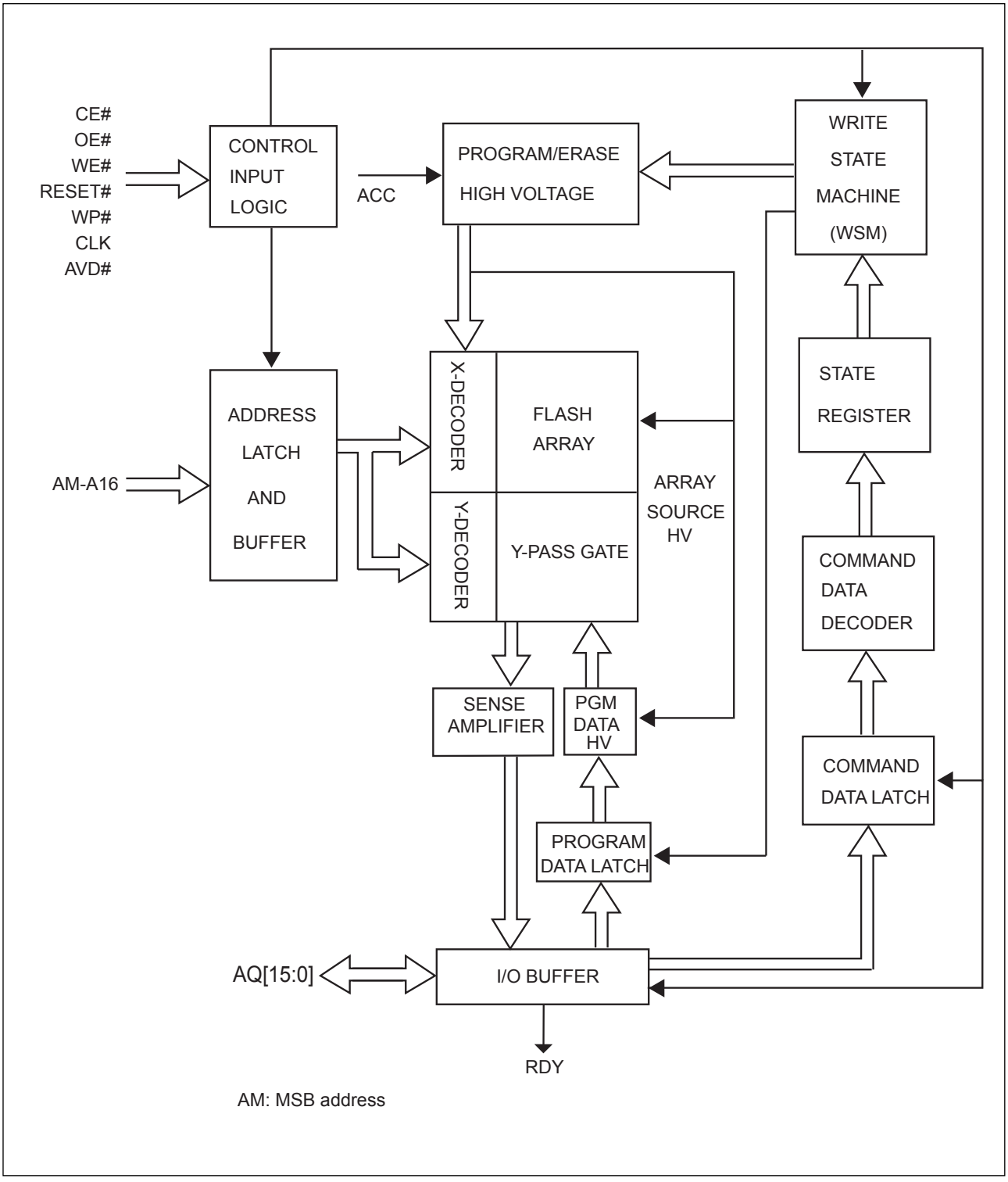
SYMBOL	DESCRIPTIONS
A22-A16	Address Inputs for MX29NS128E
A21-A16	Address Inputs for MX29NS640E
A20-A16	Address Inputs for MX29NS320E
A/Q15~ A/Q0	Multiplexed Data Inputs/Outputs
CE#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
VCC	Device Power Supply (1.70V~1.95V)
VI/O	Input/Output Power Supply (1.70V~1.95V)
VSS	Device Ground
VSSQ	Input/Output Ground
NC	No Connection
RDY	Ready output, the status of the Burst Read
	Refer to configuration register table
CLK	The first rising edge of CLK in conjunction with AVD# low latches address input and activates burst mode operation.
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs (Address bits A15–A0 are multiplexed, address bits Amax–A16 are address only). VIL= For asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. VIH = Device ignores address inputs
RESET#	Hardware Reset Pin, Active Low
WP#	Hardware Write Protect
ACC	Programming Acceleration Input

***NOTES**:*

1. *WP# and ACC have internal pull up. WP# VIL protects the upper most two sectors from write; ACC=Vhv enters into the ACC programming mode. ACC=VIL, erase/program function disabled.*
2. *VI/O Voltage must tight up with VCC.*

   VI/O = VCC = 1.70V~1.95V

4. BLOCK DIAGRAM



4-1. Block Structure

The main flash memory array is organized as Word mode (x16). The details of the address ranges and the corresponding sector addresses are shown in Table 1.

Table 1-1. Sector Address Table (MX29NS320E)

Sector Size Kwords	Sector	Address Range
32	SA0	000000h-007FFFh
32	SA1	008000h-00FFFFh
32	SA2	010000h-017FFFh
32	SA3	018000h-01FFFFh
32	SA4	020000h-027FFFh
32	SA5	028000h-02FFFFh
32	SA6	030000h-037FFFh
32	SA7	038000h-03FFFFh
32	SA8	040000h-047FFFh
32	SA9	048000h-04FFFFh
32	SA10	050000h-057FFFh
32	SA11	058000h-05FFFFh
32	SA12	060000h-067FFFh
32	SA13	068000h-06FFFFh
32	SA14	070000h-077FFFh
32	SA15	078000h-07FFFFh
32	SA16	080000h-087FFFh
32	SA17	088000h-08FFFFh
32	SA18	090000h-097FFFh
32	SA19	098000h-09FFFFh
32	SA20	0A0000h-0A7FFFh
32	SA21	0A8000h-0AFFFFh
32	SA22	0B0000h-0B7FFFh
32	SA23	0B8000h-0BFFFFh
32	SA24	0C0000h-0C7FFFh
32	SA25	0C8000h-0CFFFFh
32	SA26	0D0000h-0D7FFFh
32	SA27	0D8000h-0DFFFFh
32	SA28	0E0000h-0E7FFFh
32	SA29	0E8000h-0EFFFFh
32	SA30	0F0000h-0F7FFFh
32	SA31	0F8000h-0FFFFFh
32	SA32	100000h-107FFFh
32	SA33	108000h-10FFFFh
32	SA34	110000h-117FFFh
32	SA35	118000h-11FFFFh
32	SA36	120000h-127FFFh
32	SA37	128000h-12FFFFh
32	SA38	130000h-137FFFh
32	SA39	138000h-13FFFFh
32	SA40	140000h-147FFFh

Sector Size Kwords	Sector	Address Range
32	SA41	148000h-14FFFFh
32	SA42	150000h-157FFFh
32	SA43	158000h-15FFFFh
32	SA44	160000h-167FFFh
32	SA45	168000h-16FFFFh
32	SA46	170000h-177FFFh
32	SA47	178000h-17FFFFh
32	SA48	180000h-187FFFh
32	SA49	188000h-18FFFFh
32	SA50	190000h-197FFFh
32	SA51	198000h-19FFFFh
32	SA52	1A0000h-1A7FFFh
32	SA53	1A8000h-1AFFFFh
32	SA54	1B0000h-1B7FFFh
32	SA55	1B8000h-1BFFFFh
32	SA56	1C0000h-1C7FFFh
32	SA57	1C8000h-1CFFFFh
32	SA58	1D0000h-1D7FFFh
32	SA59	1D8000h-1DFFFFh
32	SA60	1E0000h-1E7FFFh
32	SA61	1E8000h-1EFFFFh
32	SA62	1F0000h-1F7FFFh
8	SA63	1F8000h-1F9FFFh
8	SA64	1FA000h-1FBFFFh
8	SA65	1FC000h-1FDFFFh
8	SA66	1FE000h-1FFFFFh

Table 1-2. Sector Address Table (MX29NS640E)

Sector Size Kwords	Sector	Address Range
32	SA0	000000h-007FFFh
32	SA1	008000h-00FFFFh
32	SA2	010000h-017FFFh
32	SA3	018000h-01FFFFh
32	SA4	020000h-027FFFh
32	SA5	028000h-02FFFFh
32	SA6	030000h-037FFFh
32	SA7	038000h-03FFFFh
32	SA8	040000h-047FFFh
32	SA9	048000h-04FFFFh
32	SA10	050000h-057FFFh
32	SA11	058000h-05FFFFh
32	SA12	060000h-067FFFh
32	SA13	068000h-06FFFFh
32	SA14	070000h-077FFFh
32	SA15	078000h-07FFFFh
32	SA16	080000h-087FFFh
32	SA17	088000h-08FFFFh
32	SA18	090000h-097FFFh
32	SA19	098000h-09FFFFh
32	SA20	0A0000h-0A7FFFh
32	SA21	0A8000h-0AFFFFh
32	SA22	0B0000h-0B7FFFh
32	SA23	0B8000h-0BFFFFh
32	SA24	0C0000h-0C7FFFh
32	SA25	0C8000h-0CFFFFh
32	SA26	0D0000h-0D7FFFh
32	SA27	0D8000h-0DFFFFh
32	SA28	0E0000h-0E7FFFh
32	SA29	0E8000h-0EFFFFh
32	SA30	0F0000h-0F7FFFh
32	SA31	0F8000h-0FFFFFh
32	SA32	100000h-107FFFh
32	SA33	108000h-10FFFFh
32	SA34	110000h-117FFFh
32	SA35	118000h-11FFFFh
32	SA36	120000h-127FFFh
32	SA37	128000h-12FFFFh
32	SA38	130000h-137FFFh
32	SA39	138000h-13FFFFh
32	SA40	140000h-147FFFh
32	SA41	148000h-14FFFFh
32	SA42	150000h-157FFFh
32	SA43	158000h-15FFFFh
32	SA44	160000h-167FFFh
32	SA45	168000h-16FFFFh

Sector Size Kwords	Sector	Address Range
32	SA47	178000h-17FFFFh
32	SA48	180000h-187FFFh
32	SA49	188000h-18FFFFh
32	SA50	190000h-197FFFh
32	SA51	198000h-19FFFFh
32	SA52	1A0000h-1A7FFFh
32	SA53	1A8000h-1AFFFFh
32	SA54	1B0000h-1B7FFFh
32	SA55	1B8000h-1BFFFFh
32	SA56	1C0000h-1C7FFFh
32	SA57	1C8000h-1CFFFFh
32	SA58	1D0000h-1D7FFFh
32	SA59	1D8000h-1DFFFFh
32	SA60	1E0000h-1E7FFFh
32	SA61	1E8000h-1EFFFFh
32	SA62	1F0000h-1F7FFFh
32	SA63	1F8000h-1FFFFFh
32	SA64	200000h-207FFFh
32	SA65	208000h-20FFFFh
32	SA66	210000h-217FFFh
32	SA67	218000h-21FFFFh
32	SA68	220000h-227FFFh
32	SA69	228000h-22FFFFh
32	SA70	230000h-237FFFh
32	SA71	238000h-23FFFFh
32	SA72	240000h-247FFFh
32	SA73	248000h-24FFFFh
32	SA74	250000h-257FFFh
32	SA75	258000h-25FFFFh
32	SA76	260000h-267FFFh
32	SA77	268000h-26FFFFh
32	SA78	270000h-277FFFh
32	SA79	278000h-2F7FFFh
32	SA80	280000h-287FFFh
32	SA81	288000h-28FFFFh
32	SA82	290000h-297FFFh
32	SA83	298000h-29FFFFh
32	SA84	2A0000h-2A7FFFh
32	SA85	2A8000h-2AFFFFh
32	SA86	2B0000h-2B7FFFh
32	SA87	2B8000h-2BFFFFh
32	SA88	2C0000h-2C7FFFh
32	SA89	2C8000h-2CFFFFh
32	SA90	2D0000h-2D7FFFh
32	SA91	2D8000h-2DFFFFh
32	SA92	2E0000h-2E7FFFh

Sector Size Kwords	Sector	Address Range
32	SA93	2E8000h-2EFFFFh
32	SA94	2F0000h-2F7FFFh
32	SA95	2F8000h-2FFFFFh
32	SA96	300000h-307FFFh
32	SA97	308000h-30FFFFh
32	SA98	310000h-317FFFh
32	SA99	318000h-31FFFFh
32	SA100	320000h-327FFFh
32	SA101	328000h-32FFFFh
32	SA102	330000h-337FFFh
32	SA103	338000h-33FFFFh
32	SA104	340000h-347FFFh
32	SA105	348000h-34FFFFh
32	SA106	350000h-357FFFh
32	SA107	358000h-35FFFFh
32	SA108	360000h-367FFFh
32	SA109	368000h-36FFFFh
32	SA110	370000h-377FFFh
32	SA111	378000h-37FFFFh
32	SA112	380000h-387FFFh
32	SA113	388000h-38FFFFh
32	SA114	390000h-397FFFh
32	SA115	398000h-39FFFFh
32	SA116	3A0000h-3A7FFFh
32	SA117	3A8000h-3AFFFFh
32	SA118	3B0000h-3B7FFFh
32	SA119	3B8000h-3BFFFFh
32	SA120	3C0000h-3C7FFFh
32	SA121	3C8000h-3CFFFFh
32	SA122	3D0000h-3D7FFFh
32	SA123	3D8000h-3DFFFFh
32	SA124	3E0000h-3E7FFFh
32	SA125	3E8000h-3EFFFFh
32	SA126	3F0000h-3F7FFFh
8	SA127	3F8000h-3F9FFFh
8	SA128	3FA000h-3FBFFFh
8	SA129	3FC000h-3FDFFFh
8	SA130	3FE000h-3FFFFFh

Table 1-3. Sector Address Table (MX29NS128E)

Sector Size Kwords	Sector	Address Range
64	SA0	000000h-00FFFFh
64	SA1	010000h-01FFFFh
64	SA2	020000h-02FFFFh
64	SA3	030000h-03FFFFh
64	SA4	040000h-04FFFFh
64	SA5	050000h-05FFFFh
64	SA6	060000h-06FFFFh
64	SA7	070000h-07FFFFh
64	SA8	080000h-08FFFFh
64	SA9	090000h-09FFFFh
64	SA10	0A0000h-0AFFFFh
64	SA11	0B0000h-0BFFFFh
64	SA12	0C0000h-0CFFFFh
64	SA13	0D0000h-0DFFFFh
64	SA14	0E0000h-0EFFFFh
64	SA15	0F0000h-0FFFFFh
64	SA16	100000h-10FFFFh
64	SA17	110000h-11FFFFh
64	SA18	120000h-12FFFFh
64	SA19	130000h-13FFFFh
64	SA20	140000h-14FFFFh
64	SA21	150000h-15FFFFh
64	SA22	160000h-16FFFFh
64	SA23	170000h-17FFFFh
64	SA24	180000h-18FFFFh
64	SA25	190000h-19FFFFh
64	SA26	1A0000h-1AFFFFh
64	SA27	1B0000h-1BFFFFh
64	SA28	1C0000h-1CFFFFh
64	SA29	1D0000h-1DFFFFh
64	SA30	1E0000h-1EFFFFh
64	SA31	1F0000h-1FFFFFh
64	SA32	200000h-20FFFFh
64	SA33	210000h-21FFFFh
64	SA34	220000h-22FFFFh
64	SA35	230000h-23FFFFh
64	SA36	240000h-24FFFFh
64	SA37	250000h-25FFFFh
64	SA38	260000h-26FFFFh
64	SA39	270000h-27FFFFh
64	SA40	280000h-28FFFFh
64	SA41	290000h-29FFFFh
64	SA42	2A0000h-2AFFFFh
64	SA43	2B0000h-2BFFFFh
64	SA44	2C0000h-2CFFFFh
64	SA45	2D0000h-2DFFFFh
64	SA46	2E0000h-2EFFFFh
64	SA47	2F0000h-2FFFFFh
64	SA48	300000h-30FFFFh
64	SA49	310000h-31FFFFh
64	SA50	320000h-32FFFFh
64	SA51	330000h-33FFFFh
64	SA52	340000h-34FFFFh
64	SA53	350000h-35FFFFh
64	SA54	360000h-36FFFFh
64	SA55	370000h-37FFFFh
64	SA56	380000h-38FFFFh
64	SA57	390000h-39FFFFh
64	SA58	3A0000h-3AFFFFh
64	SA59	3B0000h-3BFFFFh
64	SA60	3C0000h-3CFFFFh
64	SA61	3D0000h-3DFFFFh
64	SA62	3E0000h-3EFFFFh
64	SA63	3F0000h-3FFFFFh
64	SA64	400000h-40FFFFh
64	SA65	410000h-41FFFFh
64	SA66	420000h-42FFFFh
64	SA67	430000h-43FFFFh
64	SA68	440000h-44FFFFh
64	SA69	450000h-45FFFFh
64	SA70	460000h-46FFFFh
64	SA71	470000h-47FFFFh
64	SA72	480000h-48FFFFh
64	SA73	490000h-49FFFFh
64	SA74	4A0000h-4AFFFFh
64	SA75	4B0000h-4BFFFFh
64	SA76	4C0000h-4CFFFFh
64	SA77	4D0000h-4DFFFFh
64	SA78	4E0000h-4EFFFFh
64	SA79	4F0000h-4FFFFFh
64	SA80	500000h-50FFFFh
64	SA81	510000h-51FFFFh
64	SA82	520000h-52FFFFh
64	SA83	530000h-53FFFFh
64	SA84	540000h-54FFFFh
64	SA85	550000h-55FFFFh
64	SA86	560000h-56FFFFh
64	SA87	570000h-57FFFFh
64	SA88	580000h-58FFFFh
64	SA89	590000h-59FFFFh
64	SA90	5A0000h-5AFFFFh
64	SA91	5B0000h-5BFFFFh
64	SA92	5C0000h-5CFFFFh
64	SA93	5D0000h-5DFFFFh
64	SA94	5E0000h-5EFFFFh
64	SA95	5F0000h-5FFFFFh
64	SA96	600000h-60FFFFh
64	SA97	610000h-61FFFFh
64	SA98	620000h-62FFFFh
64	SA99	630000h-63FFFFh
64	SA100	640000h-64FFFFh
64	SA101	650000h-65FFFFh
64	SA102	660000h-66FFFFh
64	SA103	670000h-67FFFFh
64	SA104	680000h-68FFFFh
64	SA105	690000h-69FFFFh
64	SA106	6A0000h-6AFFFFh
64	SA107	6B0000h-6BFFFFh
64	SA108	6C0000h-6CFFFFh
64	SA109	6D0000h-6DFFFFh
64	SA110	6E0000h-6EFFFFh
64	SA111	6F0000h-6FFFFFh
64	SA112	700000h-70FFFFh
64	SA113	710000h-71FFFFh
64	SA114	720000h-72FFFFh
64	SA115	730000h-73FFFFh
64	SA116	740000h-74FFFFh
64	SA117	750000h-75FFFFh
64	SA118	760000h-76FFFFh
64	SA119	770000h-77FFFFh
64	SA120	780000h-78FFFFh
64	SA121	790000h-79FFFFh
64	SA122	7A0000h-7AFFFFh
64	SA123	7B0000h-7BFFFFh
64	SA124	7C0000h-7CFFFFh
64	SA125	7D0000h-7DFFFFh
64	SA126	7E0000h-7EFFFFh
16	SA127	7F0000h-7F3FFFh
16	SA128	7F4000h-7F7FFFh
16	SA129	7F8000h-7FBFFFh
16	SA130	7FC000h-7FFFFFh

5. BUS OPERATIONS

This chapter indicates the functions and utilizations of Bus Operations. Bus operations are initiated through the internal command register and executed by a bus interface or similar logic circuitry. The command register itself does not occupy any memory addresses. The register is formed of latches that store the commands, along with the address and data information needed for executing the command.

The content of the register acts as inputs to the internal state machine. The state machine outputs determine the function of the device.

Table 2. shows all the bus operations, inputs and control levels required, and the resulting output. All the operations are described in the following sections in details.

***NOTE**: Falling edge of AVD# determines when to disable the current burst cycle while a new burst read cycle is started by the rising edge of CLK.*

Table 2. Bus Operations

Operation	CE#	OE#	WE#	CLK	AVD#	Address	Data	RDY	RESET#
Synchronous Operations									
Latch Starting Burst Address by CLK	L	H	H	R	L	Addr In	Output Invalid	X	H
Advance Burst Read to Next Address	L	L	H	R	H	X	Output Valid	H	H
Terminate Current Burst Read Cycle	H	X	X	X	X	X	HighZ	HighZ	H
Terminate Current Burst Read Cycle through RESET#	X	X	X	X	X	X	HighZ	HighZ	L
Terminate Current Burst Read Cycle and Start New Burst Read Cycle	L	H	H	R	L	Addr In	Output Invalid	X	H
Asynchronous Operations									
Asynchronous Read - Addresses Latched	L	H	H	L	R	Addr In	X	H	H
Asynchronous Read - Data on Bus	L	L	H	L	H	X	Output Data	H	H
Asynchronous Program (AVD# Latched Addresses)	L	H	L	L	R	Addr In	X	H	H
Asynchronous Program (WE# Latched Data)	L	H	R	L	H	X	Input Valid	H	H
Non-Operations									
Standby (CE#)	H	X	X	X	X	X	HighZ	HighZ	H
Hardware Reset	X	X	X	X	X	X	HighZ	HighZ	L

Legend:

L = 0; H = 1; X = VIL or VIH; R = Rising ege; h-l = High to low.

NOTES:

1. *WP# protects the top two sectors.*
2. *ACC low protects all sectors.*
3. *Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.*
4. *In Word Mode, the addresses are AM to A0, AM: MSB of address.*

5-1. Non-Burst (Asynchronous) Read Operation

Upon device's power-up, non-burst mode read is as the default state. To perform a read operation, the system addresses the desired memory array or status register location by providing its address on the address pins and simultaneously enabling the chip by driving AVD# & CE# LOW, and WE# HIGH. The CLK keeps low during asynchronous read operation. The address is latched on the rising edge of AVD#; OE# will be driven low afterwards. A/Q15-A/Q0 output the data after previous operations is complete.

5-2. Burst (Synchronous) Read Operation

The device supports the following burst read modes:

- Continuous burst read

- Linear burst reads (8/16 words) with/without wrap around

5-2-1. Continuous Burst Read

Burst read mode is enabled when first CLK rising edge meets AVD# low period. The AVD# keeps low for no more than one clock cycle.

The number of dummy cycles should be set (for tIACC for each burst session) before the clock signal is being activated. Before the burst read mode is activated, the number of dummy cycle will be determined by the setting configuration register command.

The process of the continuous burst read operation is as follows:

First CLK cycle's rising edge --> Initial word output tIACC --> Wait for dummy cycle --> Rising rising edge of each consecutive clock, following words output (tBACC) (Automatically increase the internal address counter)

1. For address boundary every 8 words, the first boundary starts with 000007h, next with 00000Fh by adding 8 words address; and etc.
2. For address boundary every 128 words, the first boundary starts with 00007Fh, next with 0000FFh by adding 128 words address; and etc.
3. Additional dummy cycles are needed if the start address for the output cannot be divided by 4.

   RDY status indicates the condition of the device by de-asserting.

   NOTE*: There is a permanent internal address boundary in the device that occurs 8 or 128 words. Boundary crossing latency is needed when the device operates with dummy cycles set from 5 to 10.*

Table 3-1. Address Latency for 10, 9 and 8 Dummy Cycles

Word																	
0	10, 9 and 8 dc	D0	D1	D2	D3	D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15
1		D1	D2	D3	1dc	D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15
2		D2	D3	1dc	1dc	D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15
3		D3	1dc	1dc	1dc	D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15
4		D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15	1dc	D16	D17	D18
5		D5	D6	D7	1dc	1dc	D8	D9	D10	D11	D12	D13	D14	D15	1dc	D16	D17	D18
6		D6	D7	1dc	1dc	1dc	D8	D9	D10	D11	D12	D13	D14	D15	1dc	D16	D17	D18
7		D7	1dc	1dc	1dc	1dc	D8	D9	D10	D11	D12	D13	D14	D15	1dc	D16	D17	D18

Table 3-2. Address Latency for 7, 6, and 5 Dummy Cycles

Word										
0	7, 6, and 5 dc	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	1 dc	D4	D5	D6	D7	D8
2		D2	D3	1 dc	1 dc	D4	D5	D6	D7	D8
3		D3	1 dc	1 dc	1 dc	D4	D5	D6	D7	D8

Table 3-3. Address Latency for 4 Dummy Cycles

Word										
0	4 dc	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	1 dc	D4	D5	D6	D7	D8	D9
3		D3	1 dc	1 dc	D4	D5	D6	D7	D8	D9

Table 3-4. Address Latency for 3 Dummy Cycles

Word										
0	3 dc	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	D4	D5	D6	D7	D8	D9	D10
3		D3	1 dc	D4	D5	D6	D7	D8	D9	D10

Table 3-5. Address/8-word Boundary Crossing Latency for 10, 9 and 8 Dummy Cycles

Word																	
0	10, 9 and 8 dc	D0	D1	D2	D3	D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15
1		D1	D2	D3	1dc	D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15
2		D2	D3	1dc	1dc	D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15
3		D3	1dc	1dc	1dc	D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15
4		D4	D5	D6	D7	1dc	D8	D9	D10	D11	D12	D13	D14	D15	1dc	D16	D17	D18
5		D5	D6	D7	1dc	1dc	D8	D9	D10	D11	D12	D13	D14	D15	1dc	D16	D17	D18
6		D6	D7	1dc	1dc	1dc	D8	D9	D10	D11	D12	D13	D14	D15	1dc	D16	D17	D18
7		D7	1dc	1dc	1dc	1dc	D8	D9	D10	D11	D12	D13	D14	D15	1dc	D16	D17	D18

Table 3-6. Address/128-word Boundary Crossing Latency for 7, 6, and 5 Dummy Cycles

Word										
0	7, 6, and 5 dc	D0	D1	D2	D3	1 dc	D4	D5	D6	D7
1		D1	D2	D3	1 dc	1 dc	D4	D5	D6	D7
2		D2	D3	1 dc	1 dc	1 dc	D4	D5	D6	D7
3		D3	1 dc	1 dc	1 dc	1 dc	D4	D5	D6	D7

Table 3-7. Address/128-word Boundary Crossing Latency for 4 Dummy Cycles

Word										
0	4 dc	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	1 dc	D4	D5	D6	D7	D8
2		D2	D3	1 dc	1 dc	D4	D5	D6	D7	D8
3		D3	1 dc	1 dc	1 dc	D4	D5	D6	D7	D8

Table 3-8. Address/128-word Boundary Crossing Latency for 3 Dummy Cycles

Word										
0	3 dc	D0	D1	D2	D3	D4	D5	D6	D7	D8
1		D1	D2	D3	D4	D5	D6	D7	D8	D9
2		D2	D3	1 dc	D4	D5	D6	D7	D8	D9
3		D3	1 dc	1 dc	D4	D5	D6	D7	D8	D9

5-2-2. 8-, 16-Word Modes Linear Burst with Wrap Around

Fixed amount of data (8 or 16 words) is output from continuous address for the linear wrap around mode. (in the unit of words). The origin burst read address is decided by the group where the origin address falls. The definition of groups is as illustrated in Table 4 below.

Table 4. Burst Address Groups

Mode	Group Size	Group Address Ranges
8-word	8 words	0-7h, 8-Fh, 10-17h, 18-1Fh...
16-word	16 words	0-Fh, 10-1Fh, 20-2Fh, 30-3Fh...

5-2-3. Reading Memory Array

Read mode is the default state after a power-up or a reset operation.

An erase operation will be paused (after a time delay less than tESL) and the device will enter Erase-Suspended Read mode if the device receives an Erase Suspend command while in the Sector Erase state. While in the Erase-Suspended Read mode, data can be programmed or read from any sector which is not being erased. Reading from addresses within sector (s) being erased will only return the contents of the status register, which is the current status of the device.

If a program command is issued to any inactive (not currently being erased) sector during Erase-Suspended Read mode, the device will perform the program operation and automatically return to Erase-Suspended Read mode after the program operation completes successfully.

While in Erase-Suspended Read mode, an Erase Resume command must be issued by the system to reactivate the erase operation. The erase operation will resume from where it was suspended and will continue the operation until it completely finishes or another Erase Suspend command is received.

After the memory device completes an embedded operation (automatic Chip Erase, Sector Erase, or Program) successfully, it will automatically return to Read mode and data can be read from any address in the array. If the embedded operation fails to complete, as indicated by status register bit Q5 (exceeds time limitation flag) going HIGH during the operations, the system must perform a reset operation to set the device back to Read mode.

There are several situations requiring a reset operation to return to Read mode:

- A program or erase failure – can be indicated by status register bit Q5 going HIGH during the operation. Failures happened during the both operations will not cause the device automatically returning to Read mode.

- The device is in Auto Select, CFI mode or read configure register mode – All of the states will remain active until they are terminated by a reset operation.

In the two situations above, if a reset operation (either hardware reset or software reset command) is not performed, the device will not return to Read mode and the system will not be able to read array data.

5-3. Set Configuration Register Command Sequence

The burst mode parameter is set by the configuration register. The following modes are configured: Burst read mode, RDY configuration, synchronous mode active & number of dummy cycles. Before entering burst mode, the configuration register needs to be set. It's consisted of 4 cycles. Cycle 1 & 2: Unlock sequences. Cycle 3: Data D0h & address 555h. Cycle 4: Configuration code with address (000h). To reset the device to read or suspended read, a software reset command needs to be issued. The device's default state after power up or hardware reset is asynchronous read mode. Before entering synchronous mode, the register needs to be set. During bus operation, the register can not be modified.

5-3-1. Programmable Dummy Cycle

This feature is able to indicate the device the configurable period of time for the number of additional clock cycles. And then address data will be available after the time elapsed and AVD# is driven active.The dummy cycle will be set to default value after power up. The total number of dummy cycles is programmable from 3rd to 10th cycles. Refer to ***Section 5.3 Set Configuration Register Command Sequence*** in above section for more details.

5-3-2. Configurable Dummy Cycle

The Configurable Dummy Cycle settings can be decided by the input frequency of the device - The Configuration Bit (CR14–CR11) determines the setting. Refer to ***Table 5. Configurable Dummy Cycles vs. Frequency*** as below.

The certain number of cycles for original burst read is set by the dummy cycle command sequence. The clock frequency determines the number of dummy cycles configured.

NOTE: *After a power-up or hardware reset, the default setting of dummy cycle will be set to 10.*

In order to ensure the device is set as expected, it is recommended that dummy cycle command sequence should to be written even if the default dummy cycle value is desired. Default state can also be obtained by hardware reset.

Other setting not listed in the table above will be reserved as invalid.

If the setting CR[14:11] is not in legal setting as table listed, the device will output CR[14:11] to 0001 and RDY will be disasserted.

5-3-3. Burst Length Configuration

Three different burst read modes are supported: 8 & 16 word linear burst read with wrap around; continuous burst read. The device's default burst read is continuous read. It launches with starting address till the burst read ends. When reaches the highest address, it wraps around to the lowest address. The wrap around occurs in the 8 or 16 word boundary.

Table 5. Configurable Dummy Cycles vs. Frequency

CR [14:11]	Dummy Cycles	Freq Max (Mhz)
0001	3	25
0010	4	38
0011	5	50
0100	6	63
0101	7	75
0110	8	87
0111	9	98
1000	10	108

5-3-4. Burst Wrap Around

CR3 is set to "1" by default. When it changes to "0", the burst warp around mode is disabled.

5-3-5. Output Drive Strength

User may tune the strength of output driver from full strength to half strength depends on the configuration bit CR7.

The default setting is CR7=1; with full strength.

If CR7=0, the strength of output buffer will be reduced to half strength.

5-4. Program Operation

All three devices provide the ability to program the memory array in Word mode. As long as users enter the correct cycle defined in the ***Chapter 7. Command Definitions*** (including 2 unlock cycles and the A0H program command), word data provided on the data lines by the system will automatically be programmed into the array at the specified location.

After the program command sequence has been executed, the internal write state machine (WSM) automatically executes the algorithms and timings necessary for programming and verification, which includes generating suitable program pulses, checking cell threshold voltage margins, and repeating the program pulse if any cells do not pass verification or have low margins. The internal controller protects cells that do pass verification and margin tests from being over-programmed by inhibiting further program pulses to these passing cells as weaker cells continue to be programmed.

With the internal WSM automatically controlling the programming process, users only need to enter the program command and data once.

Programming will only change the bit status from "1" to "0". It is not possible to change the bit status from "0" to "1" by programming. This can only be done with an erase operation. Furthermore, the internal write verification only checks and detects errors in cases where a "1" is not successfully programmed to "0".

Any commands written to the device during programming will be ignored except hardware reset or program suspend. Hardware reset will terminate the program operation after a period of time not more than tPSL. When the program is complete or the program operation is terminated by a hardware reset, the device will return to Read mode. When program suspend is ready, the device will enter program suspend read mode.

After the embedded program operation has begun, users can check for completion by reading the following bits in the status register table below:

Status	Q7[*1]	Q6	Q5	Q1
In progress	Q7#	Toggling	0	0
Exceed Time Limit	Q7#	Toggling	1	N/A

NOTE: *DQ7 (Data# Polling bit) shows the status of on-going or completion for program and erase operations or in erase suspend mode.*

5-4-1. Programming Commands/Command Sequences

To perform a program operation, the system provides the desired address on the address pins, enables the chip by asserting CE# & WE# LOW & OE# to HIGH, and disables the Data (I/O) pins by holding OE# HIGH. To Latch address, AVD# needs to be asserted LOW. On 1st falling edge of WE#, address latched. On 1st rising edge of WE#, data latched.

Table2. Bus Operation on page 16, described the detail of the combinations.

To see an example of the implementation on waveform, please refer to **Figure 17. Program Operation Timings Waveform**. The system is not allowed to write invalid commands (commands not defined in this datasheet) to the device. Writing an invalid command may put the device in an undefined state.

5-4-2. Accelerated Program and Erase Operations

By applying high voltage (Vhv) to the ACC pin, the device will enter the Accelerated Programming mode. This mode permits the system to skip the normal command unlock sequences and program locations directly. During accelerated programming, the current drawn from the ACC pin is no more than ICP1.

5-4-3. Write Buffer Programming Operation

The devices program 32 words in a programming operation. To trigger the Write Buffer Programming, start with the first two unlock cycles, then third cycle writes the Write Buffer Load command at the predefined programming Sector Address. The fourth cycle writes the "word locations subtract one" number.

Following the above operations, system starts to write the mingling of address and data. After the programming of the first address or data, the "write-buffer-page" is selected. The following data should be within the above mentioned page. The "write-buffer-page" is selected by choosing address Amax-A5. "Write-Buffer-Page" address has to be the same for all address/data write into the write buffer. If not, operation will be aborted.

To program the content of the write buffer page this command must be followed by a write to buffer Program confirm command. The operation of write-buffer can be suspended or resumed by the standard commands, once the write buffer programming operation is finished, it will return to normal READ mode.

“Abort” will be executed for the Write Buffer Programming Sequence if the following conditions occurred:

- The value loaded is bigger than the page buffer size during "Number of Locations to Program"

- Address written in a sector is not the same as the one assigned during the Write-Buffer-Load command.

- Address/ Data pair written to a different write-buffer-page than the one assigned by the "Starting Address" during the "write buffer data loading" operation.

- Writing not "Confirm Command" after the assigned number of "data load" cycles.

At Write Buffer Abort mode, the status register will be Q1=1, Q7=DATA# (last address written), Q6=toggle, Q5=0. A Write-to-Buffer-Abort Reset command sequence has to be written to reset the device for the next operation.

Write buffer programming can be conducted in any sequence. However the CFI functions, Auto-select, Secured Silicon sectors are not functional when program operation is in progress. Multiple write buffer programming operations on the same write buffer address range without intervening erases is available. Any bit in a write buffer address range can not be programmed from 0 back to 1.

5-4-4. Write Buffer Programming Command Sequence

Write Buffer Programming Sequence is able to facilitate faster programming as compared to the standard Program Command Sequence.

See Table 7. and Figure 1. below for the program command sequence.

5-4-5. Buffer Write Abort

In the table below, Q1 is the indicator of Buffer Write Abort. When Q1=1, the device will abort from buffer write and go back to read status register:

Status	Q7	Q6	Q5	Q3	Q2	Q1
Buffer Write Busy	Q7#	Toggle	0	N/A	N/A	0
Buffer Write Abort	Q7#	Toggle	0	N/A	N/A	1
Buffer Write Exceeded Time Limit	Q7#	Toggle	1	N/A	N/A	0

Table 6. Write Buffer Command Sequence

Sequence	Command	Address	Data	Remarks
1	Unlock (1)	555	00AA	
2	Unlock (2)	2AA	0055	
3	Load Write Buffer	Start Address	0025h	
4	Indicate # of Program Locations	Start Address	Word Count	(# of locations) - 1
5	Load 1st word	Start Address	Write	Addresses need to be within write-buffer-page boundaries, but no need to be loaded in any order.
6-X	Load next word	Write Buffer Location	Write	Same as above
X+1	Load last word	Write Buffer Location	Write	Same as above
X+2	Write Buffer Program Confirm	Sector Address	0029h	This command must come after the last write buffer location loaded, or the operation will ABORT.
X+3	Device goes busy			
Last	Status monitoring through Q pins (Conduct Data Bar Polling on the Last Loaded Address)			

Figure 1. Write Buffer Programming Operation

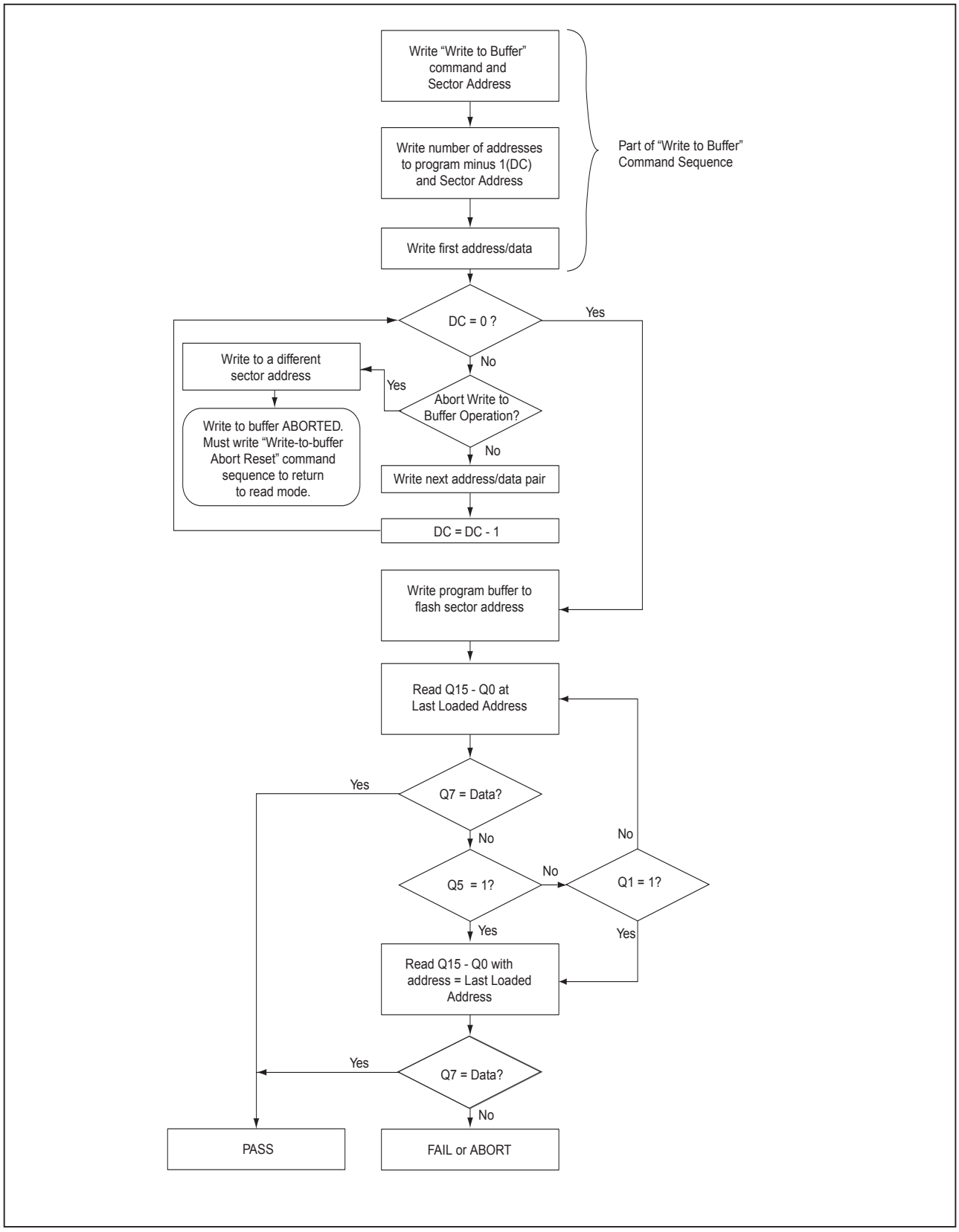
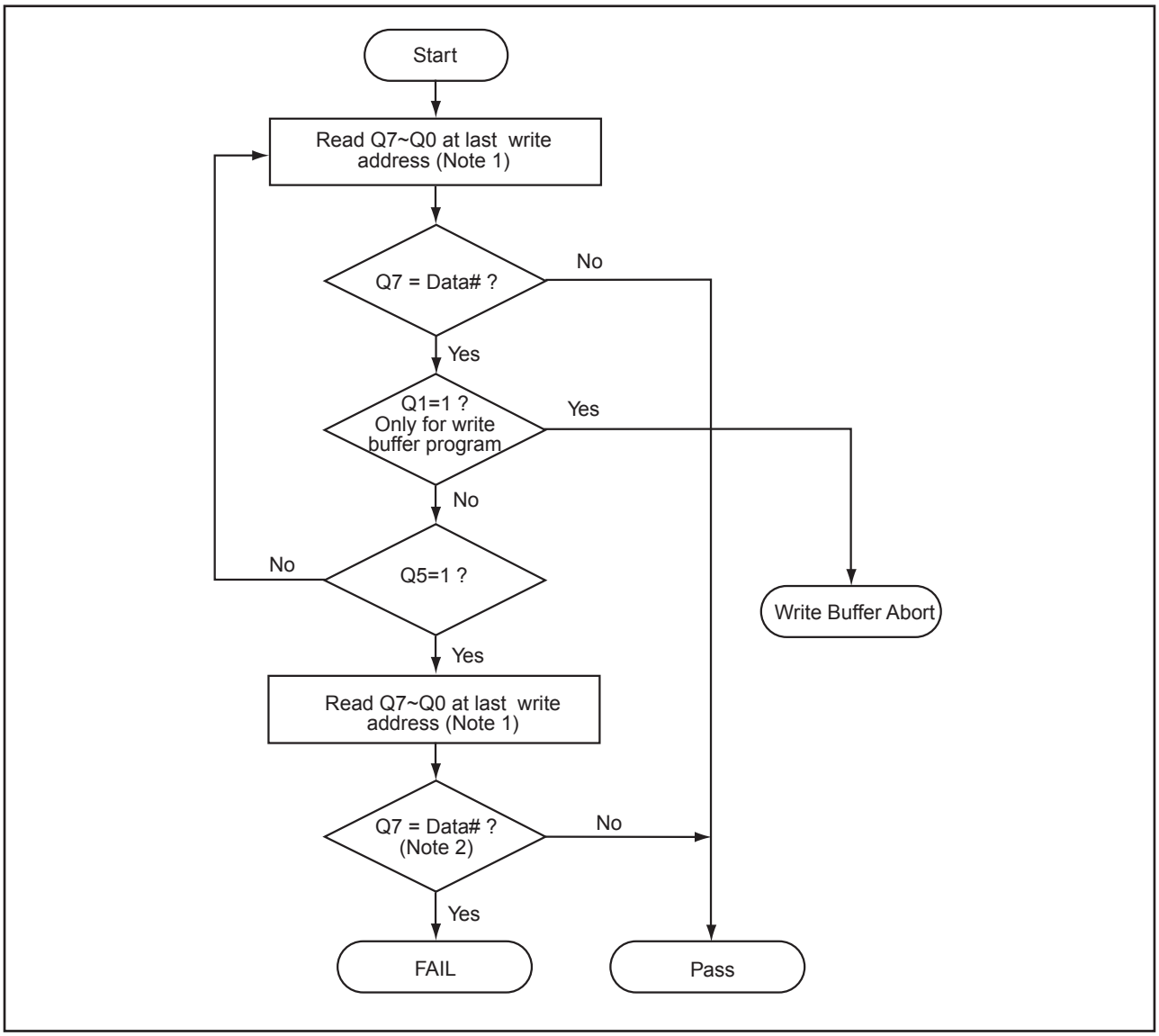


Figure 2. Status Polling For Write Buffer Program



NOTES:

1. *For programming, valid address means program address. For erasing, valid address means erase sectors address.*
2. *Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.*

5-5. Erase Operation

There are two types of erase operations performed on the memory array -- Sector Erase and Chip Erase. Sector Erase operation erases one selected sector.

Chip erase will not be conducted if any of the sectors is protected. It can be done after the sector is being un-protected.

5-5-1. Sector Erase

The sector erase operation is used to clear data within a sector by returning all the memory location to the “1” state. It requires six command cycles to initiate the erase operation.

The first two are "unlock cycles", the third is a configuration cycle, the fourth and fifth ones are also "unlock cycles", and the last cycle is the Sector Erase command. After the sector erase command sequence has been issued, the embedded sector erase operation will then begin.

After the embedded sector erase operation begins, all commands except Erase Suspend will be ignored. The only way to interrupt the operation is with an Erase Suspend command or with a hardware reset. The hardware reset will completely abort the operation and return the device to Read mode.

The system can determine the status of the embedded sector erase operation by the following methods:

Status	Q7	Q6	Q5	Q3	Q2
In progress	0	Toggling	0	NA	Toggling
Exceeded time limit	0	Toggling	1	NA	Toggling

NOTE:

Q2 is a localized indicator showing a specified sector is undergoing erase operation or not. Q2 toggles when user reads at addresses where the sectors are actively being erased (in erase mode) or to be erased (in erase suspend mode).

5-5-2. Chip Erase

The Chip Erase operation is used to erase all the data within the memory array. All memory cells containing a "0" will be returned to the erased state of "1". This operation requires 6 write cycles to initiate the action. The first two cycles are "unlock" cycles, the third is a configuration cycle, the fourth and fifth are also "unlock" cycles, and the sixth cycle initiates the chip erase operation.

During the chip erase operation, no other software commands will be accepted, but if a hardware reset is received or the working voltage is too low, that chip erase will be terminated. After Chip Erase operation completes, the chip will automatically return to Read mode. If any of the sectors is locked, chip erase will not start.

The system is able to determine the status of the embedded chip erase operation by the following methods:

Status	Q7	Q6	Q5	Q2
In progress	0	Toggling	0	Toggling
Exceed time limit	0	Toggling	1	Toggling

5-5-3. Sector Erase Command Sequence

There are six bus cycles in normal sector erase operation in normal mode. Sector erase command sequence is as follows: Write 2 unlock cycles --> Set-up command --> 2 more unlock cycles -->Address of sector to be erased --> sector erase command.

Erase operation doesn't require the pre-programming in advance. An all zero data pattern before erase initiation will come to pass for programming & verifying the device per the Erase. No controls or timing is needed during sector erase operation.

After the writing of command sequence, the erase operation will start.

Upon completion of the erase operation, the device's address will not be latched and returns to read status. When Embedded Erase operation is on-going, the device cannot be read.

When erase operation is engaged, only erase suspend can be conducted. A hardware reset will terminate the erase operation.

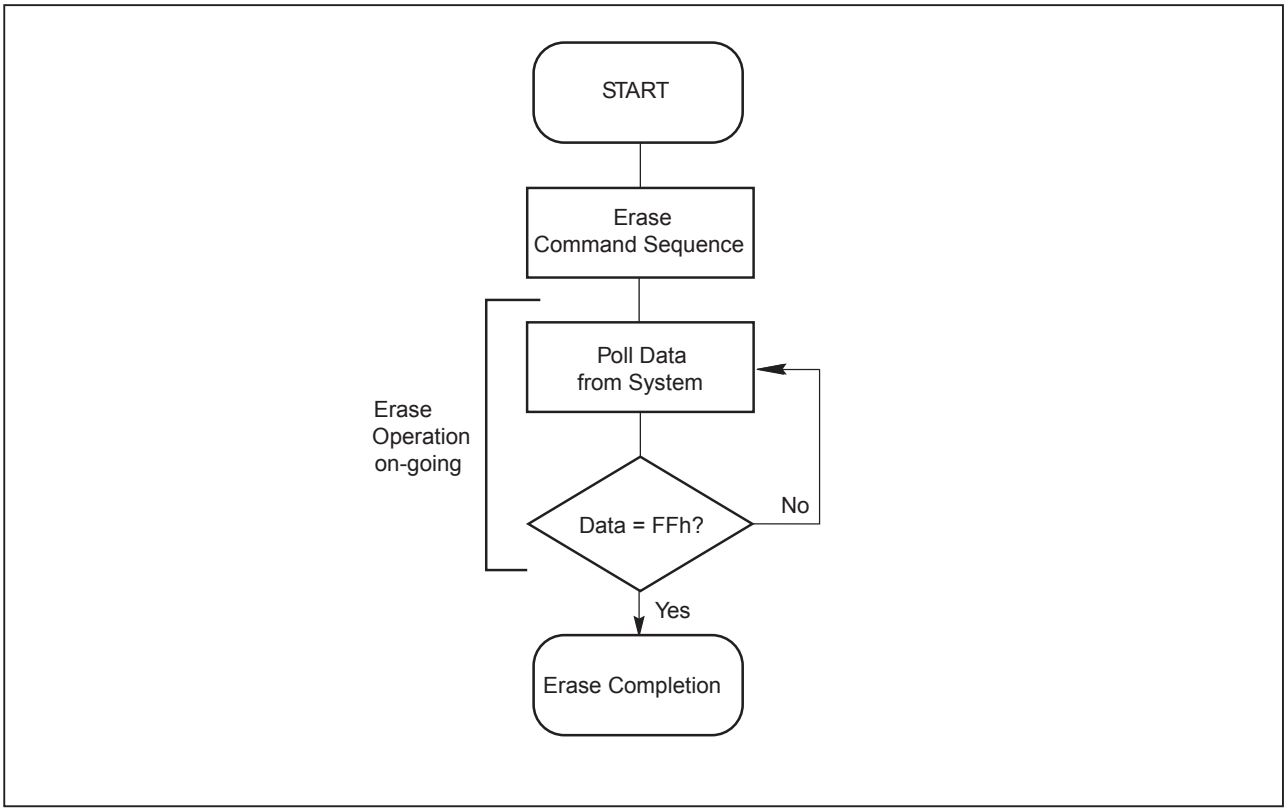
5-5-4. Accelerated Sector Erase

An accelerated erase function is provided to erase no more than 100 times per sector erase. ACC erase operation should be conducted in the range of 30C +/-10C. The ACC erase provides much faster erase operation compare with standard erase operations.

Operations below are needed prior to ACC sector erase operation:

1. Unlock the sectors should be erased with DPB before hand. Locked sectors can not be erased.
2. Vhv must be applied to ACC input at least 1 μs before executing step 3.
3. Chip erase command is issued.
4. Q2/Q6 or Q7 status bits should be monitored so to verify when erase operation is complete. This procedure is the same as in the standard erase operation.
5. ACC is lowered from Vhv to VCC.

Figure 3. Erase Operation



5-6. Program/Erase Operation Status

Program or erase operation status is disaplayed in the following status bits: Q2, Q3, Q5, Q6, and Q7. Descriptions of the bits is in the following tables & sections. Q6 and Q7 indicate if program or erase is finished or not.

Table 7. Program Operation Status

Status			Q7 (Note 2)	Q6	Q5 (Note 1)	Q3	Q2 (Note 2)	Q1 (Note 4)
Program Suspend Mode (Note 3)	Read from Program Suspended Sector		Invalid data will output from address under programming.					
	Read in Non-Program Suspended Sector		Data					
Standard Mode	Program		Q7#	Toggle	0	N/A	No Toggle	0
	Erase		0	Toggle	0	1	Toggle	N/A
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No Toggle	0	N/A	Toggle	N/A
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	Data
	Erase-Suspend-Program		Q7#	Toggle	0	N/A	N/A	N/A
Write to Buffer (Note 5)	BUSY		Q7#	Toggle	0	N/A	N/A	0
	Exceeded Timing Limits		Q7#	Toggle	1	N/A	N/A	0
	ABORT		Q7#	Toggle	0	N/A	N/A	1

Legend: T - Toggle; NT - No toggle.

NOTES:

1. *When embedded program/erase exceed max. time limit, Q5 changes to "1".*
2. *A valid address is needed for reading status info from Q7 & Q2.*
3. *When program is suspended, output data is invalid.*
4. *During write buffer program, Q1 indicates the write to buffer abort status.*
5. *During write buffer program, data-bar polling algorithm needs to be conducted. Data-bar of Q7 shows the last address loaded for write buffer.*

5-7. Program/Erase Suspend/Resume

5-7-1. Program Suspend

After a program operation begins, Program Suspend is the only valid command that can be issued. The system will determine if the device has entered the Program-Suspended Read mode through Q6.

After the device has entered Program-Suspended mode, the system can read any sector (s) except that being programmed by the suspended program operation. Reading the array being program suspended is invalid. Whenever a suspend command is issued, user must issue a resume command and check Q6 toggle bit status, before issue another program command. The system can use the Status Register bits shown in **Table 7** to determine the current state of the device:

When the device is Program/Erase suspended, user is allowed to execute read array, Auto Select, read CFI, read security silicon commands.

5-7-2. Program Resume

The Program Resume command is valid only when the device is in Program-Suspended mode. After program resumes, users are allowed to issue another Program Suspend command, but there should be a 25us interval between Program Resume and the next Program Suspend command.

5-7-3. Program Suspend/Program Resume Commands

The Program suspend command is for pausing the "Write to Buffer" operation.

The Program suspend operation is as follows: Issuing Programming Suspend Command --> Device's programming operation suspended paused within tPSL; Status Bits updated; Address defined --> Data to be read from non-suspended sectors.

Note that when an erase suspend is in operation, program suspend can also be conducted, data can then be read from non-suspended sectors.

If read from OTP sectors needed, it needs to exit the region with proper command sequences.

Auto Select code can also be read from suspended sectors. When exit from Auto select mode, it returns to suspend mode.

For Program Resume, it operates as thus: Issuing Program Resume command --> Device resumes programming (Status to be checked by Status bit Q7 or Q6)

It must exit the suspend by issuing resume command. After programming being resumed, another program suspend can be issued.

NOTE: *While a program operation is suspended and resumed more than once, a minimum delay of tPRS (Program Resume to Program Suspend) is required between next resume and suspend command.*

5-7-4. Erase Suspend

After a sector erase operation begins, Erase Suspend is the only valid command that can be issued. If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended Read mode until tESL has elapsed. The system is able to determine if the device has entered the Erase-Suspended Read mode through Q6 and Q7.

After the device has entered Erase-Suspended Read mode, the system can read or program any sector (s) except that being erased by the suspended erase operation. Reading any sector being erased or programmed will return the contents of the status register. Whenever a suspend command is issued, users must issue a resume command and check Q6 toggle bit status, before issue another erase command.

When the device reads from a erase suspended sector during burst read mode, the burst read operation will stop and RDY will be disabled when crossing the boundary to the suspended sector. User may restart the burst operation by issuing new address and AVD# pulse.

The system is able to use the status register bits shown in the following table to determine the current state of the device:

Status	Q7	Q6	Q5	Q3	Q2	Q1
Erase suspend read in erase suspended sector	1	No toggle	0	N/A	Toggle	N/A
Erase suspend read in non-erase suspended sector	Data	Data	Data	Data	Data	Data
Erase suspend program in non-erase suspended sector	Q7#	Toggle	0	N/A	N/A	N/A

5-7-5. Sector Erase Resume

The Sector Erase Resume command is valid only when the device is in Erase-Suspended Read mode. After erase operation resumes, users can issue another Erase Suspend command, but there should be a 400us interval between Erase Resume and the next Erase Suspend command.

Figure 4. Data# Polling Timing Waveforms (During Embedded Algorithms)

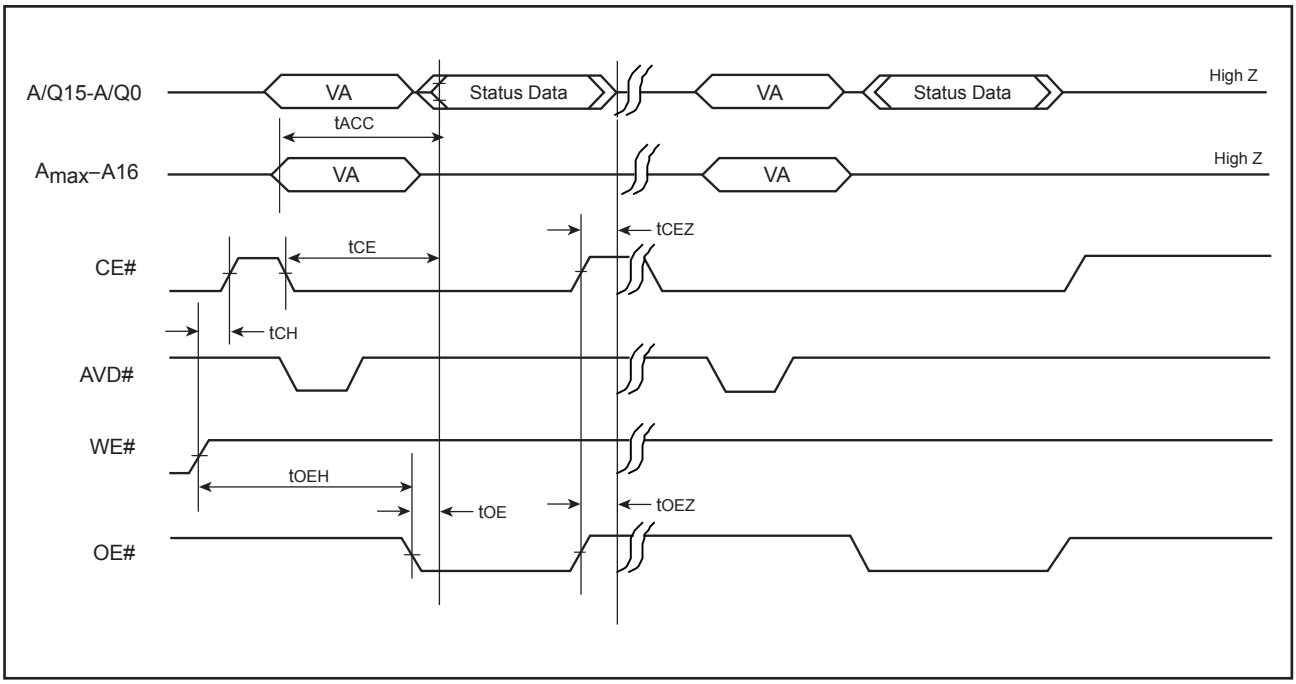


Figure 5. Data# Polling For Word Program/Erase

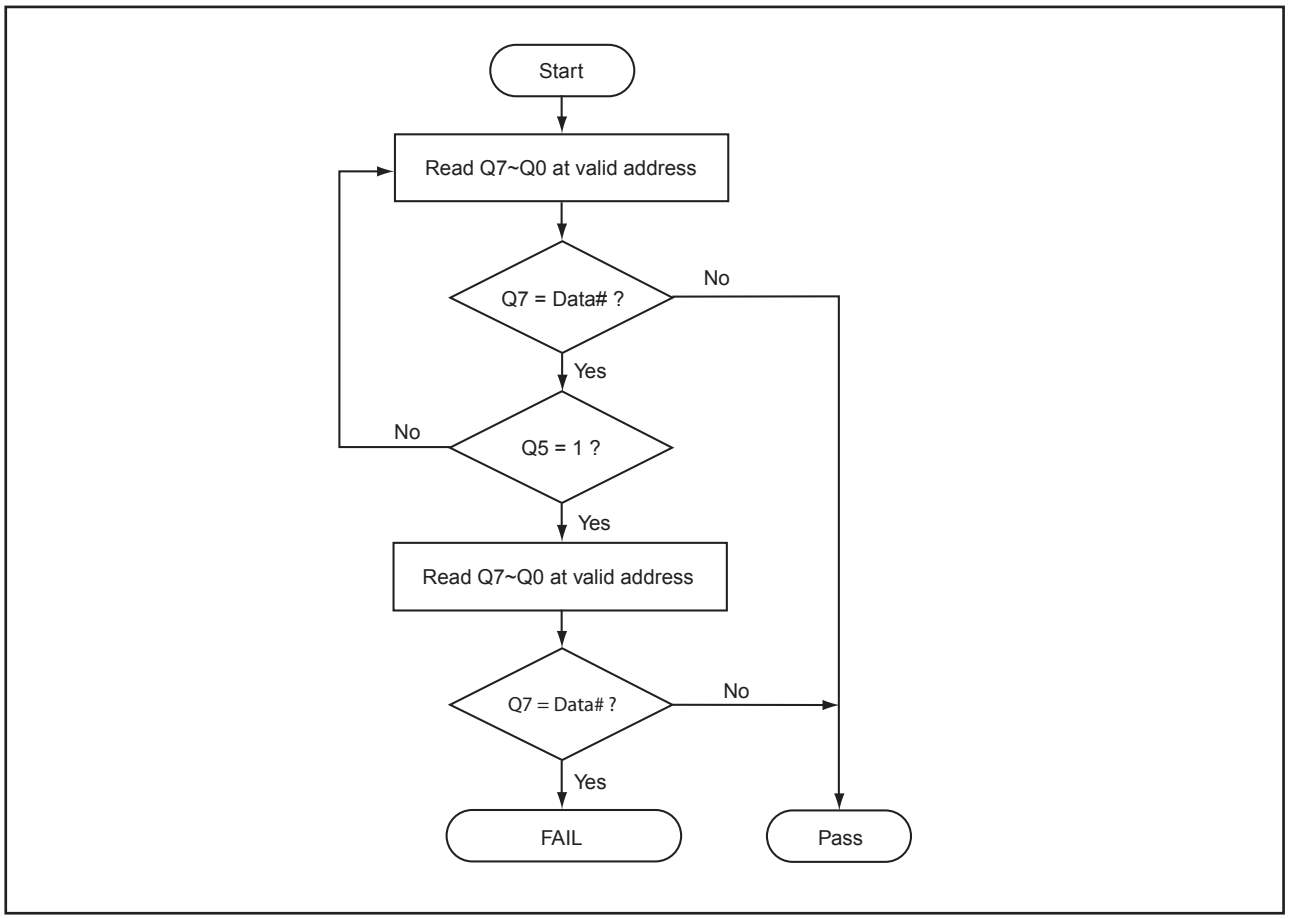


Figure 6. Toggle Bit Timing Waveforms (During Embedded Algorithms)

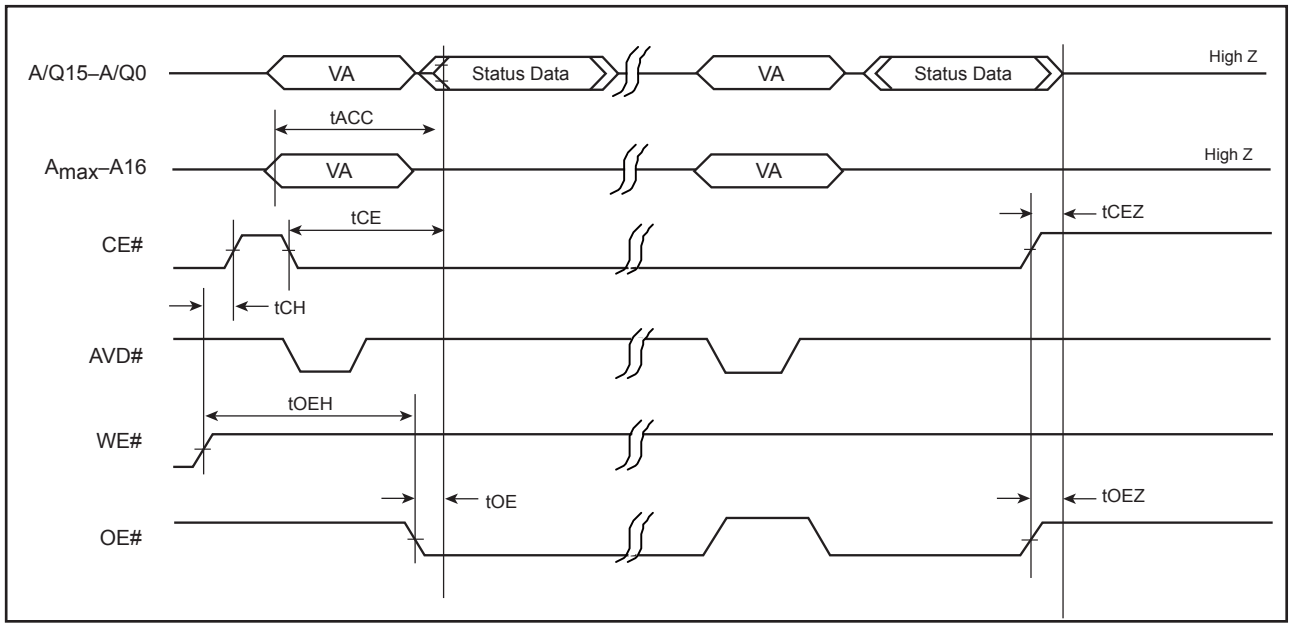
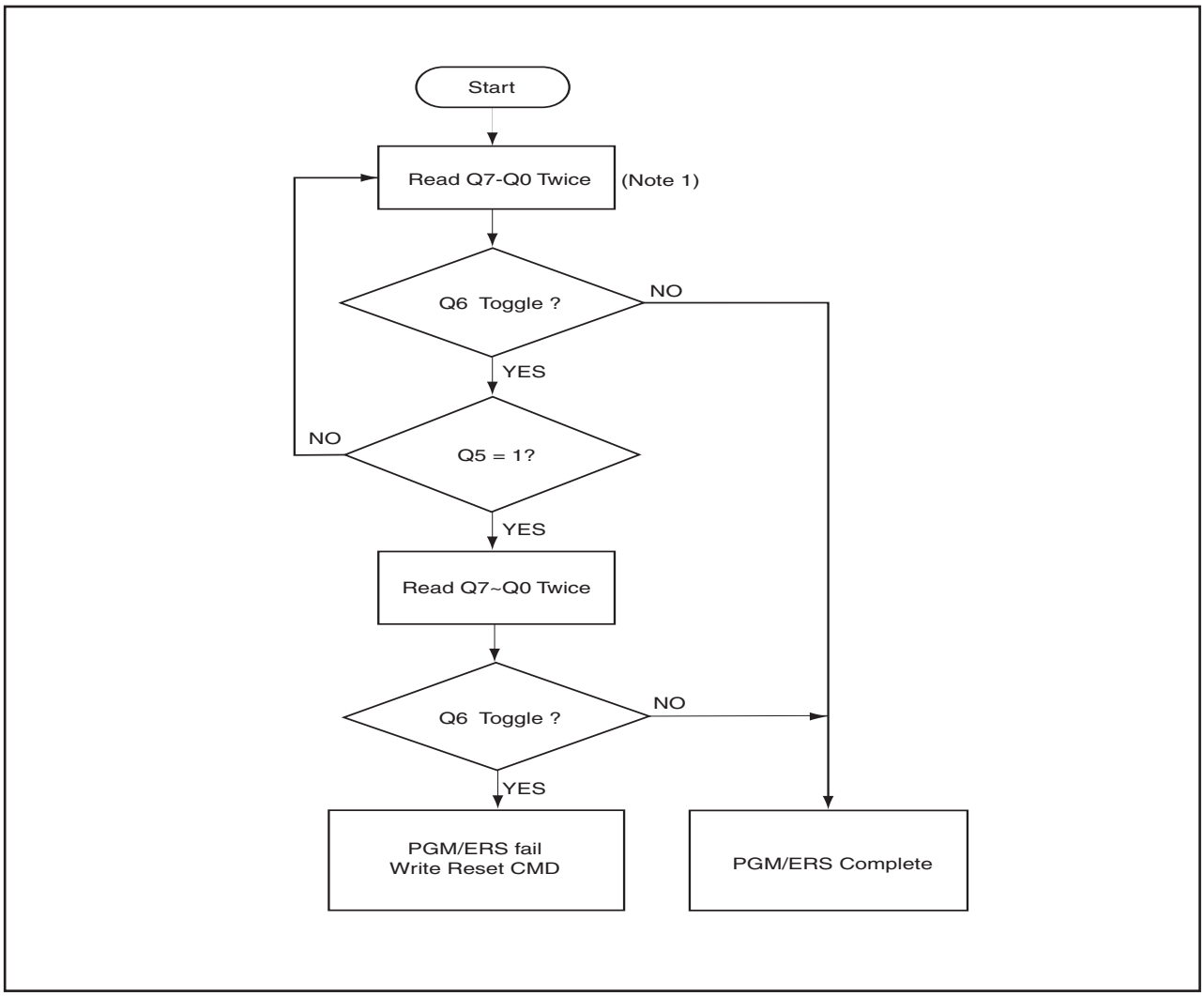


Figure 7. Toggle Bit Algorithm



NOTES:

1. Read toggle bit twice to determine whether or not it is toggling.

2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

5-8. Configuration Register

A configuration register is used to set the various burst parameters: number of dummy cycles, burst read mode, burst length, RDY configuration, and synchronous mode active.

The **Configuration Register Table** displays the address bits of configuration register settings represent various device functions.

Table 8. Configuration Register

Function	CR Bit	Settings (Binary)
Reserved	CR15	0 = Default
Programmable Dummy Cycles	CR14	0000 = Reserved 0001 = Data is valid on the 3rd active CLK rising edge (Default Value) 0010 = Data is valid on the 4th active CLK rising edge 0011 = Data is valid on the 5th active CLK rising edge
	CR13	0100 = Data is valid on the 6th active CLK rising edge 0101 = Data is valid on the 7th active CLK rising edge 0110 = Data is valid on the 8th active CLK rising edge 0111 = Data is valid on the 9th active CLK rising edge
	CR12	1000 = data is valid on the 10th active CLK rising edge 1001 = Reserved 1010 = Reserved 1011 = Reserved
	CR11	1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved
RDY Polarity	CR10	0 = RDY signal is active low 1 = RDY signal is active high (default)
Reserved	CR9	1 = Default
RDY	CR8	0 = RDY active one clock cycle before data 1 = RDY active with data (Default)
Driver Strength	CR7	1 = Full driver strength (Default) 0=Half driver strength
Reserved	CR6	1 = Default
Reserved	CR5	0 = Default
Reserved	CR4	0 = Default
Burst Wrap Around	CR3	0 = No Wrap Around Burst 1 = Wrap Around Burst (Default)
Burst Length	CR2	000 = Continuous (Default) 010 = 8-Word Linear Burst 011 = 16-Word Linear Burst (All other bit settings are reserved)
	CR1	
	CR0	

***NOTES**:*

1. *RDY Configuration - MX29NS320/640/128E are all able to set RDY to output VOH with valid data by default. RDY goes active one data cycle ahead of the active data. CR8 sets to "1" for RDY being active; "0" for RDY being active one cycle ahead of the valid data to be output.*

2. *RDY Polarity - All devices have this default setting to indicate if the system is ready for CR10 to set to "1" when RDY is high. Set to "0" will set RDY to low. When RDY is low, RDY shows the device is ready.*

5-9. Enter/Exit Secured Silicon Sector Command Sequence

A 8-word, random ESN (Electronic Serial Number) is in the Secured Silicon Sector region. The operation of this region is thus: 3-cycle command to enter the region --> Access of the region --> 4-cycle command to exit the region --> Return to normal operation

Not the Secured Silicon Region cannot be accessed when program/erase is in operation.

In the Secured Silicon Sector region, 128-word region is factory locked, while the other 128-word region is customer locked.

5-9-1. Program Secured Silicon Sector Command Sequence

Programming Secured Silicon is a two-cycle command. It is initiated by A0h command followed by program address with program data. The program operation then starts.

The system can monitor Q7 or Q2/Q6 to check the status of the embedded operation as the system does when programming the normal array.

Programming the Secured Silicon will only change the bit status from “1” to “0”. It is not possible to change the bit status from “0” to “1” by programming. Furthermore, the internal write verification only checks and detects errors in case where a ”1” is not successfully programmed to “0”.

When program is complete, the device then returns to Read Secured Silicon Sector mode.

If embedded program exceeds max. time limit (a failure occurs), Q5 changes to “1” and Q6 keeps toggling. Under this condition, a soft ware reset command is needed and the device returns to Read Secured Silicon Sector mode.

5-10. Auto Select Operations

Users are allowed to issue the Auto Select command (two unlock cycles followed by the Auto Select command 90H) to enter Auto Select mode when the device is in either:

After entering Auto Select mode, user can query the following status multiple times without issuing a new Auto Select command:

1. *Manufacturer ID*
2. *Device ID*
3. *Security Sector locked status*
4. *Sector protected status*

While In Auto Select mode, issuing a Reset command (F0H) will return the device to one of the following modes:

- *Read mode*
- *Erase-Suspended Read mode (if Erase-Suspend is active)*
- *Program Suspended Read mode (if Program Suspend is active).*

NOTE: *After entering Auto Select mode, no other commands are allowed except the reset command.*

5-10-1. Auto Select Command Sequence

The Auto Select mode has four command cycles. The first two are unlock cycles, and followed by a specific command. The fourth cycle is a normal read cycle, and user can read at any address any number of times without entering another command sequence. The Reset command is necessary to exit the Auto Select mode and back to reading memory array. The following table shows the identification code with corresponding address.

		Address	Data (Hex)
Manufacturer ID		**X00**	**C2**
Device ID	MX29NS640E	X01/0E/0F	2B7E/2B33/2B00
Device ID	MX29NS320E	X01/0E/0F	2A7E/2A31/2A00
Device ID	MX29NS128E	X01/0E/0F	2C7E/2C35/2C00
Sector Protect Verify		(Sector address) X02	00/01
Secured Silicon		X07	Q0-Q2 = Reserved Q4 & Q3 - WP# Protections Boot Code 01 = WP# Protects only the Top Boot Sectors Q5 Handshake Bit 0 = Handshake, 1 = Reserved Q6 - Customer Lock Bit 0 = Un-Locked, 1 = Locked, Q7 - Factory Lock Bit 0 = Un-Locked, 1 = Locked Q8 - Q15 = Reserved

NOTE: *After entering Auto Select mode, no other commands are allowed except the reset command.*

5-11. Handshaking Feature

By conducting the host to detect the Ready (RDY) signal, the handshaking feature enables the system to decide when the initial burst data is ready.

The operation is as thus: Configure the # of dummy cycle by Configuration Register --> CE# goes low --> Rising edge of RDY indicates the initial burst word data indicated

The Burst read may be optimized by configuring the setting the number of dummy cycle per clock frequency.

The Auto Select Function helps the host to see if the device is ready for handshaking operation.

Table 9. Dummy Cycles for Handshaking

Clock Cycles after AVD# Low (Typical No.)	Address Issuing Condition
108 MHz	
10	Initial address (VI/O = 1.8 V)

6. SECURITY FEATURES

This device is able to provide security protection features to prevent unintentional program or erase operations.

6-1. Lock Register

A Lock Register allows the Secured Silicon Sector Protection to be configured or not.

6-1-1. Lock Register Bits

User can choose if Q0 = 1 with default OTP or Q0 = 0 to lock Secured Silicon Sector.

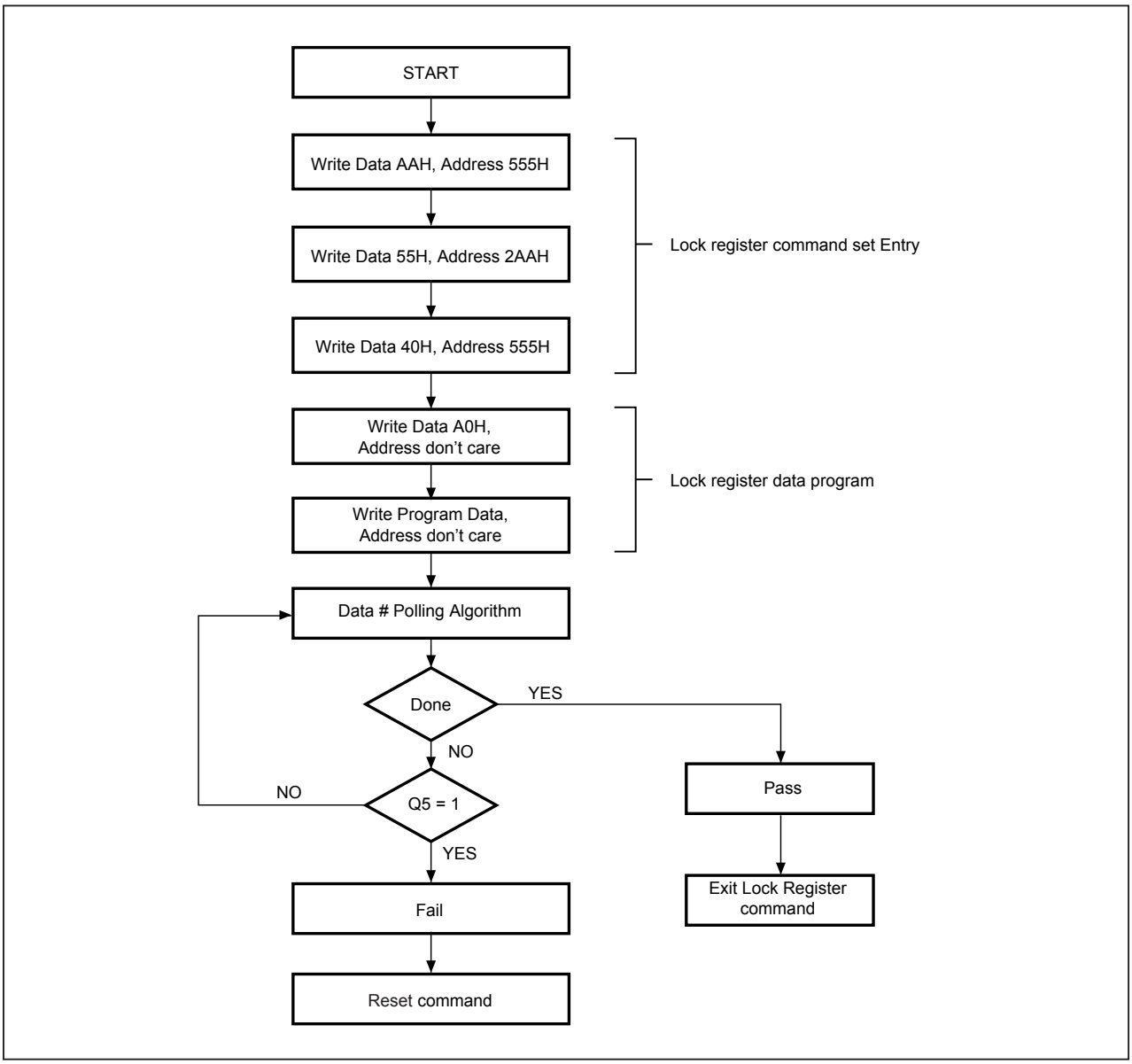
After the Lock Register Bits Command Set Entry command sequence is issued, the read and write operations for normal sectors are disabled until this mode exits.

Table 10. Lock Register bits

Q15-Q1	Q0
Don't care	Secured Silicon Sector Protection Bit

Please refer to the command for Lock Register command set to read and program the Lock register.

Figure 8. Lock Register Program Algorithm



6-1-2. Dynamic Write Protection Bits (DPBS)

The Dynamic Protection allows the software application to easily protect sectors against inadvertent change. However, the protection can be easily disabled when changes are necessary.

All Dynamic Protection bit (DPB) are volatile and assigned to each sector. It can be modify individual.To modify the DPB status by issuing the DPB Set (programmed to “0”) or DPB Clear (erased to “1”) commands, then placing each sector in the protected or unprotected state separately. The DPBs are set as protected by default.

6-2. Hardware Data Protection Mode

Two types of hardware protections is provided:

1. WP# low protects the top two sectors.
2. ACC low protects all sectors.

NOTES:

1. *Q0~Q15 are input (DIN) or output (DOUT) pins according to the requests of command sequence, sector protection, or data polling algorithm.*
2. *In Word Mode, the addresses are AM to A0, AM: MSB of address.*

6-2-1. Write Protect (WP#)

The hardware protection provided by WP# is by asserting the WP# to low. After WP# goes low, the upper two sectors will be protected. The erase & program function in these two sectors are disabled after WP# protection enabled. The WP# protection will override the software protection method.

When WP# is asserted high, software protection mode determines which array to protect.

6-2-2. WP# Boot Sector Protection

The WP# should be asserted low on the last cycle of program or erase command so it can protect the top two sectors. (4th cycle in program; 6th cycle in erase).

NOTE: *The WP# should not be left floating or unconnected; or it may cause inconsistent behavior of the device.*

6-3. Security Sector Flash Memory Region

The Security Sector region is an extra OTP memory space of 256 words in length. The security sector can be locked upon shipping from factory, or it can be locked by customer after shipping. Customer can issue Security Sector Factory Protect Verify and/or Security Sector Protect Verify to query the lock status of the device.

In factory-locked device, security sector region is protected when shipped from factory and the security silicon sector indicator bit is set to "1". In customer lockable device, security sector region is unprotected when shipped from factory and the security silicon indicator bit is set to "0".

6-3-1. Factory Locked: Security Sector Programmed and Protected at the Factory

In a factory-locked device, the Security Sector is permanently locked before shipping from the factory. The device will have a 8-word ESN in the security region. The ESN occupies 00000h to 00007h in word mode.

Secured Silicon Sector Address Range	Standard Factory Locked	Express Flash Factory Locked
000000h-00007Fh	ESN	Factory lock
000080h-0000FFh	Unavailable	Determined by Customer

6-3-2. Customer Lockable: Security Sector NOT Programmed or Protected at the Factory

When the security feature is not required, the security region can act as an extra memory space.

Security silicon sector can also be protected by two methods. Note that once the security silicon sector is protected, there is no way to unprotect the security silicon sector and the content of it can no longer be altered.

After the security silicon is locked and verified, system must write Exit Security Sector Region, go through a power cycle, or issue a hardware reset to return the device to read normal array mode.

7. COMMAND DEFINITIONS

Command Definitions Tables shows the address and data requirements for both command sequences.

Command		Asyn. Read	Reset Mode	Automatic Select			
				Manuf. ID	Device ID	Indicator Bits	Sector Protect Verify
Cycles	**1**	**1**	**1**	**4**	**6**	**4**	**4**
1st Bus Cycle	Addr	RA	XXX	555	555	555	555
	Data	RD	F0	AA	AA	AA	AA
2nd Bus Cycle	Addr			2AA	2AA	2AA	2AA
	Data			55	55	55	55
3rd Bus Cycle	Addr			555	555	555	555
	Data			90	90	90	90
4th Bus Cycle	Addr			X00	X01	07	02
	Data			C2	ID1	Data	Data
5th Bus Cycle	Addr				X0E		
	Data				ID2		
6th Bus Cycle	Addr				X0F		
	Data				ID3		

Command		CFI	Program	Program to Buffer	Program Buffer to Flash	Program to Buffer Abort Reset	Chip Erase	Sector Erase	Program/ Erase Suspend	Program/ Erase Resume	Set Config. Register	Read Config. Register
Cycles		1	4	6	1	3	6	6	1	1	4	4
1st Bus Cycle	Addr	55	555	555	SA	555	555	555	XXX	XXX	555	555
	Data	98	AA	AA	29	AA	AA	AA	B0	30	AA	AA
2nd Bus Cycle	Addr		2AA	2AA		2AA	2AA	2AA			2AA	2AA
	Data		55	55		55	55	55			55	55
3rd Bus Cycle	Addr		555	SA		555	555	555			555	555
	Data		A0	25		F0	80	80			D0	C6
4th Bus Cycle	Addr		PA	SA			555	555			X00	XX
	Data		PD	WC			AA	AA			CR	CR
5th Bus Cycle	Addr			PA			2AA	2AA				
	Data			PD			55	55				
6th Bus Cycle	Addr			WBL			555	SA				
	Data			PD			10	30				

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

PD(0) = Secured Silicon Sector Lock Bit. PD(0), or bit[0].

PD(1) = Persistent Protection Mode Lock Bit. PD(1), or bit[1], must be set to '0' for protection while PD(2), bit[2] must be left as '1'.

PD(2) = Password Protection Mode Lock Bit. PD(2), or bit[2], must be set to '0' for protection while PD(1), bit[1] must be left as '1'.

PD(3) = Protection Mode OTP Bit. PD(3) or bit[3].

Command Sequence		Deep Power Down		Lock		
		Enter	Exit	Lock Register Command Set Entry	Lock Register Bit Program	Lock Register Command Set Exit
Cycles		Word	Word	**3**	**2**	**2**
1st Bus Cycle	Addr	555	XXX	555	XXX	XX
	Data	AA	AB	AA	A0	90
2nd Bus Cycle	Addr	2AA		2AA	00	XX
	Data	55		55	Data	00
3rd Bus Cycle	Addr	XXX		555		
	Data	B9		40		
4thBus Cycle	Addr					
	Data					
5th Bus Cycle	Addr					
	Data					
6th Bus Cycle	Addr					
	Data					
7th Bus Cycle	Addr					
	Data					

Command Sequence		Secured Silicon Sector				Dynamic Protection Bits				
		Sector Entry	Sector Program	Sector Read	Sector Exit	Command Set Entry	DPB Set	DPB Clear	DPB Status Read	Command Set Exit
Cycles		3	2	1	4	3	2	2	1	2
1st Bus Cycle	Addr	555	XX	RA	555	555	XX	XX	SA	XX
	Data	AA	A0	Data	AA	AA	A0	A0	RD(0)	90
2nd Bus Cycle	Addr	2AA	PA		2AA	2AA	SA	SA		XX
	Data	55	Data		55	55	00	01		00
3rd Bus Cycle	Addr	555			555	555				
	Data	88			90	E0				
4th Bus Cycle	Addr				XX					
	Data				00					
5th Bus Cycle	Addr									
	Data									

SA = Address of the sector to be verified (in autoselect mode) or erased.
Address bits Amax - A13 uniquely select any sector.

RD(0) = Q0 protection indicator bit. If protected, Q0 = 0, if unprotected, Q0 = 1.
RD(1) = Q1 protection indicator bit. If protected, Q1 = 0, if unprotected, Q1 = 1.
RD(2) = Q2 protection indicator bit. If protected, Q2 = 0, if unprotected, Q2 = 1.
RD(4) = Q4 protection indicator bit. If protected, Q4 = 0, if unprotected, Q4 = 1.
WBL = Write Buffer Location. Address must be within the same write buffer page as PA.
WC = Word Count. Number of write buffer locations to load minus 1.

NOTE: *It is not recommended to adopt any other code not in the command definition table which will potentially enter the hidden mode.*

8. ENERGY SAVING MODE

8-1. Standby Mode

The device enters Standby mode whenever the RESET# and CE# pins are both held High except in the embedded mode. While in this mode, WE# and OE# will be ignored, all Data Output pins will be in a high impedance state, and the device will draw minimal (ICC3) current.

8-2. Automatic Sleep Mode

Automatic Sleep mode is able to minimize power consumption of flash device. The device automatically enters this mode when the addresses and clock stays stable for tACC + 20 ns. The automatic sleep mode will not be influenced by the CE#, WE#, and OE# control signals. Standard address access timings are responsible for offering new data when addresses are changed.

Output data will be always available to the system and latched in sleep mode.

ICC6 in the **Table 11. DC Characteristics** indicates the current specifications for Automatic Sleep mode.

Table 11. DC Characteristics

Parameter	Description	Test Conditions		Min	Typ	Max	Unit
ILI	Input Leakage Current	VIN = VSS to VCC, VCC = VCC max				±1	uA
ILO	Output Leakage Current	VOUT = VSS to VCC, VCC = VCC max				±1	uA
ILHV	High Voltage Pin Leakage Current	VIN=Vhv, VCC=VCC max				35	uA
ICCB	VCC Active Burst Read Current	CE# = VIL, OE# = VIL, burst length = 8	108 MHz		26	33	mA
		CE# = VIL, OE# = VIL, burst length = 16	108 MHz		26	35	mA
		CE# = VIL, OE# = VIL, burst length = continuous	108 MHz		30	39	mA
ICC1	VCC Active Asynchronous Read Current	CE# = VIL, OE# = VIH	5 MHz		15	18	mA
			1 MHz		3	4	mA
ICC2	VCC Active Write Current	CE# = VIL, OE# = VIH, ACC = VIH			20	60	mA
ICC3	VCC Standby Current	CE# = VIH, RESET# = VIH (Note 8)			40	100	uA
ICC4	VCC Reset Current	RESET# = VIL, CLK = VIL (Note 8)			80	150	uA
ICC6	VCC Sleep Current	CE# = VIL, OE# = VIH			40	100	uA
IDPD	Vcc Deep Power Down Current				10	50	uA
IPPW	Accelerated Program Current	ACC = Vhv			20	30	mA
IPPE	Accelerated Erase Current	ACC = Vhv			20	30	mA
VIL	Input Low Voltage			-0.1		0.3xVI/O	V
VIH	Input High Voltage			0.7xVI/O		VI/O+0.3	V
VOL	Output Low Voltage	IOL = 100 uA, VCC = VCC min				0.45	V
VOH	Output High Voltage	IOH = –100 uA, VCC = VCC min		0.85x VI/O			V
Vhv	Very High Voltage for Auto Select/Accelerated Program			9.5		10.5	V
VLKO	Low VCC Lock-out Voltage			1.0		1.4	V

NOTE: *Not 100% tested in production.*

8-3. Reset Commands

Executing the Reset command is able to reset the device to the Read or Erase-Suspend-Read mode. For this command, address bits are don't care.

The reset command can be written between the sequence cycles of an erase command and before the erase operation begins. It resets the device back to read mode. As soon as erase operation begins, the reset command will be ignored until it is complete.

The reset command can be written between the sequence cycles of an program command and before a program operation begins. It resets the device back to read mode. If the program command sequence is written when in the Erase Suspend mode, writing the reset command will return the device to the erase-suspend-read mode. As soon as program operation begins, the reset command will be ignored until it is complete.

The reset command can be written between the sequence cycles in Auto Select command sequence. It resets the device back to read mode when in Auto Select mode. Writing the reset command will cause the device return to the erase-suspend-read mode if the device enters the Auto Select mode while it is in Erase Suspend mode.

During a program or erase operation, if Q5 goes high, writing the reset command will either:

1. Return to read mode
2. Returns to erase-suspend-read mode (if the device was in Erase Suspend)

***NOTE**: The system must write the "Write to Buffer Abort Reset" command sequence to reset the device to read mode if Q1 goes high during a Write Buffer Programming operation. The standard reset command will not function.*

8-3-1. Hardware Reset

Driving the RESET# pin LOW for a period of Trp or more will return the device to Read mode. If the device is in the process of a program or erase operation, the reset operation will take at most a period of Tready1 before the device returns to Read mode.

When the RESET# pin is held at GND±0.3V, the device only consumes standby (Isbr) current. However, the device draws larger current if the RESET# pin is held at a voltage greater than GND+0.3V and less than or equal to Vil.

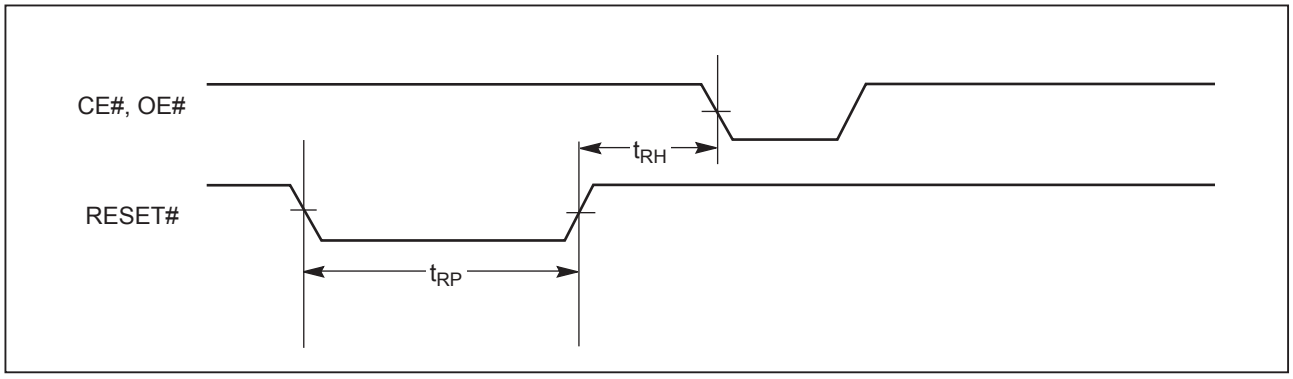
It is recommended to tie the system reset signal to the RESET# pin of the flash memory. This allows the device to be reset with the system and puts it in a state where the system can immediately begin reading boot code from it.

Table 12. Hardware Reset

Parameter	Description		Speed	Unit
tRP	RESET# Waveform Width	RESET at Embedded Program / Erase Operation	25	us
		RESET at Read Operation	5	us
tRH	Reset High Time Before Read		200	ns

***NOTE**: Not 100% tested.*

Figure 9. Reset Timings



8-3-2. Software Reset

Software reset is one of command in the command set **(See Chapter 7. Command Definitions**) that is able to returns the device to read array memory after reset. It must be used under the following conditions:

1. Exit from the Autoselect mode.
2. Erase or program cycle is not complete successfully that status bit Q5 goes high during write procedure.
3. Return to erase-suspend-read mode if the device was previously in Erase Suspend mode.
4. Return to initial state after any aborted operations.
5. Exit read configuration registration mode.
6. Exit CFI mode.

9. COMMON FLASH MEMORY INTERFACE (CFI) MODE

The device features CFI mode. Host system can retrieve the operating characteristics, structure and vendor-specified information such as identifying information, memory size, byte/word configuration, operating voltages and timing information of this device by CFI mode. If the system writes the CFI Query command "98h", to address "55h", the device will enter the CFI Query Mode. The system can read CFI information at the addresses given in **Table 13.**

Once user enters CFI query mode, users are allowed to issue reset command to exit CFI mode and return to read array mode.

Table 13-1. CFI Mode: Identification Data Values

Description	Address (h) (Word Mode)	Data (h)
Query-unique ASCII string "QRY"	10	0051h
	11	0052h
	12	0059h
Primary vendor command set and control interface ID code	13	0002h
	14	0000h
Address for primary algorithm extended query table	15	0040h
	16	0000h
Alternate vendor command set and control interface ID code	17	0000h
	18	0000h
Address for alternate algorithm extended query table	19	0000h
	1A	0000h

Table 13-2. CFI Mode: System Interface Data Values

Description	Address (h) (Word Mode)	Data (h)
VCC Min. (program/erase) D7–D4: volt, D3–D0: 100 millivolt	1Bh	0017h
VCC Max. (program/erase) D7–D4: volt, D3–D0: 100 millivolt	1Ch	0019h
ACC Min. voltage (00h = no ACC pin present) Refer to 4Dh	1Dh	0000h
ACC Max. voltage (00h = no ACC pin present) Refer to 4Eh	1Eh	0000h
Typical timeout per single word write 2^N us	1Fh	0004h
Typical timeout for Min. size buffer write 2^N us (00h = not supported)	20h	0008h
Typical timeout per individual block erase 2^N ms	21h	0009h
Typical timeout for full chip erase 2^N ms (00h = not supported)	22h	0010h
Max. timeout for word write 2^N times typical	23h	0005h
Max. timeout for buffer write 2^N times typical	24h	0002h
Max. timeout per individual block erase 2^N times typical	25h	0003h
Max. timeout for full chip erase 2^N times typical (00h = not supported)	26h	0002h

Table 13-3. CFI Mode: Device Geometry Data Values

Description	Address	Data		
		320E	640E	128E
Device Size = 2^N byte	27h	016h	0017h	0018h
Flash Device Interface description (refer to CFI publication 100)	28h	0001h		
	29h	0000h		
Max. number of bytes in multi-byte write = 2^N (00h = not supported)	2Ah	0005h		
	2Bh	0000h		
Number of Erase Block Regions within device	2Ch	0002h		
Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)	2Dh	003Eh	007Eh	007Eh
	2Eh	0000h		
	2Fh	0000h		
	30h	0001h	0001h	0002h
Erase Block Region 2 Information	31h	0003h		
	32h	0000h		
	33h	0040h	0040h	0080h
	34h	0000h		
Erase Block Region 3 Information	35h	0000h		
	36h	0000h		
	37h	0000h		
	38h	0000h		
Erase Block Region 4 Information	39h	0000h		
	3Ah	0000h		
	3Bh	0000h		
	3Ch	0000h		

Table 13-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address (h) (Word Mode)	Data (h)
Query - Primary extended table, unique ASCII string, PRI	40h	0050h
	41h	0052h
	42h	0049h
Major version number, ASCII	43h	0031h
Minor version number, ASCII	44h	0033h
Unlock recognizes address (Bits 1-0) 0= recognize, 1= don't recognize Process Technology (Bits 7-2) 0101b=110nm	45h	0014h
Erase suspend (2= to both read and program)	46h	0002h
Sector protect (N= # of sectors/group)	47h	0001h
Temporary sector unprotect (1=supported)	48h	0000h
Sector protect/Chip unprotect scheme	49h	0008h
Simultaneous R/W operation (0=not supported)	4Ah	0000h
Burst mode (0=not supported)	4Bh	0001h
Page mode (0=not supported, 01 = 4 word page, 02 = 8 word page)	4Ch	0000h
Minimum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4Dh	0095h
Maximum ACC(acceleration) supply (0= not supported), [D7:D4] for volt, [D3:D0] for 100mV	4Eh	00A5h
WP# Protection Flag	4Fh	0003h
Program Suspend (0=not supported, 1=supported)	50h	0001h

10. ELECTRICAL CHARACTERISTICS

10-1. Absolute Maximum Stress Ratings

Surrounding Temperature with Bias		-65°C to +125°C
Storage Temperature		-65°C to +150°C
Voltage Range	VCC	-0.5V to +2.0V
	VI/O	-0.5V to +2.0V
	ACC	-0.5V to +10.5V
	The other pins.	-0.5V to Vcc +0.5V
Output Short Circuit Current (less than one second)		200 mA

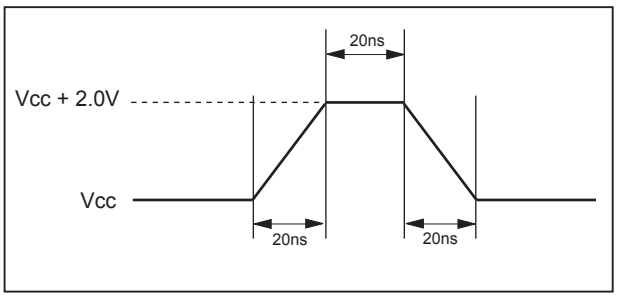
10-2. Operating Temperatures and Voltages

Commercial (C) Grade	Surrounding Temperature (T_A)	0°C to +70°C
Industrial (I) Grade	Surrounding Temperature (T_A)	-40°C to +85°C
VCC Supply Voltages	Full VCC range	1.7~1.95V
	VI/O range	= VCC

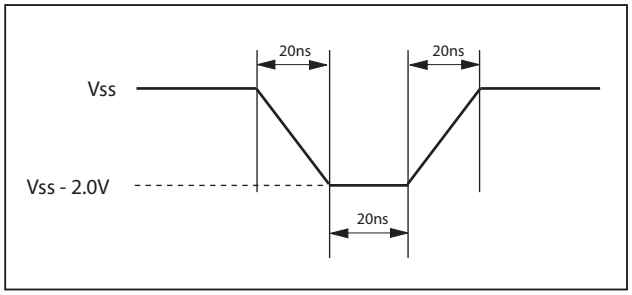
NOTES:

1. *Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.*
2. *Specifications contained within the following tables are subject to change.*
3. *During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see Figures below.*
4. *Not 100% tested.*

Maximum Positive Overshoot Waveform

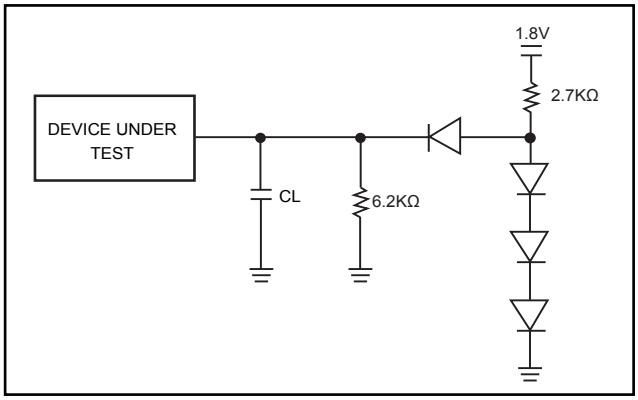


Maximum Negative Overshoot Waveform



10-3. Test Conditions

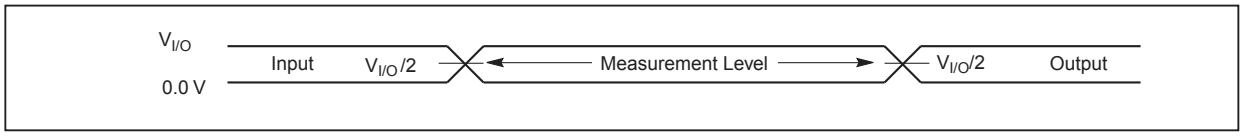
Figure 10. Test Setup



Testing Conditions:

- Output Load Capacitance, CL : 1TTL gate, 10pF
- Rise/Fall Times : 2ns
- Input Pulse levels :0.0 ~ VI/O
- In/Out reference levels :0.5VI/O

Figure 11. Input Waveforms and Measurement Levels



10-4. AC Characteristics

VCC Power-up and Power-down Sequencing

Once VCC attains its operating voltage, de-assertion of RESET# to VIH is permitted. VCC power-up and power-down sequencing are not restricted. During the entire VCC power sequence, RESET# needs to be asserted to VIL until the respective supplies reach their operating voltages. Once VCC operating voltage has been achieved, RESET# to VIH is allowed to be de-asserted.

Output Disable Mode

Once OE# is input is at VIH, output from the device is disabled and placed in the state of high impedance.

VCC Power-up

Parameter	Description	Test Setup	Speed	Unit
tVCS	VCC Setup Time	Min	1	ms

VCC Power-down

Symbol	Description	Test Setup	Speed	Unit
tVCS	VCC Setup Time	Max	200	us

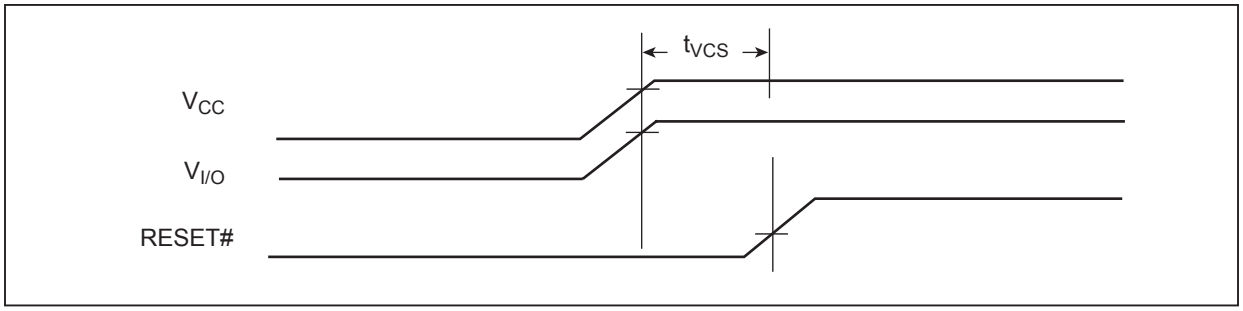
NOTES:

1. VCC >+ VI/O - 100 mV

2. VCC ramp rate is >1 V/100 us

3. Not 100% tested.

Figure 12. VCC Power-up Diagram CLK Characterization



Parameter	Description		Frequency			Unit
			66	83	108	
tCLK	CLK Cycle	Min	15	12	9.26	ns
tCLKR	CLK Rise Time	Max	3	2.5	1.9	ns
tCLKF	CLK Fall Time					
tCLKH/L	CLK High or Low Time	Min	7	5.5	4.2	ns

NOTES:

1. Clock jitter of +/- 5% permitted.

2. Values guaranteed by characterization, not 100% tested in production.

AC CHARACTERISTICS

ITEM		TYP	MAX
WEB high to release from deep power down mode	tRDP	100us	200us
WEB high to deep power down mode	tDP	10us	20us

NOTE: *Not 100% tested.*

Figure 13. Deep Power Down Mode Waveform

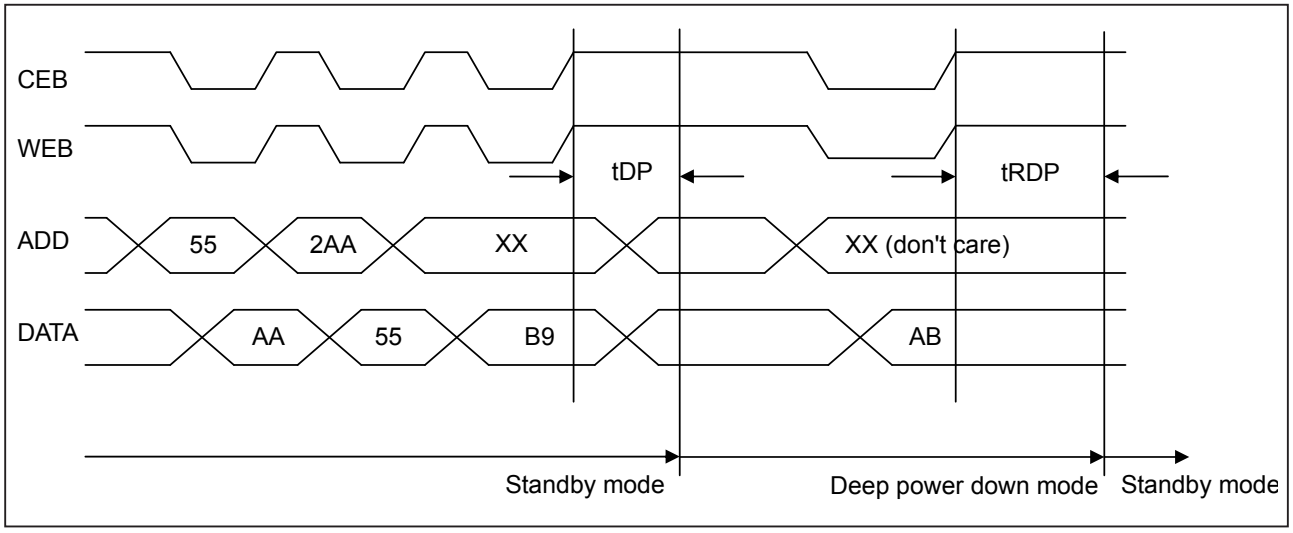


Figure 14. CLK Characterization

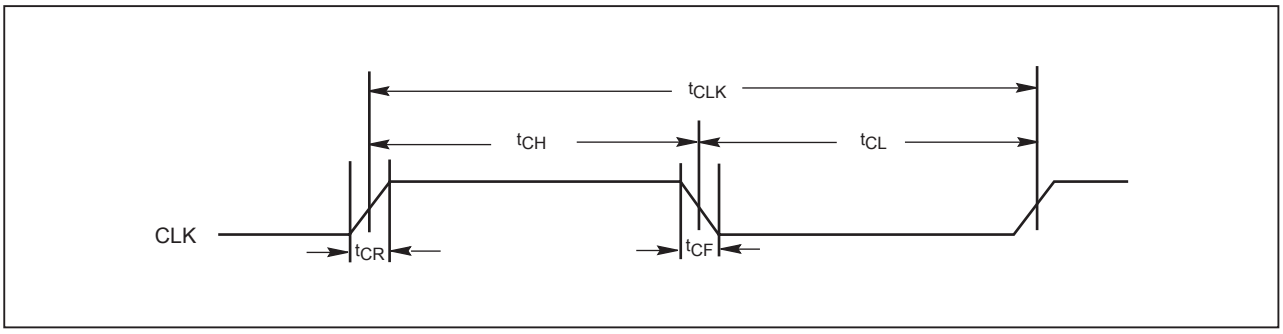
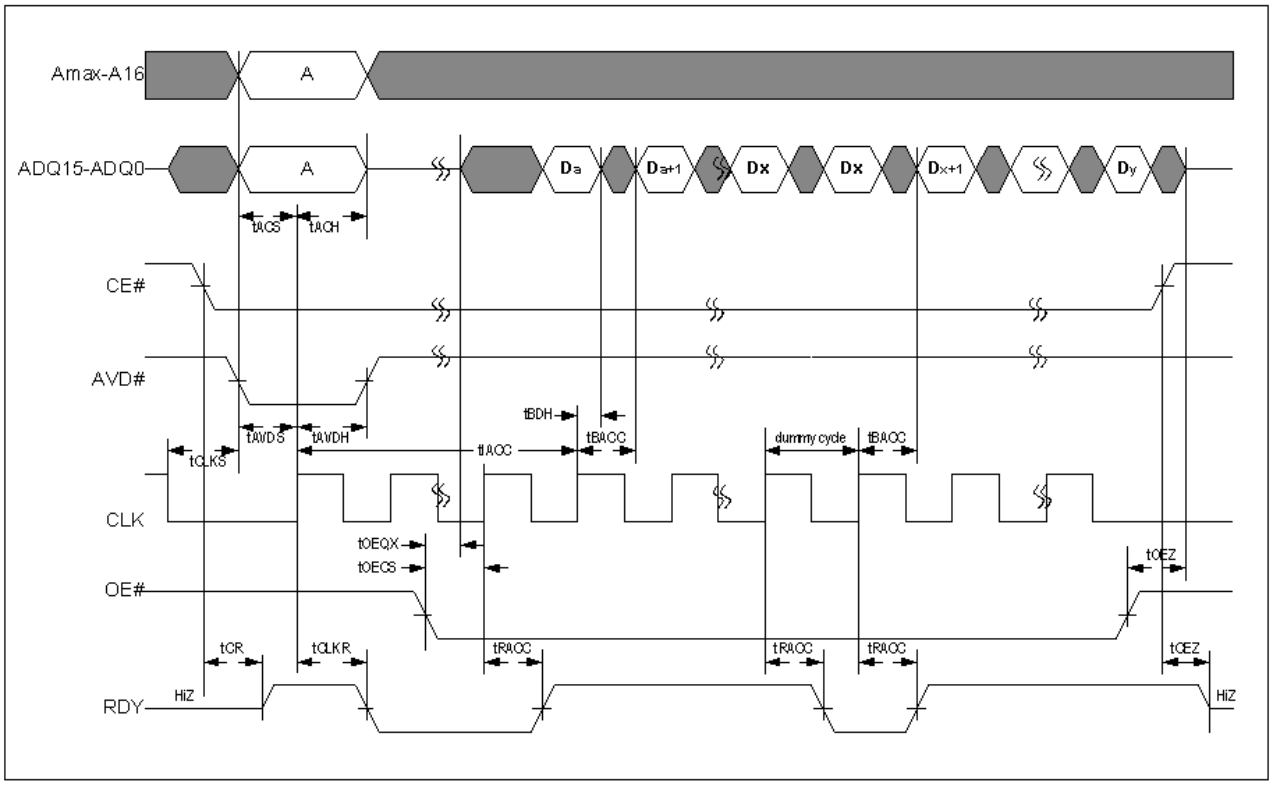


Table 15. Synchronous / Burst Read

Parameter	Description		Speed	Unit
tIACC	Initial Access Time	Max	80	ns
tBACC	Burst Access Time Valid Clock to Output Delay	Max	7	ns
tAVDS	AVD# Setup Time to CLK	Min	4	ns
tAVDH	AVD# Hold Time from CLK	Min	5	ns
tAVDO	AVD# High to OE# Low	Min	4	ns
tACS	Address Setup Time to CLK	Min	4	ns
tACH	Address Hold Time from CLK	Min	5	ns
tBDH	Data Hold Time from Next Clock Cycle	Min	0	ns
tCEZ	Chip Enable to High Z (Note)	Max	10	ns
tOEZ	Output Enable to High Z (Note)	Max	10	ns
tCES	CE# Setup Time to CLK	Max	4	ns
tRACC	Ready access time from CLK	Max	7	ns
tCLKR	First CLK rising to RDY de-asserted	Max	10	ns
tCLKS	CLK low to AVD# low	Min	5	ns
tOECS	OE# Enable to First Output CLK Setup Time	Max	8	ns

NOTE: *Not 100% tested.*

Figure 15. Burst Mode Read



NOTE: *Chip enters burst mode when 1st CLK rises.*

Table 16. Asynchronous Read

Parameter	Description			Speed	Unit
tCE	Access Time from CE# Low		Max	80	ns
tACC	Asynchronous Access Time		Max	80	ns
tAVDP	AVD# Low Time		Min	7	ns
tAAVDS	Address Setup Time to Rising Edge of AVD		Min	3.5	ns
tAAVDH	Address Hold Time from Rising Edge of AVD		Min	3.2	ns
tOE	Output Enable to Output Valid		Max	15	ns
tOEH	Output Enable Hold Time	Read	Min	0	ns
		Toggle and Data# Polling	Min	10	ns
tOEZ	Output Enable to High Z (See Note)		Max	10	ns
tOAVD	AVDB disable to OEB enable		Min	10	ns
tAVDO	OEB disable to AVDB enable		Min	10	ns
tOEQX	Output Enable to Data Low Z		Min	15	ns
tCR	CEB enable to RDY ready		Max	10	ns
tCEZ	CEB disable to RDY HiZ		Max	10	ns

NOTE: *Not 100% tested.*

Figure 16. Asynchronous Mode Read

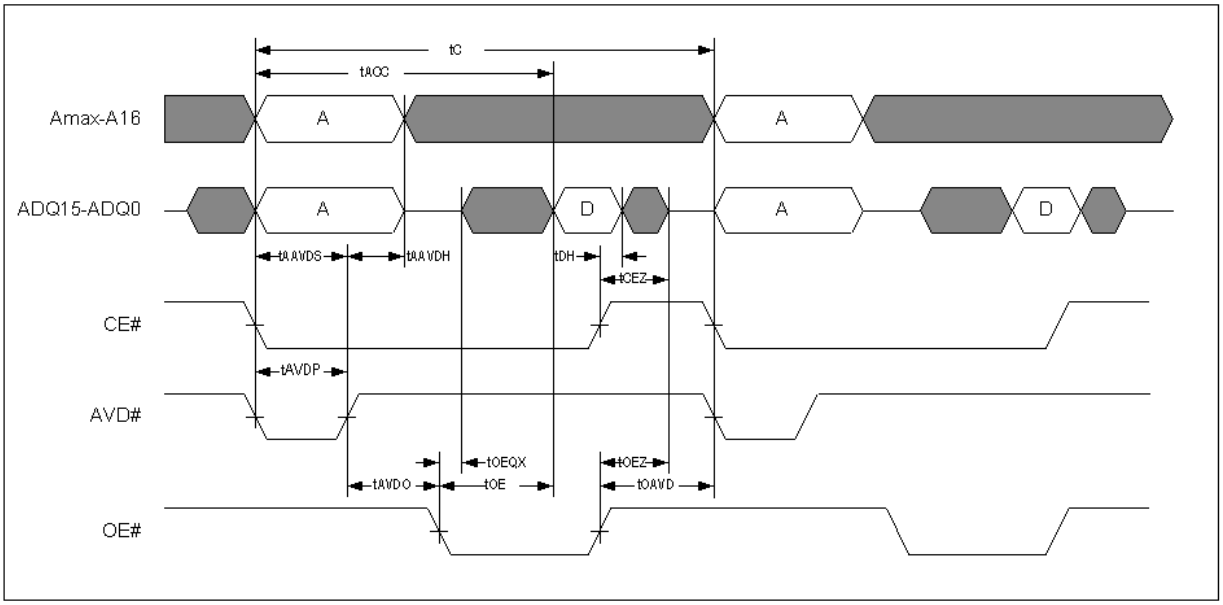


Table 17. Erase/Program Operations

Parameter	Description		Speed	Unit
tWC	Write Cycle Time (Note 1)	Min	45	ns
tAS	Address Setup Time	Min	4	ns
tAH	Address Hold Time	Min	6	ns
tAVDP	AVD# Low Time	Min	7	ns
tDS	Data Setup Time	Min	25	ns
tDH	Data Hold Time	Min	0	ns
tGHWL	Read Recovery Time Before Write	Typ	0	ns
tCS	CE# Setup Time to WE#	Typ	8	ns
tCH	CE# Hold Time	Typ	0	ns
tWP/tWRL	Write Pulse Width	Typ	30	ns
tWPH	Write Pulse Width High	Typ	20	ns
tSR/W	Latency Between Read and Write Operations	Min	0	ns
tACC	ACC Rise and Fall Time	Min	500	ns
tVPS	ACC Setup Time (During Accelerated Programming)	Min	1	us
tVCS	VCC Setup Time	Min	1	ms
tESL	Erase Suspend Latency	Max	25	us
tPSL	Program Suspend Latency	Max	25	us
tERS	Erase Resume to Erase Suspend	Min	400	us
tPRS	Program Resume to Program Suspend	Min	25	us
tWEA	WEB disable to AVDB enable	Min	10	ns

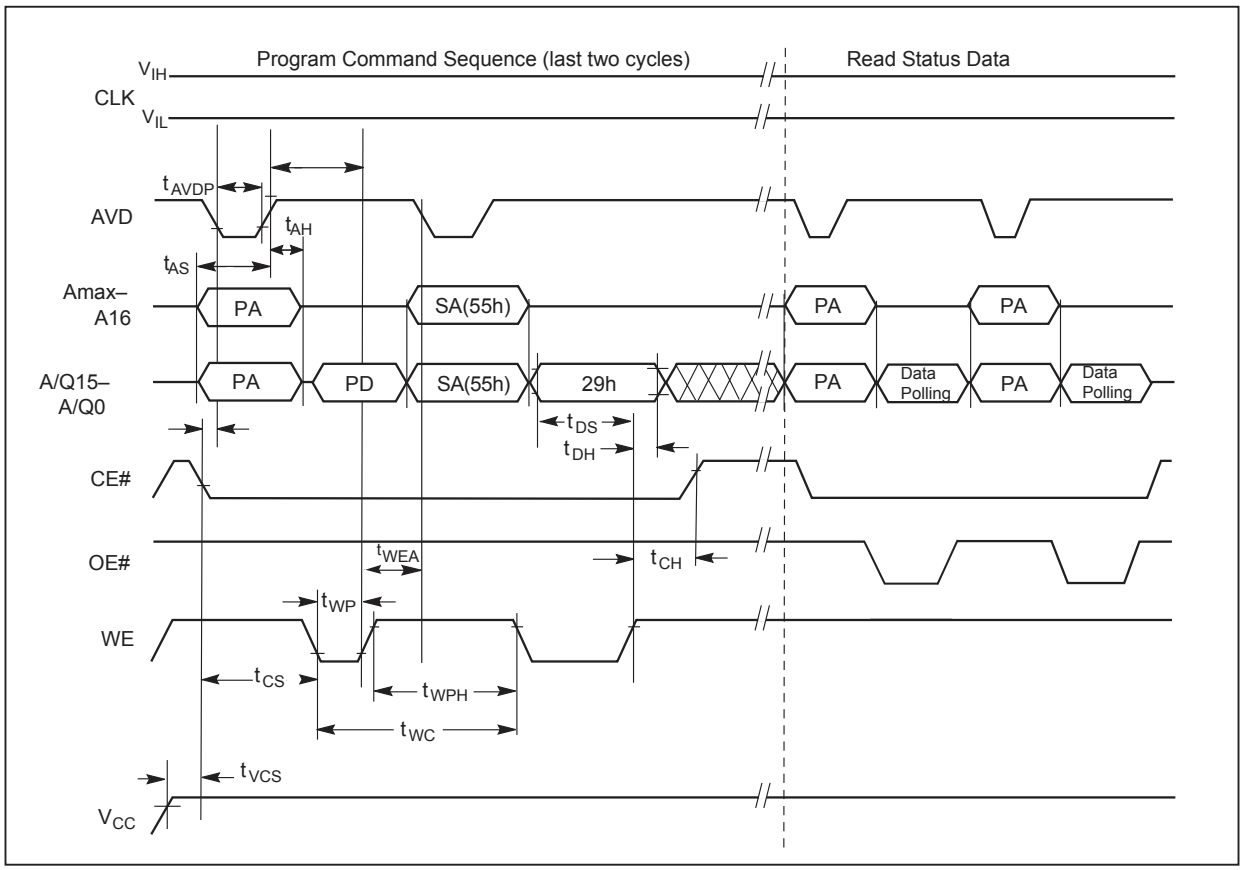
NOTES:

1. Not 100% tested.

2. See the Erase and Programming Performance section for more information.

3. Does not include the preprogramming time.

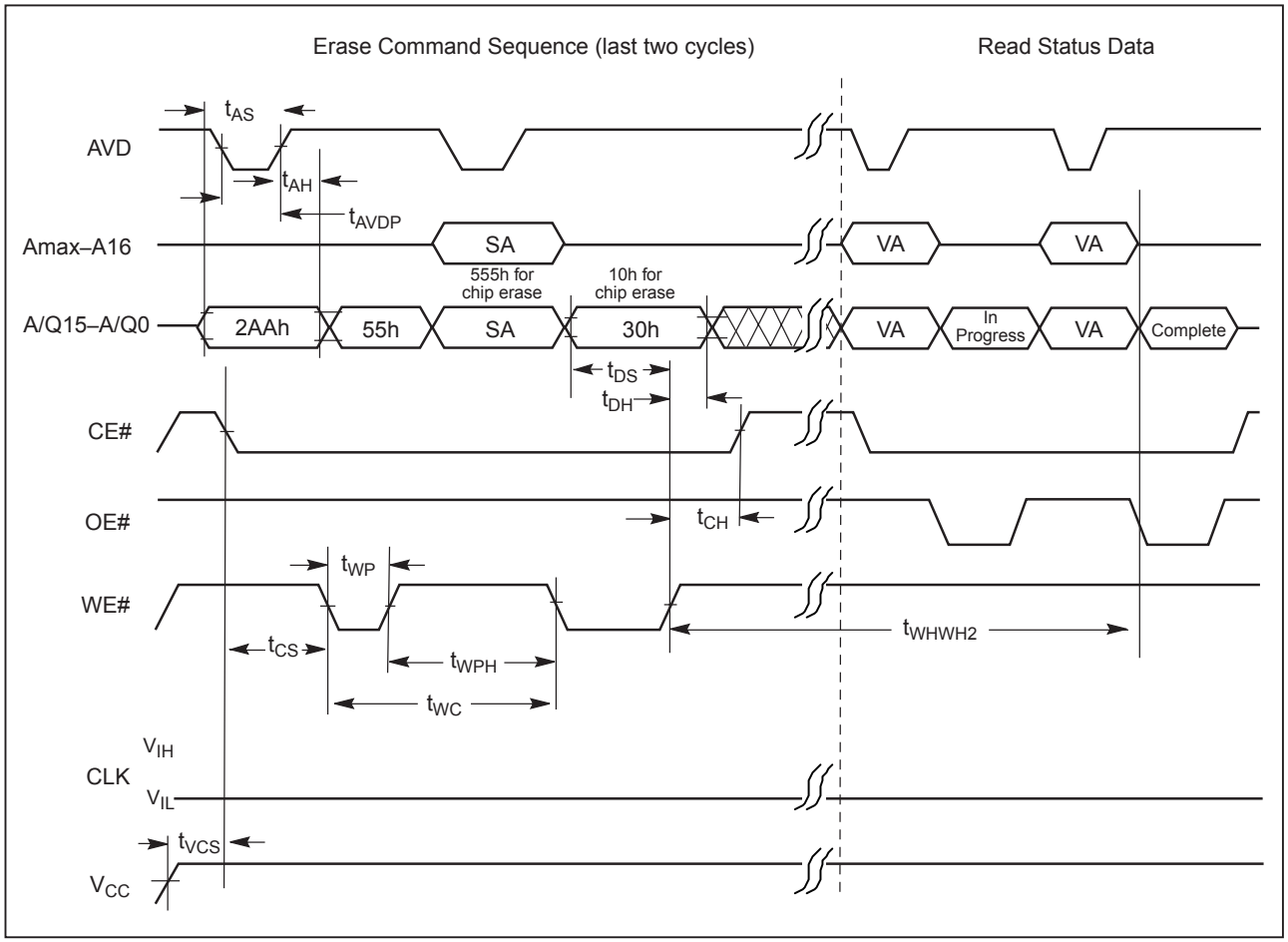
Figure 17. Program Operation Timings



NOTES:

1. *PA = Program Address, PD = Program Data, VA = Valid Address for reading status bits.*
2. *"In progress" and "complete" refer to status of program operation.*
3. *Amax–A16 are "Don't care" during command sequence unlock cycles.*

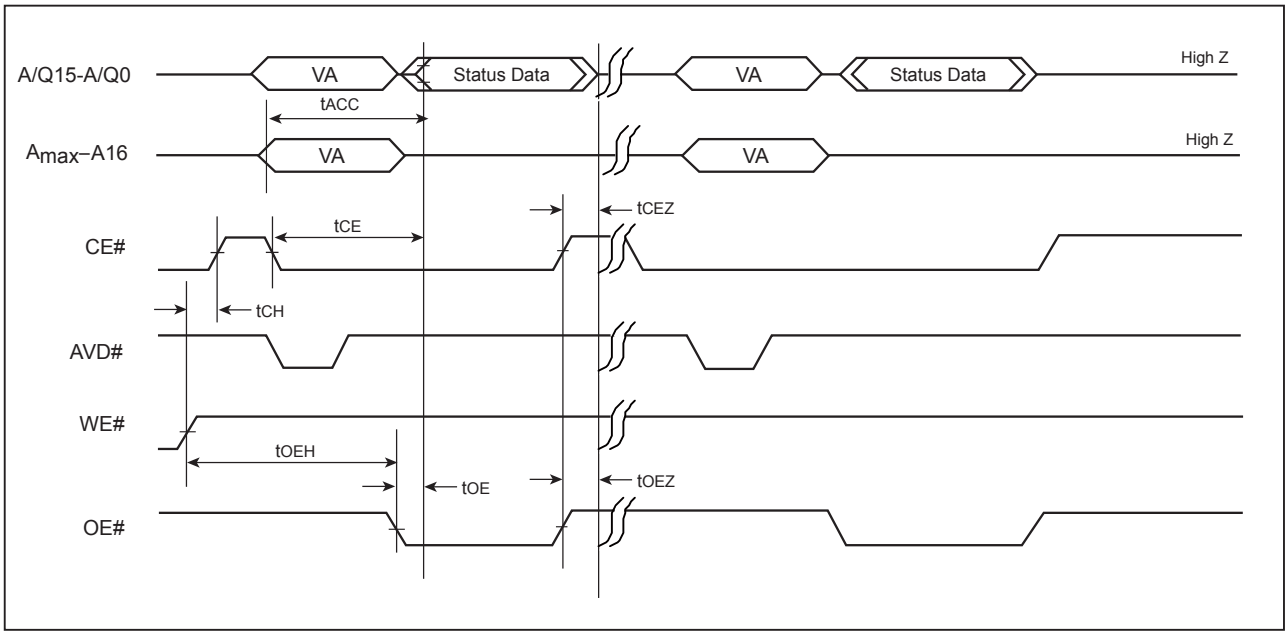
Figure 18. Chip/Sector Erase Operations



NOTES:

1. *SA is the sector address for Sector Erase.*
2. *Address bits Amax–A16 are don't cares during unlock cycles in the command sequence.*

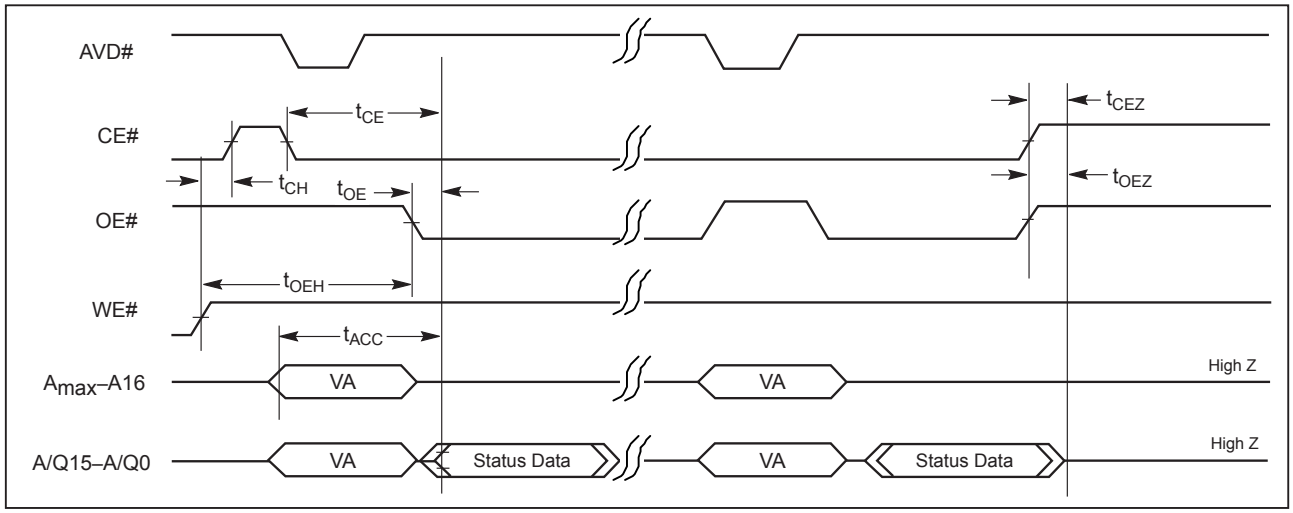
Figure 19. Data# Polling Timings (During Embedded Algorithm)



NOTES:

1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, and Data# Polling will output true data.*

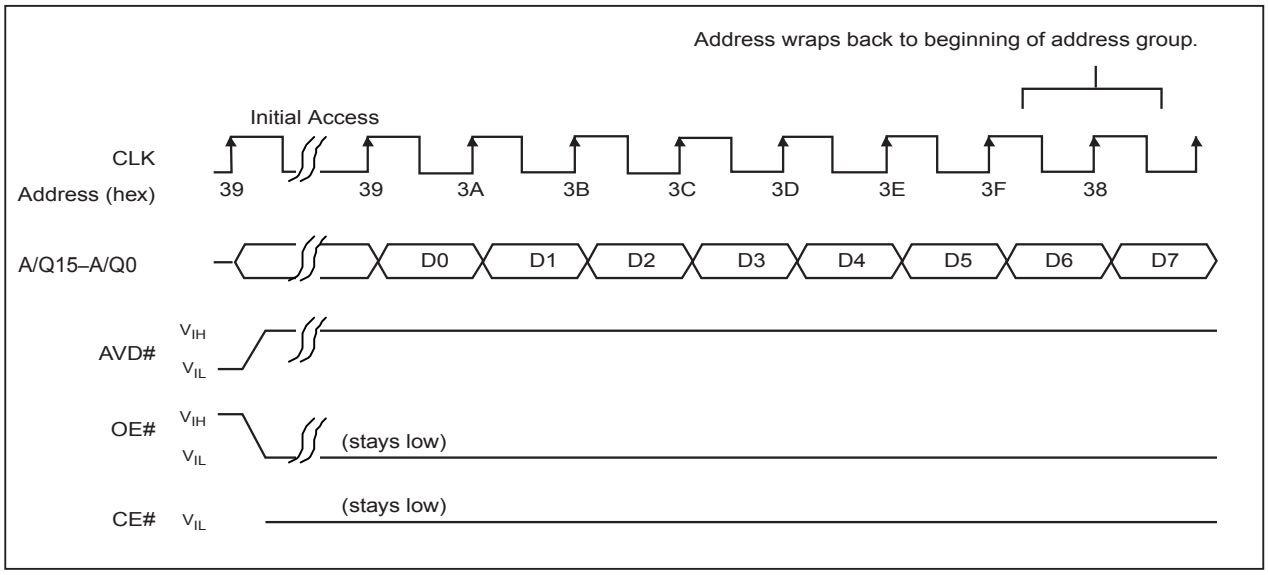
Figure 20. Toggle Bit Timings (During Embedded Algorithm)



NOTES:

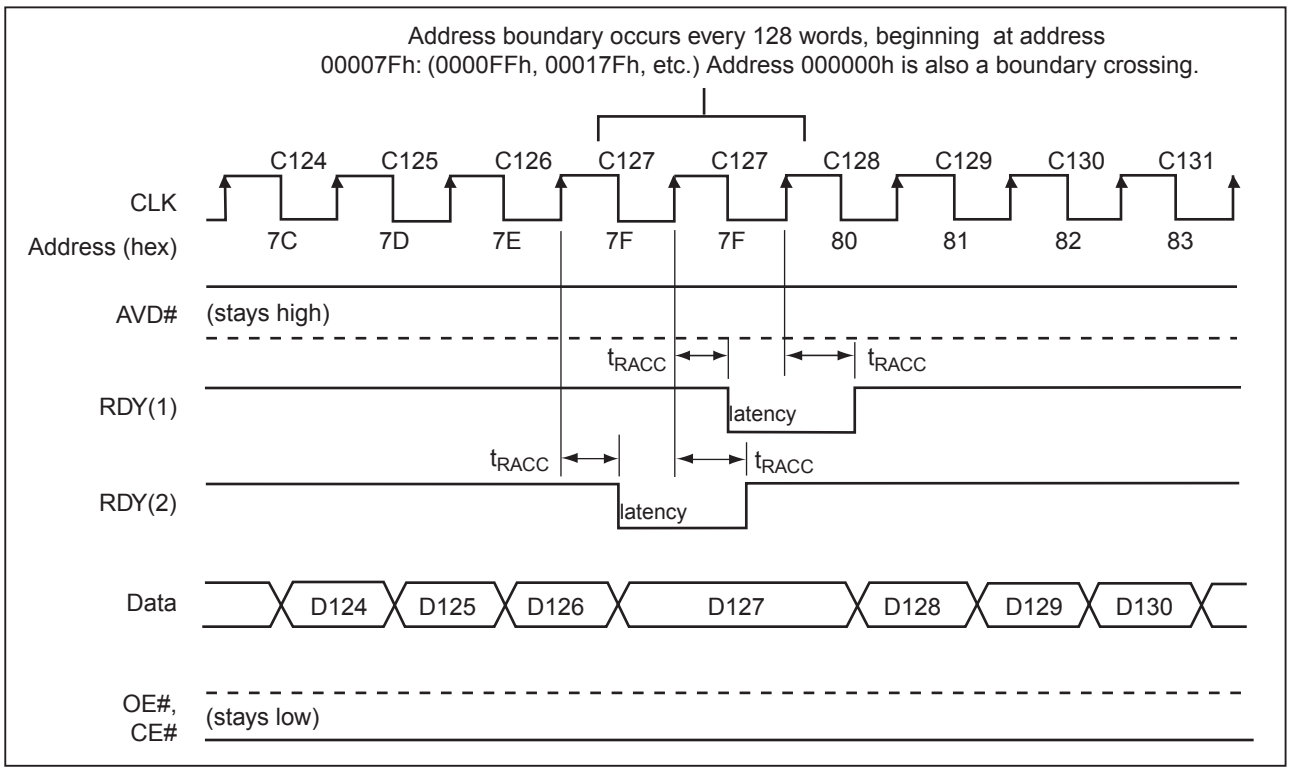
1. *All status reads are asynchronous.*
2. *VA = Valid Address. Two read cycles are required to determine status. When the Embedded Algorithm operation is complete, the toggle bits will stop toggling.*

Figure 21. 8-, 16-Word Linear Burst Address Wrap Around



NOTE: *8-word linear burst mode shown. 16-word linear burst read modes behave similarly. D0 represents the first word of the linear burst.*

Figure 22. Latency with Boundary Crossing



NOTES:

1. *Cxx indicates the clock that triggers data Dxx on the outputs; for example, C60 triggers D60.*
2. *Please reference burst read related tables for details.*

10-5. Erase and Programming Performance

PARAMETER	LIMITS			UNITS
	MIN.	TYP. (1)	MAX. (2)	
Chip Programming Time (32Mb)		20		sec
Chip Programming Time (64Mb)		40		sec
Chip Programming Time (128Mb)		80		sec
Chip Erase Time (32Mb)		32	75	sec
Chip Erase Time (64Mb)		64	150	sec
Chip Erase Time (128Mb)		128	300	sec
Sector Erase Time (32KW)		0.6	5	sec
Sector Erase Time (64KW)		0.8	7	sec
Word Program Time		40	360	us
Total Write Buffer Time		300		us
ACC Total Write Buffer Time		150		us
Erase/Program Cycles		100,000		cycles
Effective Word Programming Time		9.4		us

NOTES:

1. *Typical program and erase times assume the following conditions: 25°C, 1.8V VCC. Programming specifications assume checkboard data pattern.*
2. *Maximum values are measured at VCC = 1.8 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.*
3. *Erase/Program cycles comply with JEDEC JESD-47E & A117A standard.*
4. *Exclude 00h program before erase operation.*
5. *Not 100% tested.*

Data Retention

PARAMETER	Condition	Min.	Max.	UNIT
Data retention	55˚C	20		years

Latch-up Characteristics

	MIN.	MAX.
Input Voltage voltage difference with GND on ACC pins	-1.0V	10.5V
Input Voltage voltage difference with GND on all normal pins input	-1.0V	1.5Vcc
Vcc Current	-100mA	+100mA
All pins included except Vcc. Test conditions: Vcc = 1.8V, one pin per testing		

Pin Capacitance

Parameter Symbol	Parameter Description	Test Setup	TYP	MAX	UNIT
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN	Input Capacitance	VIN=0	6	7.5	pF

10-5-1. BGA Ball Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
CIN	Input Capacitance	VIN = 0	4.2	5.0	pF
COUT	Output Capacitance	VOUT = 0	5.4	6.5	pF
CIN2	Control Pin Capacitance	VIN = 0	3.9	4.7	pF

NOTES:

1. *Sampled, not 100% tested.*
2. *Test conditions TA = 25°C, f = 1.0 MHz.*

10-6. Low VCC Write Prohibit

The device refuses to accept any write command when Vcc is less than VLKO. This prevents data from spuriously being altered during power-up, power-down, or temporary power interruptions. The device automatically resets itself when Vcc is lower than VLKO and write cycles are ignored until Vcc is greater than VLKO. The system must provide proper signals on control pins after Vcc rises above VLKO to avoid unintentional program or erase operations.

10-6-1. Write Pulse "Glitch" Protection

CE#, WE#, OE# pulses shorter than 5ns are treated as glitches and will not be regarded as an effective write cycle. On WE#, noise pulses of less than 5ns do not initiate a write cycle.

10-6-2. Logical Prohibit

A valid write cycle requires both CE# and WE# at Vil with OE# at Vih. While initiating a write cycle, CE# and WE# must be a logical "0" while OE# is a logical "1". Write cycle is ignored when either CE# at Vih, WE# at Vih, or OE# at Vil.

10-6-3. Power-up Sequence

Upon power-up, the device is placed in Read mode. Furthermore, program or erase operation will begin only after successful completion of specified command sequences.

10-6-4. Power-up Write Prohibit

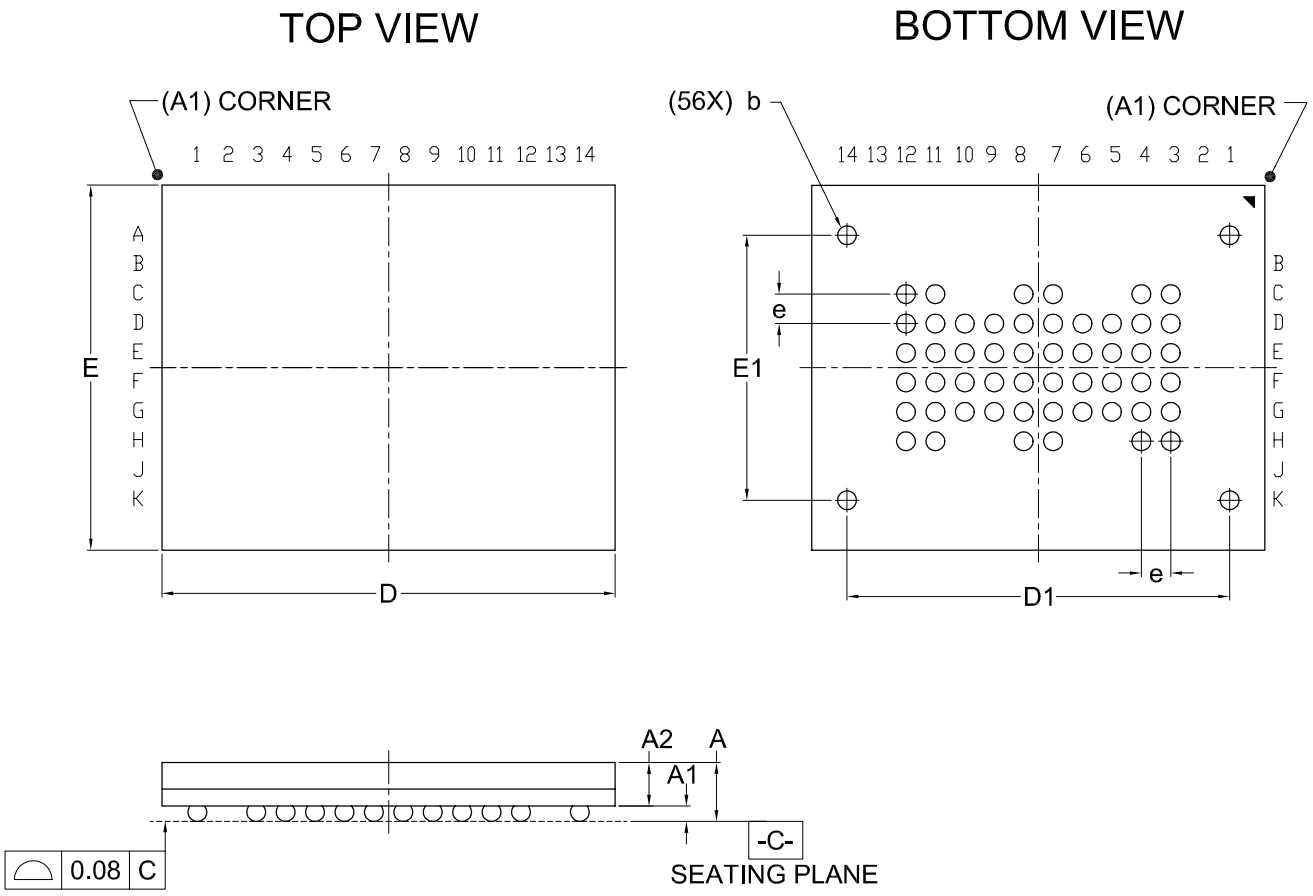
When WE#, CE# is held at Vil and OE# is held at Vih during power up, the device ignores the first command on the rising edge of WE#.

10-6-5. Power Supply Decoupling

A 0.1uF capacitor should be connected between the Vcc and GND to reduce the noise effect.

11. PACKAGE INFORMATION

Title: **Package Outline for CSP 56BALL(7.7X6.2X1.2MM,BALL PITCH 0.5MM,BALL DIAMETER 0.3MM)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.16	0.65	0.25	7.6	---	6.1	—	—
	Nom.	---	0.21	—	0.30	7.7	6.5	6.2	4.5	0.50
	Max.	1.20	0.26	—	0.35	7.8	---	6.3	—	—
Inch	Min.	—	0.006	0.026	0.010	0.299	—	0.240	—	---
	Nom.	—	0.008	—	0.012	0.303	0.256	0.244	0.177	0.0197
	Max.	0.047	0.010	—	0.014	0.307	—	0.248	—	---

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-4264	0				

12. REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. A note added to Table 2-2 Ordering Information.	P8	MAR/23/2011
	2. A note added to Table 11. DC Characteristics.	P49	MAR/23/2011
	3. A note revised for CLK Characteristics.	P57	MAR/23/2011
1.1	1. Modified: MX29NS320/640/128E have been pre-released & in mass production.	P8	APR/26/2011
	2. Table 17. Parameters tPSP & tASP removed	P61	

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