MX29L1611G / MX29L1611*

16M-BIT [2M x 8/1M x 16] CMOS SINGLE VOLTAGE FLASH EEPROM

FEATURES

- 3.3V ± 10% for write and read operation
- 11V Vpp erase/programming operation
- Endurance: 100 cycles
- Fast random access time: 90ns/100ns/120ns
- Fast page access time: 30ns (Only for 29L1611PC-90/10/12)
- Sector erase architecture
  - 32 equal sectors of 64k bytes each
  - Sector erase time: 200ms typical
- Auto Erase and Auto Program Algorithms
  - Automatically erases any one of the sectors or the whole chip
  - Automatically programs and verifies data at specified addresses
- Status Register feature for detection of program or erase cycle completion
- Low VCC write inhibit is equal to or less than 1.8V
- Software data protection
- Page program operation
  - Internal address and data latches for 64 words per page
  - Page programming time: 5ms typical
- Low power dissipation
  - 50mA active current
  - 20uA standby current
- Two independently Protected sectors
- Package type
  - 42 pin plastic DIP

* For page mode read only

GENERAL DESCRIPTION

The MX29L1611G is a 16-mega bit Flash memory organized as either 1M wordx16 or 2M bytex8. The MX29L1611G includes 32 sectors of 64KB(65,536 Bytes or 32,768 words). MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29L1611G is packaged in 42 pin PDIP.

The standard MX29L1611G offers access times as fast as 100ns,allowing operation of high-speed microprocessors without wait. To eliminate bus contention, the MX29L1611G has separate chip enable $\overline{CE}$ and, output enable ($\overline{OE}$).

MXIC's Flash memories augment EPROM functionality with electrical erasure and programming. The MX29L1611G uses a command register to manage this functionality.

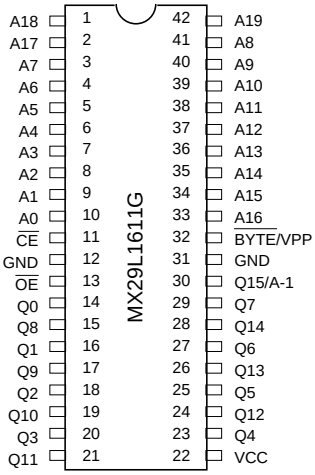
MX29L1611G does require high input voltages for programming. Commands require 11V input to determine the operation of the device. Reading data out of the device is similar to reading from an EPROM.

MXIC Flash technology reliably stores memory contents even after 100 cycles. The MXIC's cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29L1611G uses a 11V Vpp supply to perform the Auto Erase and Auto Program algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC +1V.

PIN CONFIGURATIONS

42 PDIP



PIN DESCRIPTION

SYMBOL	PIN NAME
A0 - A19	Address Input
Q0 - Q14	Data Input/Output
Q15/A-1	Q15(Word mode)/LSB addr.(Byte mode, for read mode only)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{BYTE}$/VPP	Word/Byte Selection Input, Erase/ Program supply voltage
VCC	Power Supply
GND	Ground Pin

BLOCK DIAGRAM

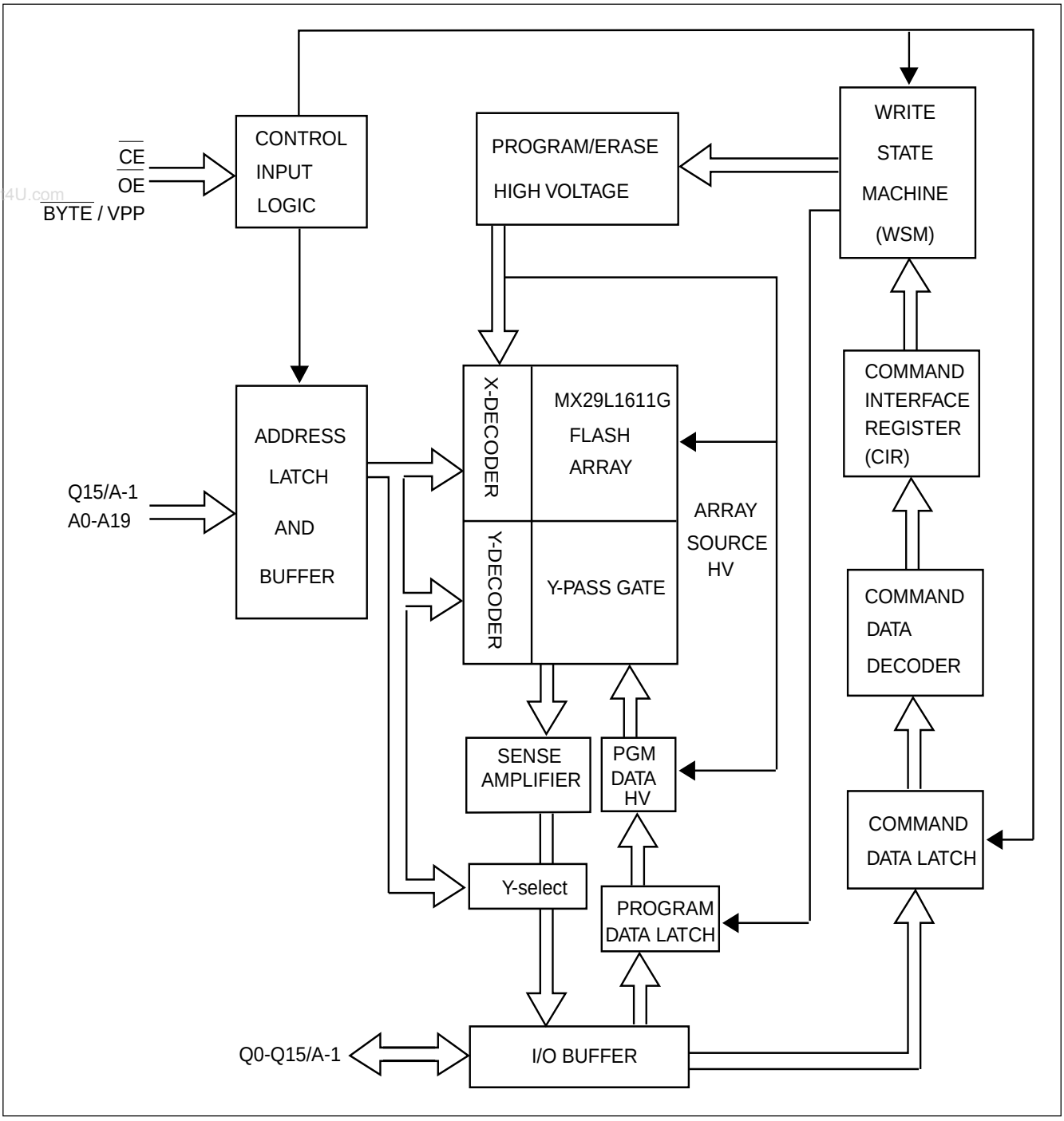


Table1. PIN DESCRIPTIONS

SYMBOL	TYPE	NAME AND FUNCTION
A0 - A19	INPUT	ADDRESS INPUTS: for memory addresses. Addresses are internally latched during a write cycle.
Q0 - Q7	INPUT/OUTPUT	LOW-BYTE DATA BUS: Input data and commands during Command Interface Register(CIR) write cycles. Outputs array,status and identifier data in the appropriate read mode. Floated when the chip is de-selected or the outputs are disabled.
Q8 - Q14	INPUT/OUTPUT	HIGH-BYTE DATA BUS: Inputs data during x 16 Data-Write operations. Outputs array, identifier data in the appropriate read mode; not used for status register reads. Floated when the chip is de-selected or the outputs are disabled
Q15/A -1	INPUT/OUTPUT	Selects between high-byte data INPUT/OUTPUT($\overline{BYTE}$ = HIGH) and LSB ADDRESS($\overline{BYTE}$ = LOW) for raed operation.
$\overline{CE}$	INPUT	CHIP ENABLE INPUTS: Activate the device's control logic, Input buffers, decoders and sense amplifiers. With $\overline{CE}$ high, the device is deselected and power consumption reduces to Standby level upon completion of any current program or erase operations. $\overline{CE}$ must be low to select the device.
$\overline{OE}$	INPUT	OUTPUT ENABLES: Gates the device's data through the output buffers during a read cycle $\overline{OE}$ is active low.
$\overline{BYTE}$/VPP	INPUT	BYTE ENABLE: While operating read mode, $\overline{BYTE}$ Low places device in x8 mode. All data is then input or output on Q0-7 and Q8-14 float. AddressQ15/A-1 selects between the high and low byte. While operating read mode, $\overline{BYTE}$ high places the device in x16 mode, and turns off the Q15/A-1 input buffer. Address A0, then becomes the lowest order address. ERASE/PROGRAM ENABLE:When $\overline{BYTE}$/VPP=11V would place this device into ERASE/PROGRAM mode.
VCC		DEVICE POWER SUPPLY(3.3V ± 10%)
GND		GROUND

BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU . All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

Table 2.1 Bus Operations for Word-Wide Mode ($\overline{BYTE}$/VPP = VIH)

Mode	Notes	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$/VPP	A0	A1	A9	Q0-Q7	Q8-Q14	Q15/A-1
Read	1	VIL	VIL	VIH	X	X	X	DOUT	DOUT	DOUT
Output Disable	1	VIL	VIH	VIH	X	X	X	High Z	High Z	HighZ
Standby	1	VIH	X	H/L	X	X	X	High Z	HIgh Z	HighZ
Manufacturer ID	2,4	VIL	VIL	VIH	VIL	VIL	VID	C2H	00H	0B
Device ID	2,4	VIL	VIL	VIH	VIH	VIL	VID	F6H	00H	0B
Write	1,3,5	VIL	VIH	VPP	X	X	X	DIN	DIN	DIN

Table2.2 Bus Operations for Byte-Wide Mode ($\overline{BYTE}$ = VIL)

Mode	Notes	$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$/VPP	A0	A1	A9	Q0-Q7	Q8-Q14	Q15/A-1
Read	1	VIL	VIL	VIL	X	X	X	DOUT	HighZ	VIL/VIH
Output Disable	1	VIL	VIH	VIL	X	X	X	High Z	High Z	X
Standby	1	VIH	X	H/L	X	X	X	High Z	HIgh Z	X
Manufacturer ID	2,4	VIL	VIL	VIL	VIL	VIL	VID	C2H	High Z	VIL
Device ID	2,4	VIL	VIL	VIL	VIH	VIL	VID	F6H	High Z	VIL
Write	1,3,5	VIL	VIH	VPP	X	X	X	DIN	DIN	DIN

NOTES :

1. X can be VIH or VIL for address or control pins.
2. A0 and A1 at VIL provide manufacturer ID codes. A0 at VIH and A1 at VIL provide device ID codes. A0 at VIL, A1 at VIH and with appropriate sector addresses provide Sector Protect Code.(Refer to Table 4),A2~A19=Do not care.
3. Commands for different Erase operations, Data program operations or Sector Protect operations can only be successfully completed through proper command sequence.
4. VID = 11.5V- 12.5V
5. Word mode only for write operation VPP=10.5V~11.5V

WRITE OPERATIONS

Commands are written to the COMMAND INTERFACE REGISTER (CIR) using standard microprocessor write timings. The CIR serves as the interface between the microprocessor and the internal chip operation. The CIR can decipher Read Array, Read Silicon ID, Erase and Program command. In the event of a read command, the CIR simply points the read path at either the array or the silicon ID, depending on the specific read command given. For a program or erase cycle, the CIR informs the write state machine that a program or erase has been requested. During a program cycle, the write state machine will control the program sequences and the CIR will only respond to status reads. During a sector/chip erase cycle, the CIR will respond to status reads. After the write state machine has completed its task, it will allow the CIR to respond to its full command set. The CIR stays at read status register mode until the microprocessor issues another valid command sequence.

Device operations are selected by writing commands into the CIR. Table 3 below defines 16 Mbit flash family command.

TABLE 3. COMMAND DEFINITIONS($\overline{BYTE}$/VPP=VHH)

Command Sequence		Read/ Reset	Silicon ID Read	Page Program	Chip Erase	Sector Erase	Read Status Reg.	Clear Status Reg.
Bus Write Cycles Req'd		4	4	4	6	6	4	3
First Bus Write Cycle	Addr	5555H	5555H	5555H	5555H	5555H	5555H	5555H
	Data	AAH	AAH	AAH	AAH	AAH	AAH	AAH
Second Bus Write Cycle	Addr	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH	2AAAH
	Data	55H	55H	55H	55H	55H	55H	55H
Third Bus Write Cycle	Addr	5555H	5555H	5555H	5555H	5555H	5555H	5555H
	Data	F0H	90H	A0H	80H	80H	70H	50H
Fourth Bus Read/Write Cycle	Addr	RA	00H/01H	PA	5555H	5555H	X	
	Data	RD	C2H/F6H	PD	AAH	AAH	SRD	
Fifth Bus Write Cycle	Addr				2AAAH	2AAAH		
	Data				55H	55H		
Sixth Bus Write Cycle	Addr				5555H	SA		
	Data				10H	30H		

TABLE 3. COMMAND DEFINITIONS

Command Sequence		Sector Protection	Sector Unprotect	Verify Sector Protect	Abort
Bus Write Cycles Req'd		6	6	4	3
First Bus Write Cycle	Addr	5555H	5555H	5555H	5555H
	Data	AAH	AAH	AAH	AAH
Second Bus Write Cycle	Addr	2AAAH	2AAAH	2AAAH	2AAAH
	Data	55H	55H	55H	55H
Third Bus Write Cycle	Addr	5555H	5555H	5555H	5555H
	Data	60H	60H	90H	E0H
Fourth Bus Read/Write Cycle	Addr	5555H	5555H	SA**	
	Data	AAH	AAH	C2H*	
Fifth Bus Write Cycle	Addr	2AAAH	2AAAH		
	Data	55H	55H		
Sixth Bus Write Cycle	Addr	SA**	SA**		
	Data	20H	40H		

Notes:
1. Address bit A15 -- A19 = X = Don't care for all address commands except for Program Address(PA) and Sector Address(SA). 5555H and 2AAAH address command codes stand for Hex number starting from A0 to A14.
2. Bus operations are defined in Table 2.
3. RA = Address of the memory location to be read.
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{CE}$ pulse.
   SA = Address of the sector to be erased. The combination of A15 -- A19 will uniquely select any sector.
4. RD = Data read from location RA during read operation.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{CE}$.
   SRD = Data read from status register.
5. Only Q0-Q7 command data is taken, Q8-Q15 = Don't care.
   * Refer to Table 4, Figure 11.
   ** Only the top and the bottom sectors have protect- bit feature. SA = (A19,A18,A17,A16,A15) = 00000B or 11111B is valid.

DEVICE OPERATION

SILICON ID READ

The Silicon ID Read mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force VID (11.5V~12.5V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from VIL to VIH. All addresses are don't cares except A0 and A1.

The manufacturer and device codes may also be read via the command register, for instances when the MX29L1611G is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 3.

Byte 0 (A0=VIL) represents the manfacturer's code (MXIC=C2H) and byte 1 (A0=VIH) the device identifier code (MX29L1611G=F6H).

To terminate the operation, it is necessary to write the read/reset command sequence into the CIR.

Table 4. MX29L1611G Silion ID Codes and Verify Sector Protect Code

Type	A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_1	A_0	Code(HEX)	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
Manufacturer Code	X	X	X	X	X	VIL	VIL	C2H*	1	1	0	0	0	0	1	0
MX29L1611G Device Code	X	X	X	X	X	VIL	VIH	F6H*	1	1	1	1	0	1	1	0
Verify Sector Protect	Sector Address***					VIH	VIL	C2H**	1	1	0	0	0	0	1	0

* MX29L1611G Manufacturer Code = C2H, Device Code = F6H when $\overline{BYTE}$/VPP = VIL
MX29L1611G Manufacturer Code = 00C2H, Device Code = 00F6H when $\overline{BYTE}$/VPP = VIH
** Outputs C2H at protected sector address, 00H at unprotected scetor address.
***Only the top and the bottom sectors have protect-bit feature. Sector address = (A19, A18,A17,A16,A15) = 00000B or 11111B

READ/RESET COMMAND

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the CIR contents are altered by a valid command sequence.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required for "read operation". Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

The MX29L1611G is accessed like an EPROM. When $\overline{CE}$ and $\overline{OE}$ are low the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

Note that the read/reset command is not valid when program or erase is in progress.

PAGE READ

The MX29L1611G offers "fast page mode read" function. The users can take the access time advantage if keeping $\overline{CE}$, $\overline{OE}$ at low and the same page address (A3~A19 unchanged). Please refer to Figure 5-2 for detailed timing waveform. The system performance could be enhanced by initiating 1 normal read and 7 fast page reads(for word mode A0~A2) or 15 fast page reads(for byte mode altering A-1~A2).

PAGE PROGRAM

The device is set up in the programming mode when VPP=11V is applied $\overline{OE}$=VIH.

To initiate Page program mode, a three-cycle command sequence is required. There are two "unlock" write cycles. These are followed by writing the page program command-A0H.

Any attempt to write to the device without the three-cycle command sequence will not start the internal Write State Machine(WSM), no data will be written to the device.

After three-cycle command sequence is given, a byte(word) load is performed by applying a low pulse on the $\overline{CE}$ input with $\overline{CE}$ low and $\overline{OE}$ high. The address is latched on the falling edge of $\overline{CE}$. The data is latched by the first rising edge of $\overline{CE}$. Maximum of 64 words of data may be loaded into each page by the same procedure as outlined in the page program section below.

PROGRAM

Any page to be programmed should have the page in the erased state first, i.e. performing sector erase is suggested before page programming can be performed.

The device is programmed on a page basis. If a word of data within a page is to be changed, data for the entire page can be loaded into the device. Any word that is not loaded during the programming of its page will be still in the erased state (i.e. FFH). Once the words of a page are loaded into the device, they are simultaneously programmed during the internal programming period. After the first data word has been loaded into the device, successive words are entered in the same manner. Each new word to be programmed must have its high to low transition on $\overline{CE}$ within 30us of the low to high transition of $\overline{CE}$ of the preceding word. A6 to A19 specify the page address, i.e., the device is page-aligned on 64 words boundary. The page address must be valid during each high to low transition of $\overline{CE}$. A0 to A5 specify the word address withih the page. The word may be loaded in any order; sequential loading is not required. If a high to low transition of $\overline{CE}$ is not detected whithin 100us of the last low to high transition, the load period will end and the internal programming period will start. The Auto page program terminates when status on Q7 is '1' at which time the device stays at read status register mode until the CIR contents are altered by a valid command sequence.(Refer to table 3,6 and Figure 1,7,8)

CHIP ERASE

The device is set up in the erase mode when VPP=11V is applied $\overline{OE}$=VIH.

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the

"set-up" command-80H. Two more "unlock" write cycles are then followed by the chip erase command-10H.

Chip erase does not require the user to program the device prior to erase.

The automatic erase begins on the rising edge of the last $\overline{CE}$ pulse in the command sequence and terminates when the status on Q7 is "1" at which time the device stays at read status register mode. The device remains enabled for read status register mode until the CIR contents are altered by a valid command sequence.(Refer to table 3,6 and Figure 2,6,8)

Table 5. MX29L1611G Sector Address Table (Byte-Wide Mode)

	A19	A18	A17	A16	A15	Address Range [A19, -1]
SA0	0	0	0	0	0	000000H--00FFFFH
SA1	0	0	0	0	1	010000H--01FFFFH
SA2	0	0	0	1	0	020000H--02FFFFH
SA3	0	0	0	1	1	030000H--03FFFFH
SA4	0	0	1	0	0	040000H--04FFFFH
	...	...	...	...	...	.....
SA31	1	1	1	1	1	1F0000H--1FFFFFH

SECTOR ERASE

Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command-80H. Two more "unlock" write cycles are then followed by the sector erase command-30H. The sector address is latched on the falling edge of $\overline{CE}$, while the command (data) is latched on the rising edge of $\overline{CE}$.

Sector erase does not require the user to program the device prior to erase. The system is not required to provide any controls or timings during these operations.

The automatic sector erase begins on the rising edge of the last $\overline{CE}$ pulse in the command sequence and terminates when the status on Q7 is "1" at which time the device stays at read status register mode. The device remains enabled for read status register mode until the CIR contents are altered by a valid command sequence.(Refer to table 3,6 and Figure 3,4,6,8)

READ STATUS REGISTER

The MXIC's 16 Mbit flash family contains a status register which may be read to determine when a program or erase operation is complete, and whether that operation completed successfully. The status register may be read at any time by writing the Read Status command to the CIR. After writing this command, all subsequent read operations output data from the status register until another valid command sequence is written to the CIR. A Read Array command must be written to the CIR to return to the Read Array mode.

The status register bits are output on Q3 - Q7(table 6) whether the device is in the byte-wide (x8) or word-wide (x16) mode for the MX29L1611G. In the word-wide mode the upper byte, Q(8:15) is set to 00H during a Read Status command. In the byte-wide mode, Q(8:14) are tri-stated and Q15/A-1 retains the low order address function.

It should be noted that the contents of the status register are latched on the falling edge of $\overline{OE}$ or $\overline{CE}$ whichever occurs last in the read cycle. This prevents possible bus errors which might occur if the contents of the status register change while reading the status register. $\overline{CE}$ or $\overline{OE}$ must be toggled with each subsequent status read, or the completion of a program or erase operation will not be evident.

The Status Register is the interface between the microprocessor and the Write State Machine (WSM). When the WSM is active, this register will indicate the status of the WSM, and will also hold the bits indicating whether or not the WSM was successful in performing the desired operation. The WSM sets status bits four through seven and clears bits six and seven, but cannot clear status bits four and five. If Erase fail or Program fail status bit is detected, the Status Register is not cleared until the Clear Status Register command is written. The MX29L1611G automatically outputs Status Register data when read after Chip Erase, Sector Erase, Page Program or Read Status Command write cycle. The default state of the Status Register after powerup and return from deep power-down mode is (Q7, Q6, Q5, Q4) = 1000B. Q3 = 0 or 1 depends on sector-protect status, can not be changed by Clear Status Register Command or Write State Machine.

CLEAR STATUS REGISTER

The Eraes fail status bit (Q5) and Program fail status bit (Q4) are set by the write state machine, and can only be reset by the system software. These bits can indicate various failure conditions(see Table 6). By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several pages or erasing multiple blocks in squence). The status register may then be read to determine if an error occurred during that programming or erasure series. This adds flexibility to the way the device may be programmed or erased. Additionally, once the program(erase) fail bit happens, the program (erase) operation can not be performed further. The program(erase) fail bit must be reset by system software before further page program or sector (chip) erase are attempted. To clear the status register, the Clear Status Register command is written to the CIR. Then, any other command may be issued to the CIR. Note again that before a read cycle can be initiated, a Read command must be written to the CIR to specify whether the read data is to come from the Array, Status Register or Silicon ID.

TABLE 6. MX29L1611G STATUS REGISTER

	STATUS	NOTES	Q7	Q6	Q5	Q4	Q3
IN PROGRESS	PROGRAM	1,2,5	0	0	0	0	0/1
	ERASE	1,3,5	0	0	0	0	0/1
COMPLETE	PROGRAM	1,2,5	1	0	0	0	0/1
	ERASE	1,3,5	1	0	0	0	0/1
FAIL	PROGRAM	1,4,5	1	0	0	1	0/1
	ERASE	1,4,5	1	0	1	0	0/1
AFTER CLEARING STATUS REGISTER		5	1	0	0	0	0/1

NOTES:

1. Q7 : WRITE STATE MACHINE STATUS
   1 = READY, 0 = BUSY
   Q5 : ERASE FAIL STATUS
   1 = FAIL IN ERASE, 0 = SUCCESSFUL ERASE
   Q4 : PROGRAM FAIL STATUS
   1 = FAIL IN PROGRAM, 0 = SUCCESSFUL PROGRAM
   Q3 : SECTOR-PROTECT STATUS
   1 = SECTOR 0 OR/AND 15 PROTECTED
   0 = NONE OF SECTOR PROTECTED
   Q6,Q2 - 0 = RESERVED FOR FUTURE ENHANCEMENTS.
   These bits are reserved for future use ; mask them out when polling the Status Register.
2. PROGRAM STATUS is for the status during Page Programming or Sector Unprotect mode.
3. ERASE STATUS is for the status during Sector/Chip Erase or Sector Protection mode.
4. FAIL STATUS bit(Q4 or Q5) is provided during Page Program or Sector/Chip Erase modes respectively.
5. Q3 = 0 or1 depends on Sector-Protect Status.

SECTOR PROTECTION

To activate this mode, a six-bus cycle operation and VPP=11V are required. There are two 'unlock' write cycles. These are followed by writing the 'set-up' command. Two more 'unlock' write cycles are then followed by the Lock Sector command - 20H. Sector address is latched on the falling edge of $\overline{CE}$ of the sixth cycle of the command sequence. The automatic Lock operation begins on the rising edge of the last $\overline{CE}$ pulse in the command sequence and terminates when the Status on Q7 is '1' at which time the device stays at the read status register mode.

The device remains enabled for read status register mode until the CIR contents are altered by a valid command sequence (Refer to table 3,6 and Figure 9,11).

VERIFY SECTOR PROTECT

To verify the Protect status of the Top and the Bottom sector, operation is initiated by writing Silicon ID read command into the command register. Following the command write, a read cycle from address XX00H retrieves the Manufacturer code of C2H. A read cycle from XX01H returns the Device code F8H. A read cycle from appropriate address returns information as to which sectors are protected. To terminate the operation, it is necessary to write the read/reset command sequence into the CIR.
(Refer to table 3,4 and Figure 11)

A few retries are required if Protect status can not be verified successfully after each operation.

SECTOR UNPROTECT

It is also possible to unprotect the sector , same as the first five write command cycles in activating sector protection mode followed by the Unprotect Sector command -40H, the automatic Unprotect operation begins on the rising edge of the last $\overline{CE}$ pulse in the command sequence and terminates when the Status on DQ7 is '1' at which time the device stays at the read status register mode.

(Refer to table 3,6 and Figure 10,11)

The device remains enabled for read status register mode until the CIR contents are altered by a valid command sequence.

ABORT MODE

To activate Abort mode, a three-bus cycle operation is required. The E0H command (Refer to table 3) only stops Page program or Sector /Chip erase operation currently in progress and puts the device in Abort mode. So the program or erase operation will not be completed. Since the data in some page/sectors is no longer valid due to an incomplete program or erase operation, the program fail (Q4) or erase fail (Q5)bit will be set.

A read array command MUST be written to bring the device out of the abort state without incurring any wake up latency. Note that once device is brought out, Clear status register mode is required before a program or erase operation can be executed.

DATA PROTECTION

The MX29L1611G is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read Array mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transitions or system noise.

LOW VCC WRITE INHIBIT

To avoid initiation of a write cycle during VCC power-up and power-down, a write cycle is locked out for VCC less than VLKO(typically 1.8V). If VCC < VLKO, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the VCC level is greater than VLKO. It is the user's responsibility to ensure that the control pins are logically correct to prevent unintentional write when VCC is above VLKO.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 10ns (typical) on $\overline{CE}$ will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of $\overline{OE}$ = VIL, $\overline{CE}$ = VIH. To initiate a write cycle, $\overline{CE}$ must be a logical zero while $\overline{OE}$ is a logical one, and VPP=11V should be applied.

Figure 1. AUTOMATIC PAGE PROGRAM FLOW CHART

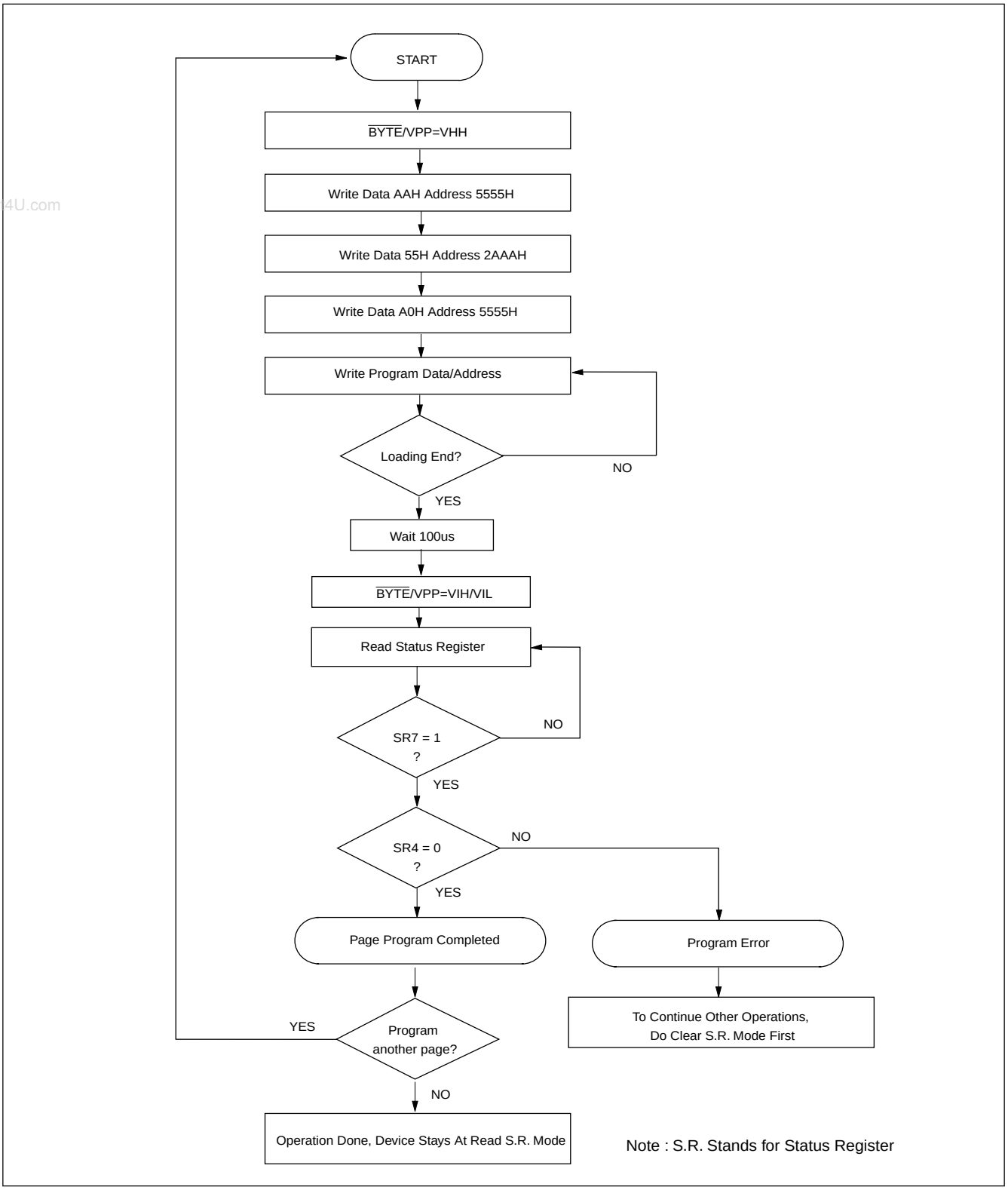


Figure 2. AUTOMATIC CHIP ERASE FLOW CHART

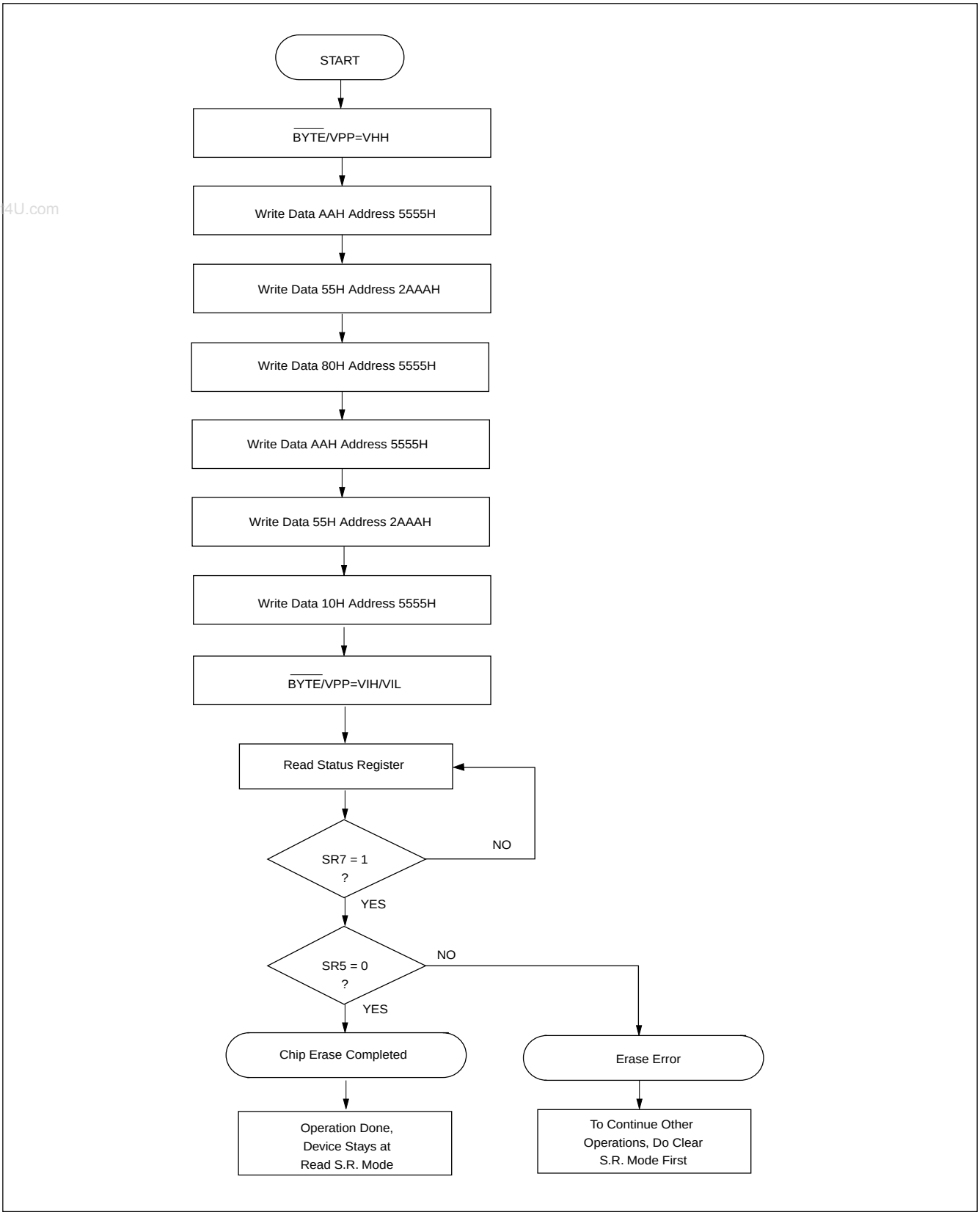
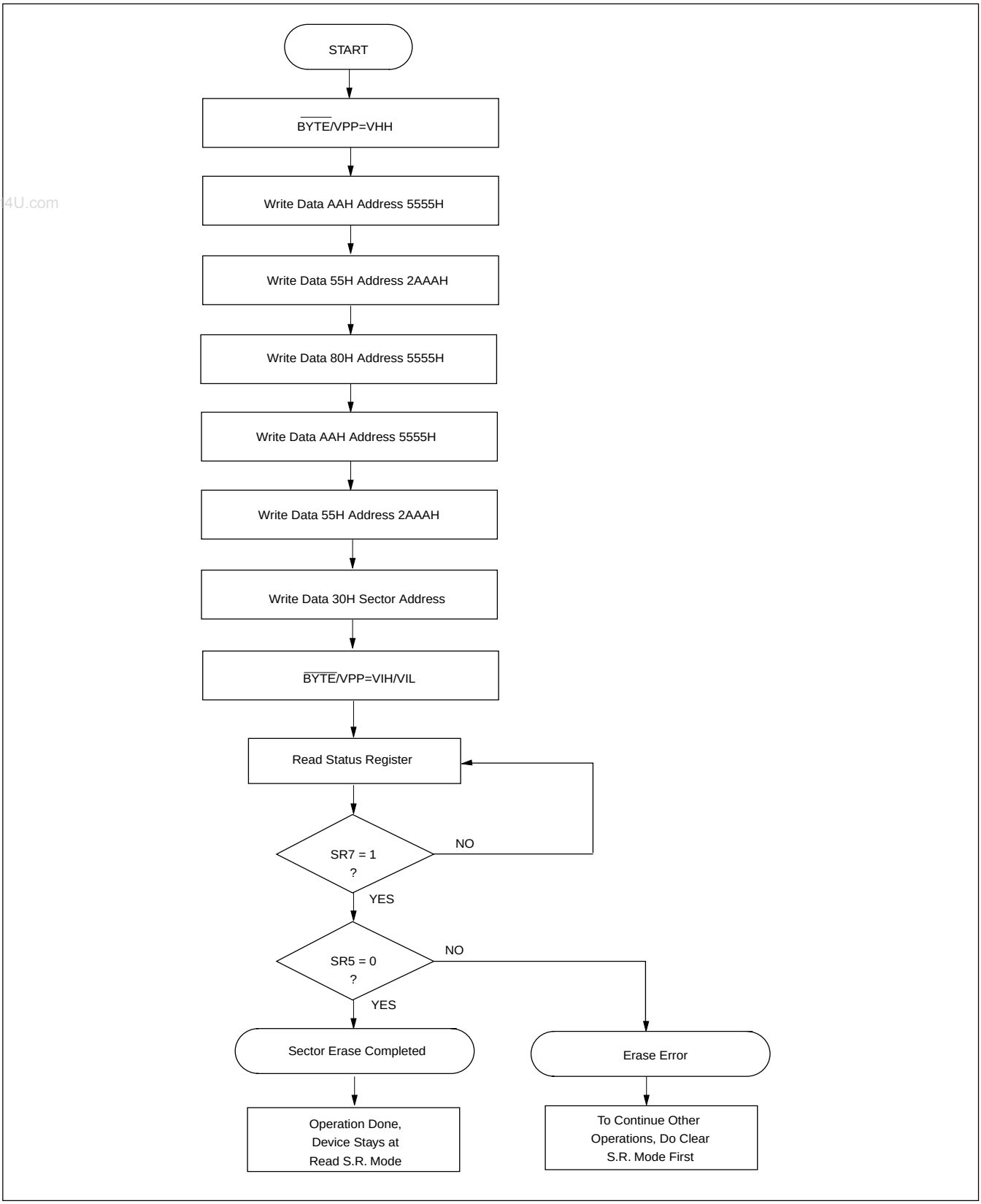


Figure 3. AUTOMATIC SECTOR ERASE FLOW CHART



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0℃ to 70℃
Storage Temperature	-65℃ to 125℃
Applied Input Voltage	-0.5V to Vcc+0.5V
Applied Output Voltage	-0.5V to Vcc+0.6V
VCC to Ground Potential	-0.5V to 4.0V
A9	-0.5V to 12.5V
$\overline{BYTE}$/VPP	-0.5V to 11.5V

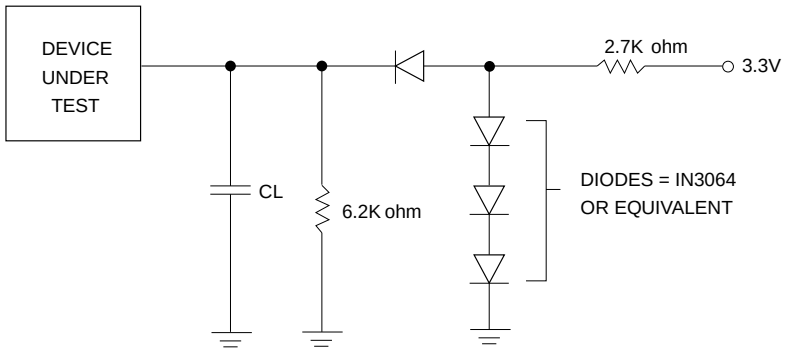
NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

CAPACITANCE TA = 25℃, f = 1.0 MHz

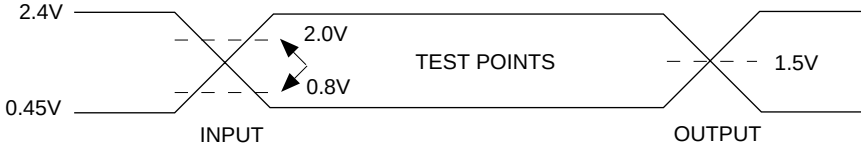
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			14	pF	VIN = 0V
COUT	Output Capacitance			16	pF	VOUT = 0V

SWITCHING TEST CIRCUITS



CL = 35 pF Including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0".
Input pulse rise and fall times are < 5ns.

DC CHARACTERISTICS VCC = 3.3V ± 10%

SYMBOL	PARAMETER	NOTES	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
IIL	Input Load Current	1			±1	uA	VCC=VCC Max VIN=VCC or GND
ILO	Output Leakage Current	1			±10	uA	VCC=VCC Max VIN=VCC or GND
ISB1	VCC Standby Current(CMOS)	1		20	50	uA	VCC=VCC Max $\overline{CE}$=VCC ± 0.2V
ISB2	VCC Standby Current(TTL)			1	2	mA	VCC=VCC Max $\overline{CE}$=VIH
ICC1	VCC Read Current	1		50	80	mA	VCC=VCC Max f=10MHz, IOUT = 0 mA
ICC2	VCC Program Current	1		15	30	mA	Program in Progress
ICC3	VCC Erase Current	1		15	30	mA	Erase in Progress
VIL	Input Low Voltage	2	-0.3		0.6	V	
VIH	Input High Voltage	3	0.7xVCC		VCC+0.3	V	
VOL	Output Low Voltage				0.45	V	IOL=2.1mA, Vcc =Vcc Min
VOH	Output High Voltage		2.4			V	IOH=-100uA, Vcc=Vcc Min

NOTES:
1. All currents are in RMS unless otherwise noted. Typical values at VCC = 3.3V, T = 25℃. These currents are valid for all product versions (package and speeds).
2. VIL min. = -1.0V for pulse width is equal to or less than 50ns.
   VIL min. = -2.0V for pulse width is equal to or less than 20ns.
3. VIH max. = VCC + 1.5V for pulse width is equal to oe less than 20ns. If VIH is over the specified maximum value, read operation cannot be guaranteed.

AC CHARACTERISTICS -- READ OPERATIONS

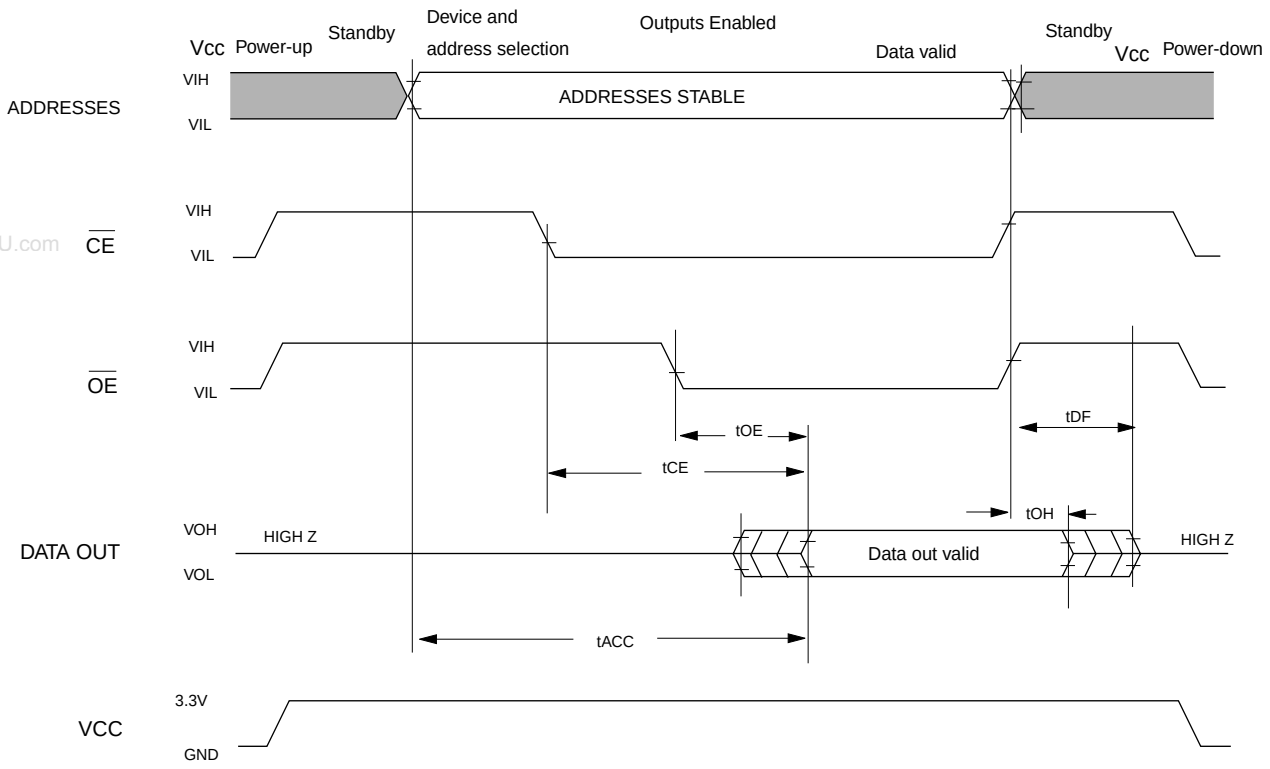
		29L1611G-90		29L1611(G)-10		29L1611G-12			
SYMBOL	DESCRIPTIONS	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT	CONDITIONS
tACC	Address to Output Delay		90		100		120	ns	$\overline{CE}$=$\overline{OE}$=VIL
tCE	$\overline{CE}$ to Output Delay		90		100		120	ns	$\overline{OE}$=VIL
tOE	$\overline{OE}$ to Output Delay		30		30		30	ns	$\overline{CE}$=VIL
tDF	$\overline{OE}$ High to Output Delay	0	20	0	20	0	20	ns	$\overline{CE}$=VIL
tOH	Address to Output hold	0		0		0		ns	$\overline{CE}$=$\overline{OE}$=VIL
tBACC	$\overline{BYTE}$ to Output Delay		100		100		120	ns	$\overline{CE}$= $\overline{OE}$=VIL
tBHZ	$\overline{BYTE}$ Low to Output in High Z		20		20		20	ns	$\overline{CE}$=VIL

TEST CONDITIONS:

- Input pulse levels: 0.45V/2.4V
- Input rise and fall times: 5ns
- Output load: 1TTL gate + 35pF(Including scope and jig)
- Reference levels for measuring timing: 1.5V

NOTE:
1. tDF is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

Figure 4.1 NORMAL READ TIMING WAVEFORMS



NOTE:

1. For real world application, BYTE/VPP pin should be either static high(word mode) or static low(byte mode); dynamic switching of BYTE/VPP pin is not recommended.

Figure 4.2 PAGE READ TIMING WAVEFORMS

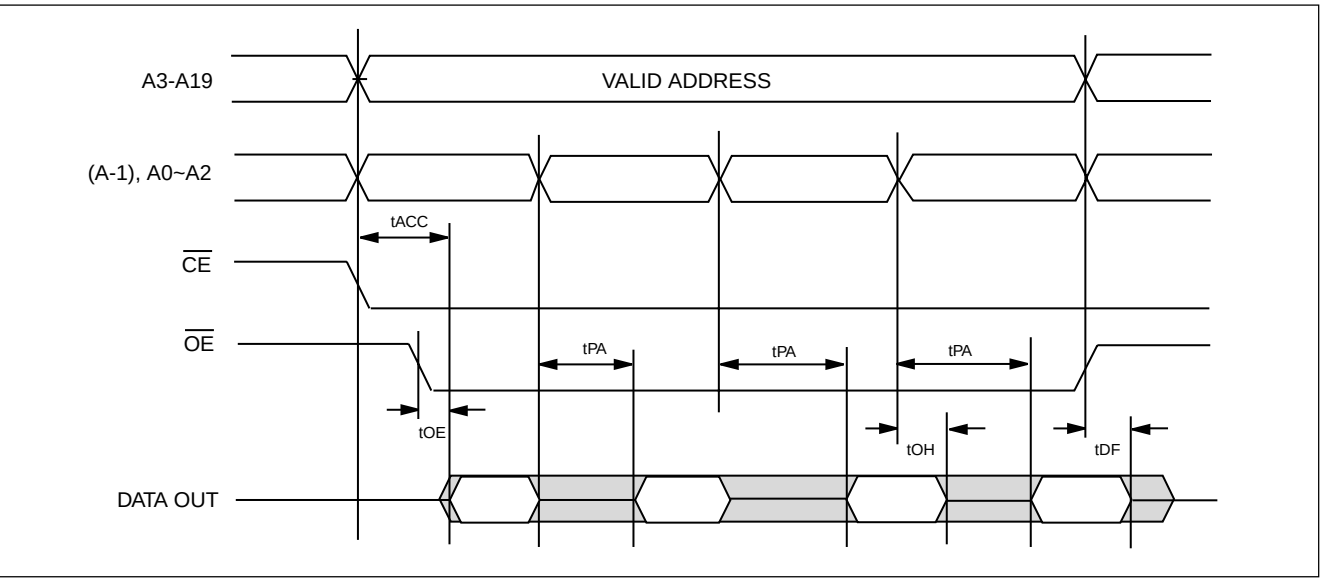
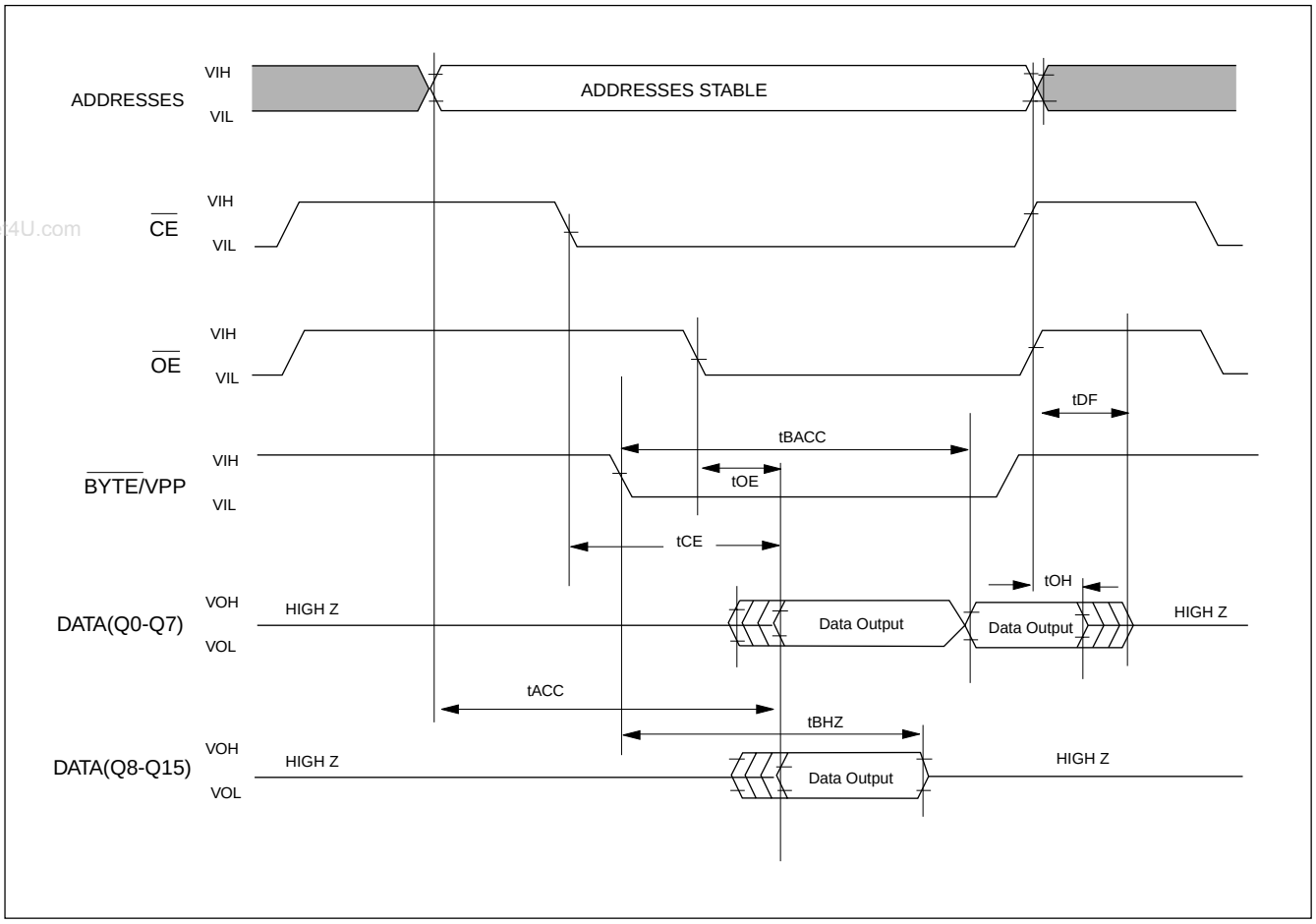


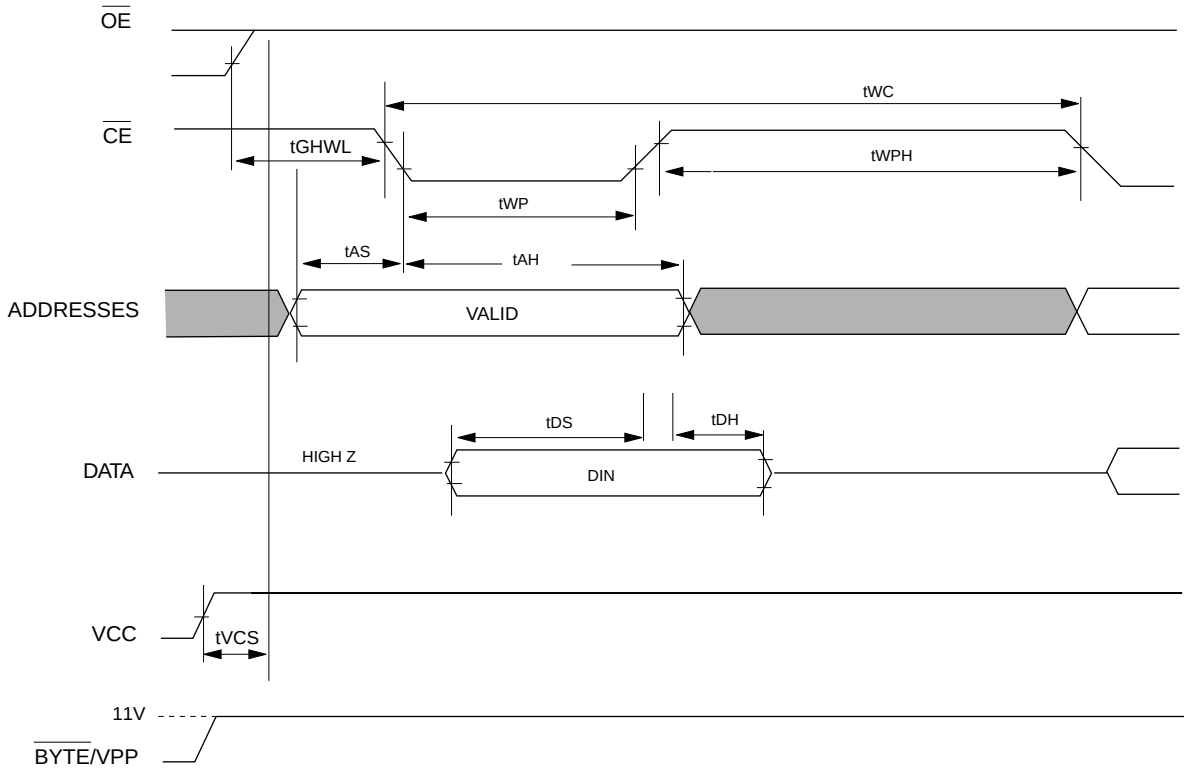
Figure 5. $\overline{\text{BYTE}}$ TIMING WAVEFORMS



AC CHARACTERISTICS -- WRITE/ERASE/PROGRAM OPERATIONS

		29L1611G-90		29L1611(G)-10		29L1611G-12		
SYMBOL	DESCRIPTION	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	UNIT
tWC	Write Cycle Time	90		100		120		ns
tAS	Address Setup Time	0		0		0		ns
tAH	Address Hold Time	60		60		60		ns
tDS	Data Setup Time	50		50		50		ns
tDH	Data Hold Time	10		10		10		ns
tCES	CE Setup Time	0		0		0		ns
tGHWL	Read Recover TimeBefore Write	0		0		0		
tWP	Write Pulse Width	60		60		60		ns
tWPH	Write Pulse Width High	40		40		40		ns
tBALC	Byte(Word) Address Load Cycle	0.3	30	0.3	30	0.3	30	us
tBAL	Byte(Word) Address Load Time	100		100		100		us
tSRA	Status Register Access Time	120		120		120		ns
tCESR	$\overline{CE}$ Setup before S.R. Read	100		100		100		ns
tVCS	VCC Setup Time	2		2		2		us
tRAW	Read Operation Set Up Time After Write		20		20		20	ns
tVPS	VPP Setup Time	2		2		2		us
tVPH	VPP Hold Time	2		2		2		us

Figure 6. COMMAND WRITE TIMING WAVEFORMS



NOTE:
1. BYTE/VPP pin should be static at 11V is equal to or less than during write operation.
2. BYTE/VPP pin should be static at TTL or CMOS level during Read operation.

Figure 7. AUTOMATIC PAGE PROGRAM TIMING WAVEFORMS

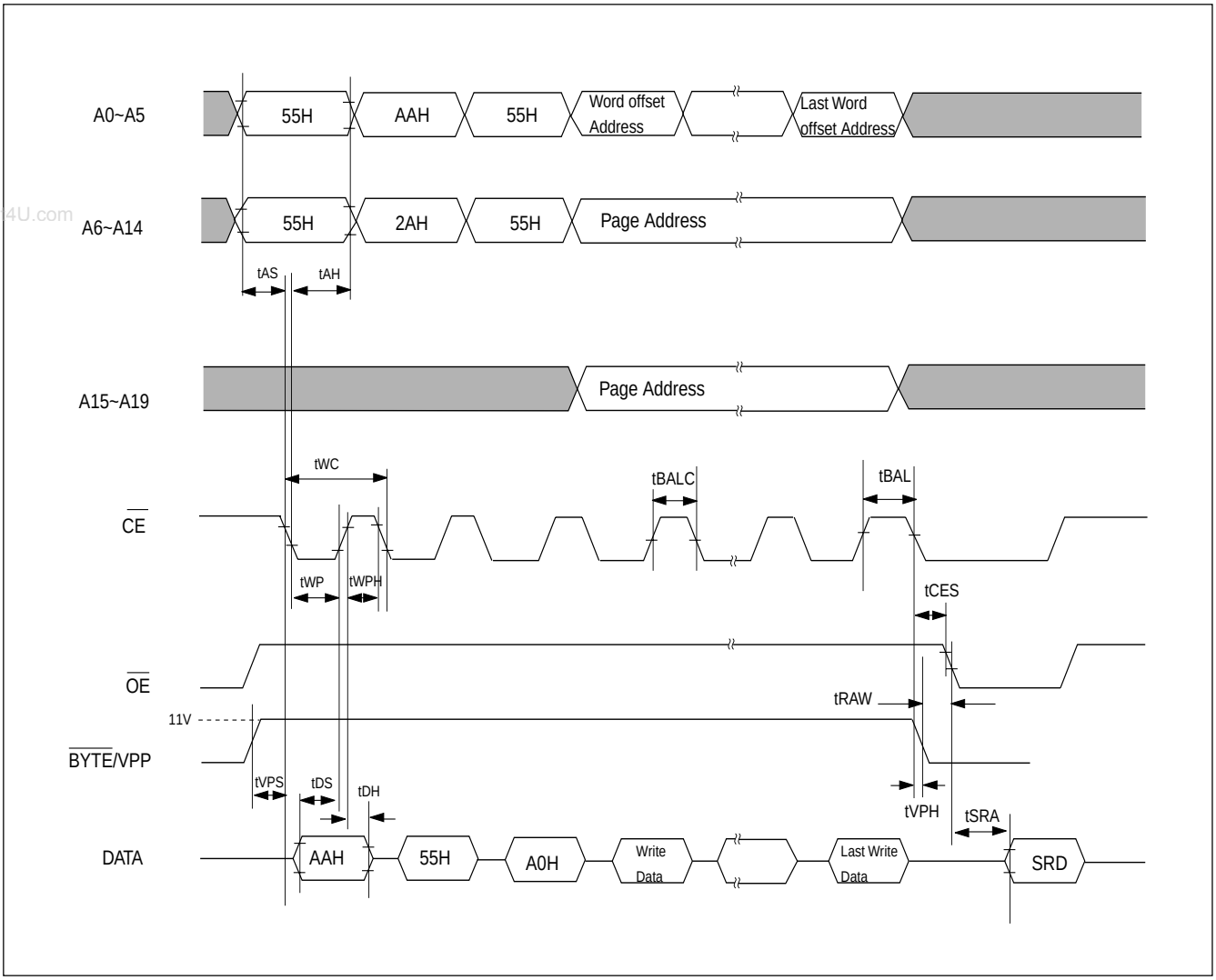
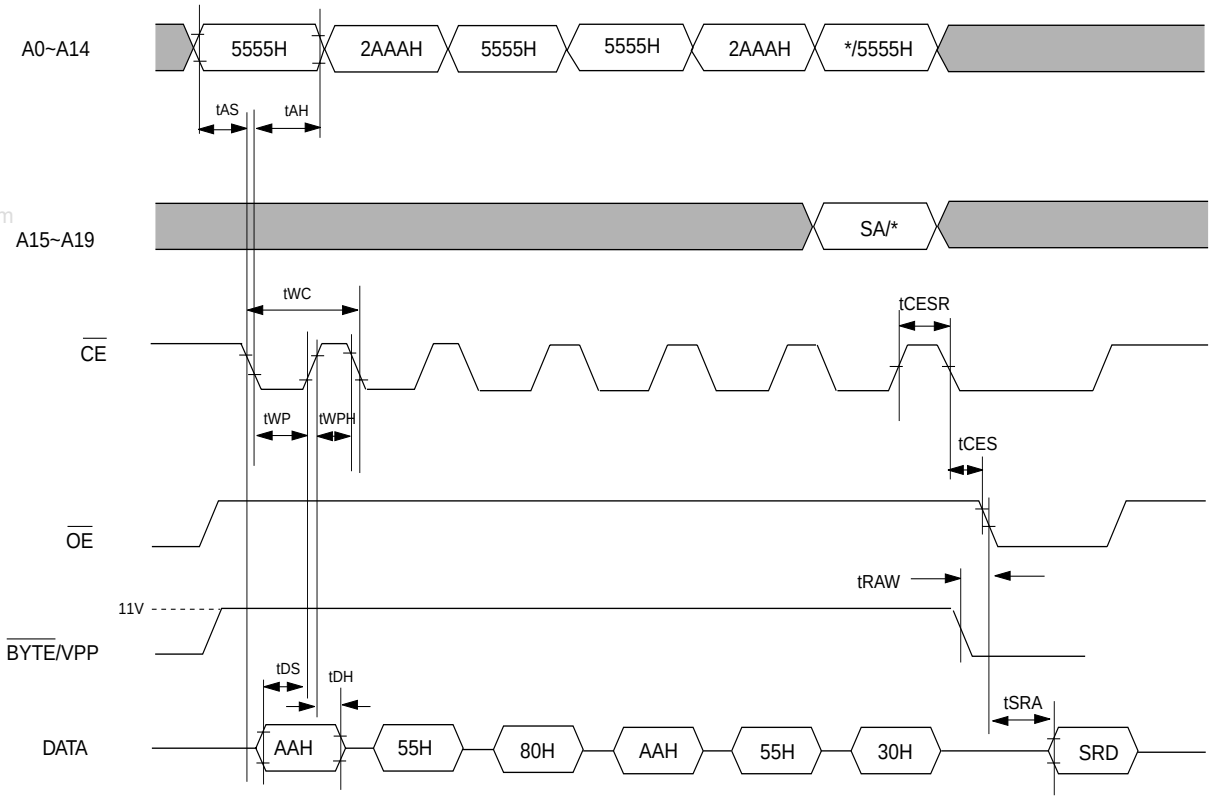


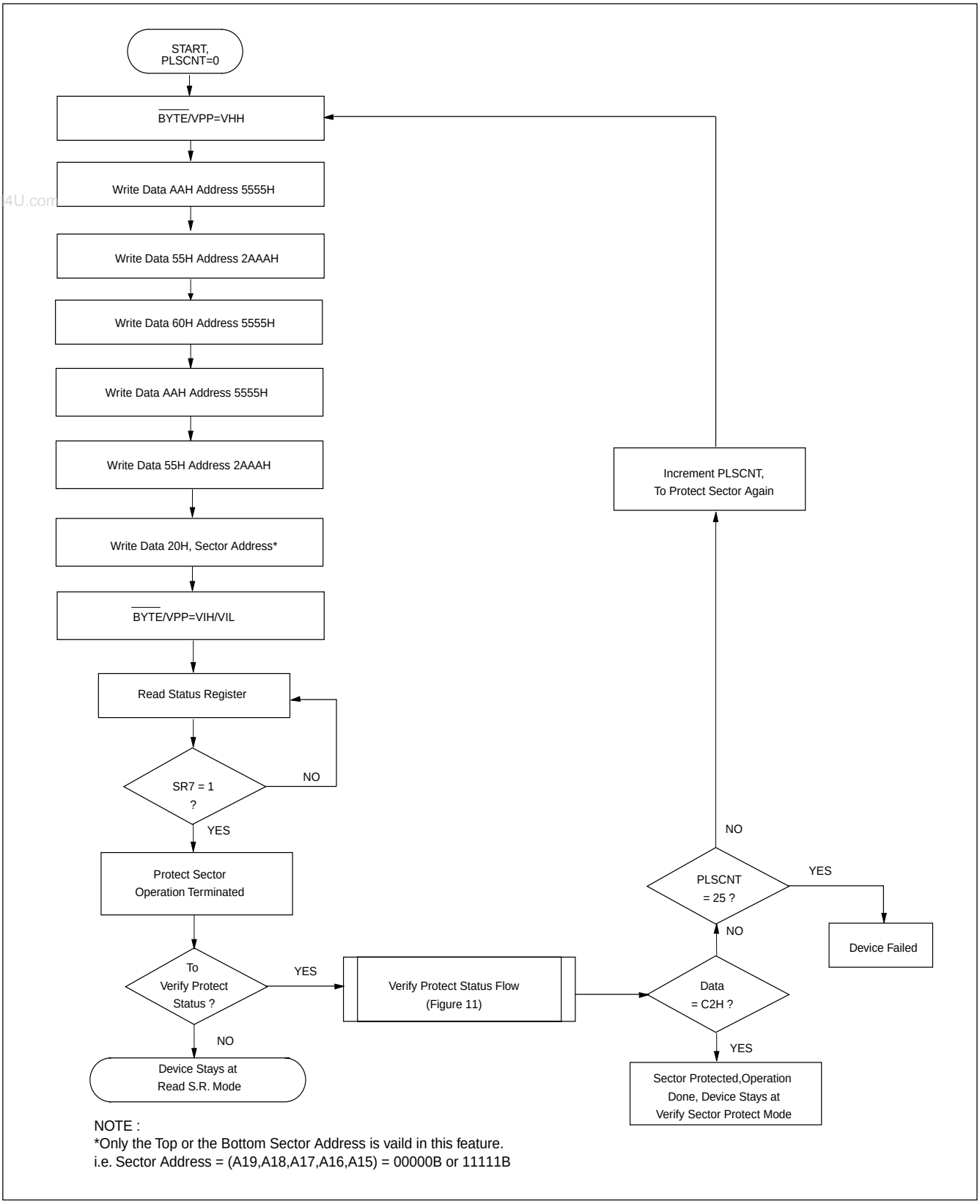
Figure 8. AUTOMATIC SECTOR/CHIP ERASE TIMING WAVEFORMS



NOTES:

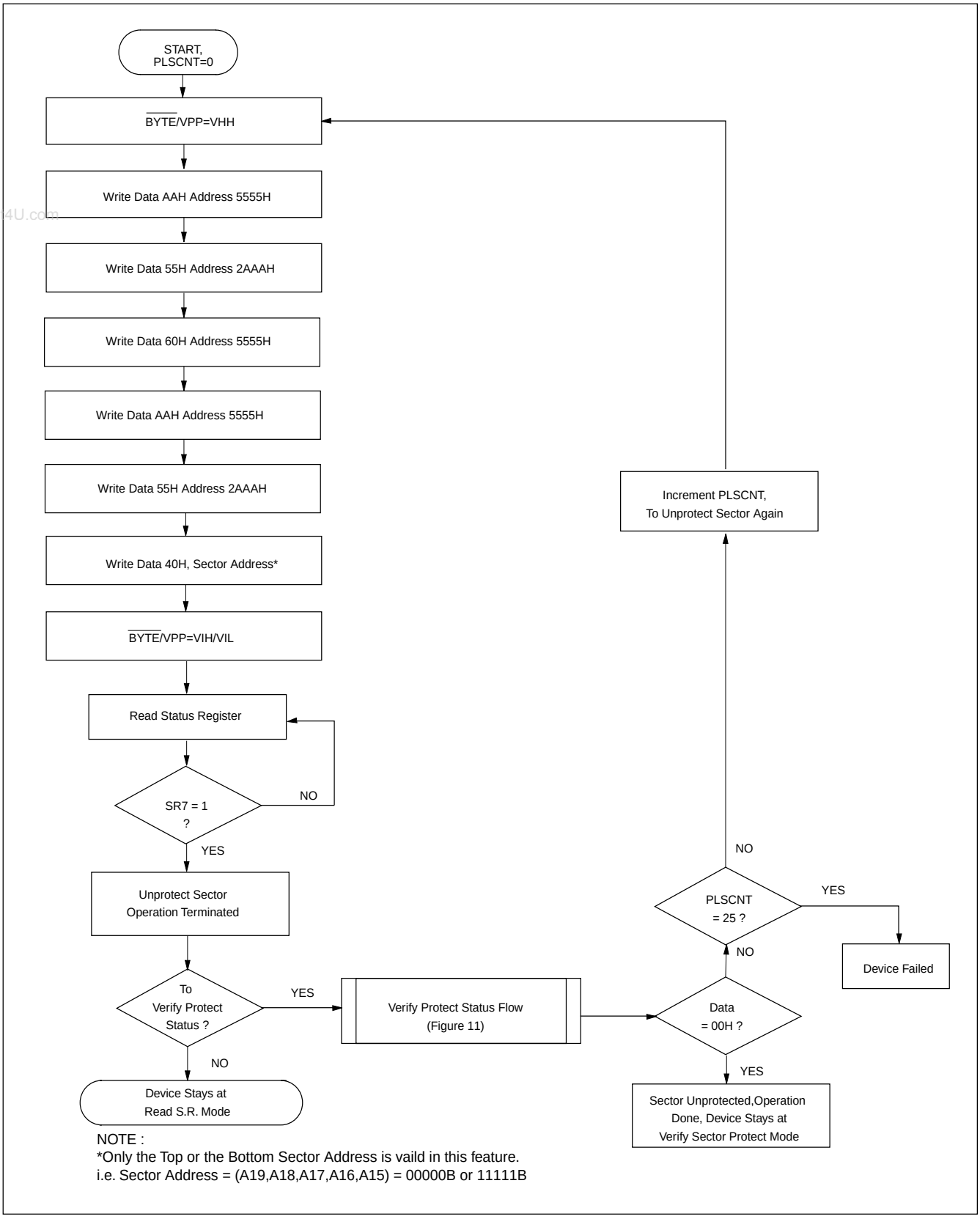
1."*" means "don't care" in this diagram.
2."SA" means "Sector Adddress".

Figure 9. SECTOR PROTECTION ALGORITHM



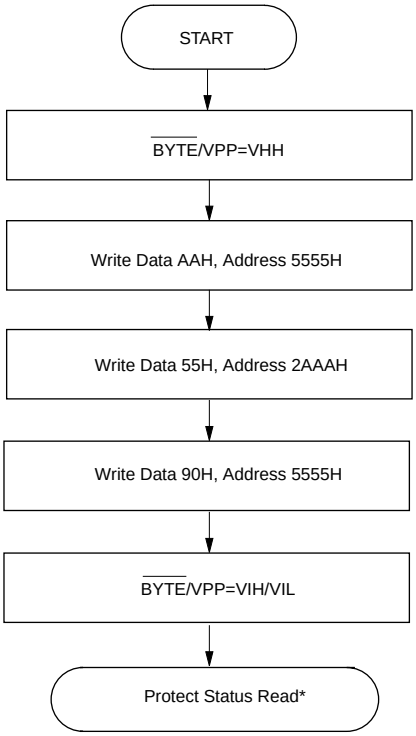
NOTE :
*Only the Top or the Bottom Sector Address is vaild in this feature.
i.e. Sector Address = (A19,A18,A17,A16,A15) = 00000B or 11111B

Figure 10. SECTOR UNPROTECT ALGORITHM



NOTE :
*Only the Top or the Bottom Sector Address is vaild in this feature.
i.e. Sector Address = (A19,A18,A17,A16,A15) = 00000B or 11111B

Figure 11. VERIFY SECTOR PROTECT FLOW CHART



* 1. Protect Status:
Data Outputs C2H as Protected Sector Verified Code.
Data Outputs 00H as Unprotected Sector Verified Code.
2. Sepecified address will be either
(A19,A18,A17,A16,A15,A1,A0) = (0000010) or (1111110),
the rest of the address pins are don't care.
3. Silicon ID can be read via this Flow Chart.
Refer to Table 4.

ERASE AND PROGRAMMING PERFORMANCE(1)

PARAMETER	LIMITS MIN.	TYP.(2)	MAX.	UNITS
Chip/Sector Erase Time		200	1600	ms
Page Programming Time		5	150	ms
Chip Programming Time		80	240	sec
Erase/Program Cycles	100			Cycles

Note:
(1).Sampled, not 100% tested. Excludes external system level over head.
(2).Typing values are measured at 25℃, noninal voltage

LATCHUP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	6.6V
Input Voltage with respect to GND on all I/O pins	-1.0V	Vcc + 1.0V
Current	-100mA	+100mA
Includes all pins except Vcc. Test conditions: Vcc = 3.3V, one pin at a time.		

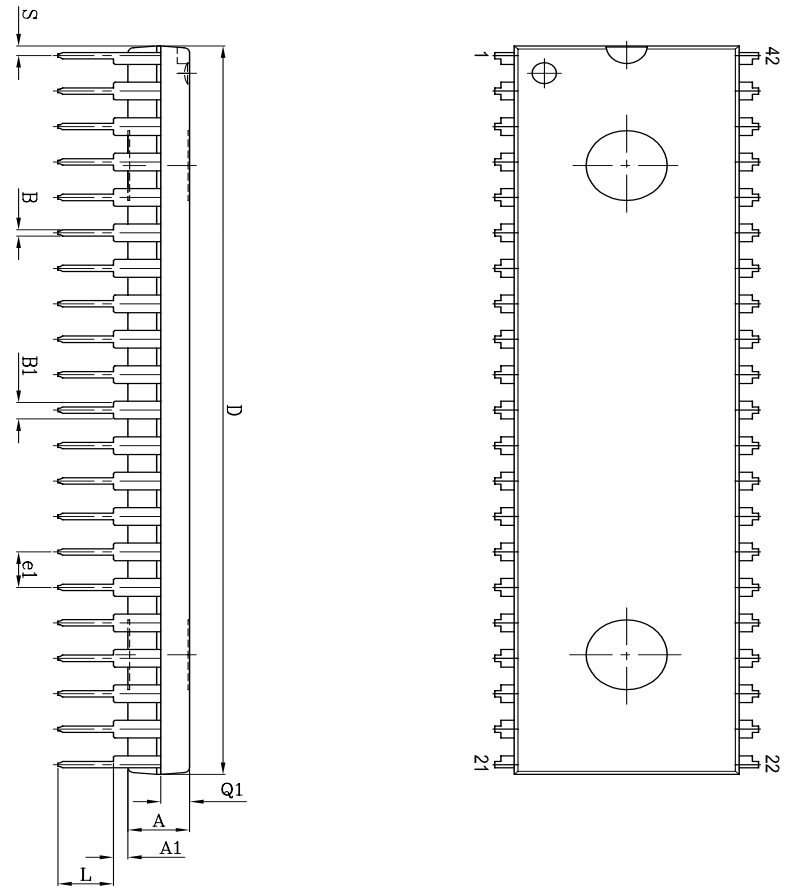
ORDER INFORMATION

PLASTIC PACKAGE

PART NO.	Access Time (ns)	Operating Current MAX.(mA)	Standby Current MAX.(uA)	PACKAGE
MX29L1611GPC-90	90	80	20	42 PDIP
MX29L1611GPC-10	100	80	20	42 PDIP
MX29L1611GPC-12	120	80	20	42 PDIP
MX29L1611PC-90	90	80	20	42 PDIP
MX29L1611PC-10	100	80	20	42 PDIP
MX29L1611PC-12	120	80	20	42 PDIP

PACKAGE INFORMATION

42-PIN PLASTIC DIP(600 mil)



UNIT / SYMBOL	INCH(BASE)	MM(REF.)
A	0.155±0.008	3.937±0.203
A1	0.025±0.005	0.635±0.127
B	0.018 (REF.)	0.457 (REF.)
B1	0.050 (REF.)	1.270 (REF.)
c	0.010 (REF.)	0.254 (REF.)
D	2.05±0.005	52.07±0.127
E	0.600±0.005	15.240±0.127
E1	0.550±0.005	13.970±0.127
e1	0.100(REF.)	2.540 (REF.)
eA	0.650±0.030	16.510±0.762
L	0.13	3.30
Q1	0.0725±0.005	1.8415±0.127
S	0.025±0.005	0.635±0.127

旺宏電子股份有限公司 Macronix International Co., Ltd.				DWG. NO.
TITLE: PACKAGE OUTLINE FOR PDIP 42L (600 MIL)				6110-0202.5
				TOLERANCE: .X ±.1 / .XX ±.01 / .XXX±.002 / ANGLE
DRAWN	APPROVED	DATE	UNIT	REVISION
C.L.Chiang	Leo Lee	05-02-'01		4

REVISION HISTORY

Revision	Description	Page	Date
0.2	Erase/programming operation voltage change(10V-->11V)	P1,4,9,14,25 P26,27	Mar/15/1999
	Modify Bus operation	P5	
	Modify command definitions	P6	
	Modify "Automatic page program time waveforms"	P26	
	Modify "Sector Protection Algorithm"	P28	
	Modify "Sector unprotect Algorithm"	P29	
	Modify "Erase and programming performance"	P31	
0.3	Description correction	P1,6,7,9,13,19 P22,23	MAR/23/1999
	Plug in $\overline{\text{BYTE}}$/VPP operation description	P15,16,17,18,28,29,30	
0.4	Delete Page mode operation	P1,9,20,22	MAY/07/1999
	Delete Erase suspard/resume operation	P6,10,12,16,17,19	
	Modify description	P1,2	
	Undate Erase and Program Performance	P30	
0.5	Change Fast random access time:100ns-->90ns	P1	APR/07/2000
	Change 29L1611G-10-->29L1611G-90 tACC:100-->90, tCE:100-->90	P20	
	Change Verify Protect Status Flow(Figure 12)-->(Figure 11)	P27,28	
0.6	Modify AC Characteristics 29L1611G-10-->29L1611G-90 ; tWC:120-->90	P23 P23	APR/18/2000
0.7	Correct ID Binay Code from 1000 to 0110	P8	JUL/10/2001
	Modify Package Information	P31	
0.8	1.Add Page Read 30ns	P1	JAN/24/2002
	2.Add Page Read	P9	
	3.Add 29L1611(G)-10	P20	
	4.Add Page Read Timing Waveform	P21	
	5.Add 29L1611(G)-10	P23	
	6.Add Order Information	P31	

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