MX26L12811MC

128M [x8/x16] SINGLE 3V PAGE MODE MTP MEMORY

FEATURES

- 3.0V to 3.6V operation voltage
- Block Structure
  - 128 x 128Kbyte Erase Blocks
- Fast random / page mode access time
  - 120/25 ns Read Access Time (page depth:4-word)
- 32-Byte Write Buffer
  - 6 us/byte Effective Programming Time

Performance

- Low power dissipation
  - typical 15mA active current for page mode read
  - 80uA/(max.) standby current
- High Performance
  - Block erase time: 2s typ.
  - Byte programming time: 210us typ.
  - Block programming time: 0.8s typ. (using Write to Buffer Command)
- Program/Erase Endurance cycles: 10 cycles

Packaging

- 44-Lead SOP

Technology

- Nbit (0.25u) MTP Technology

GENERAL DESCRIPTION

The MXIC's MX26L12811MC series MTP use the most advance 2 bits/cell Nbit technology, double the storage capacity of memory cell. The device provide the high density MTP memory solution with reliable performance and most cost-effective.

The device organized as by 8 bits or by 16 bits of output bus. The device is packaged in 44-Lead SOP. It is designed to be reprogrammed and erased in system or in standard EPROM programmers.

The device offers fast access time and allowing operation of high-speed microprocessors without wait states. The device augment EPROM functionality with in-circuit electrical erasure and programming. The device uses a command register to manage this functionality.

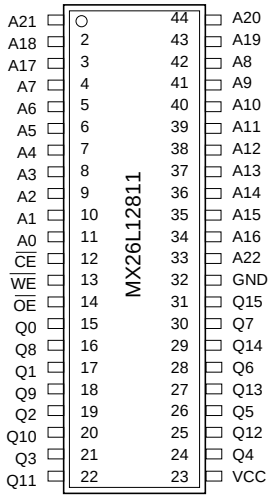
The MXIC's Nbit technology reliably stores memory contents even after the specific erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms by utilizing the dielectric's character to trap or release charges from ONO layer.

The device uses a 3.0V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamps on address and data pin from -1V to VCC + 1V.

PIN CONFIGURATION

44-SOP (for word mode only)



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A22	Address Input
Q0~Q15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VCC	Device Power Supply
GND	Device Ground

BLOCK DIAGRAM

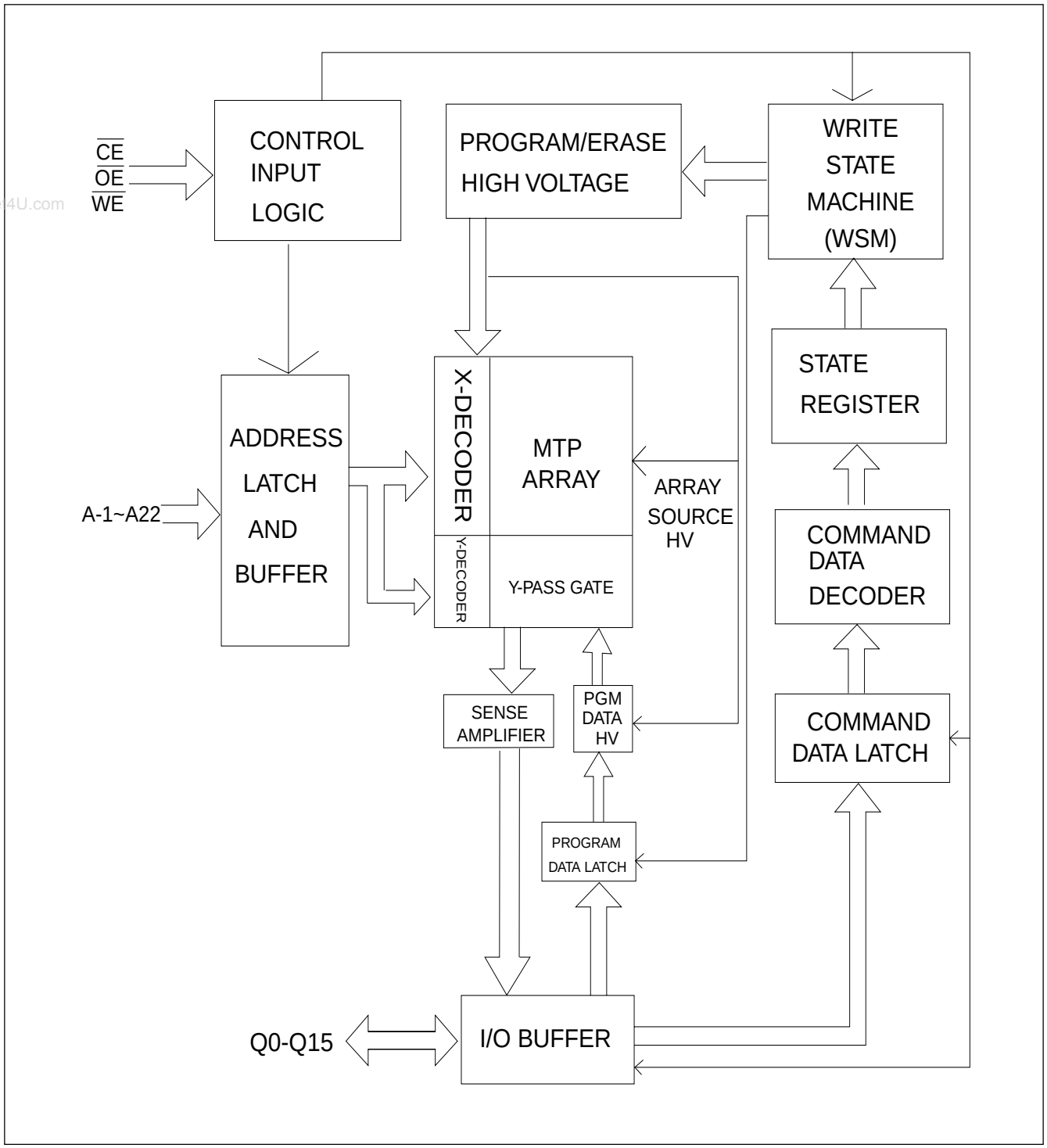


Figure 1. Block Architecture

MTP memory reads erases and writes in-system via the local CPU. All bus cycles to or from the MTP memory conform to standard microprocessor bus cycles.

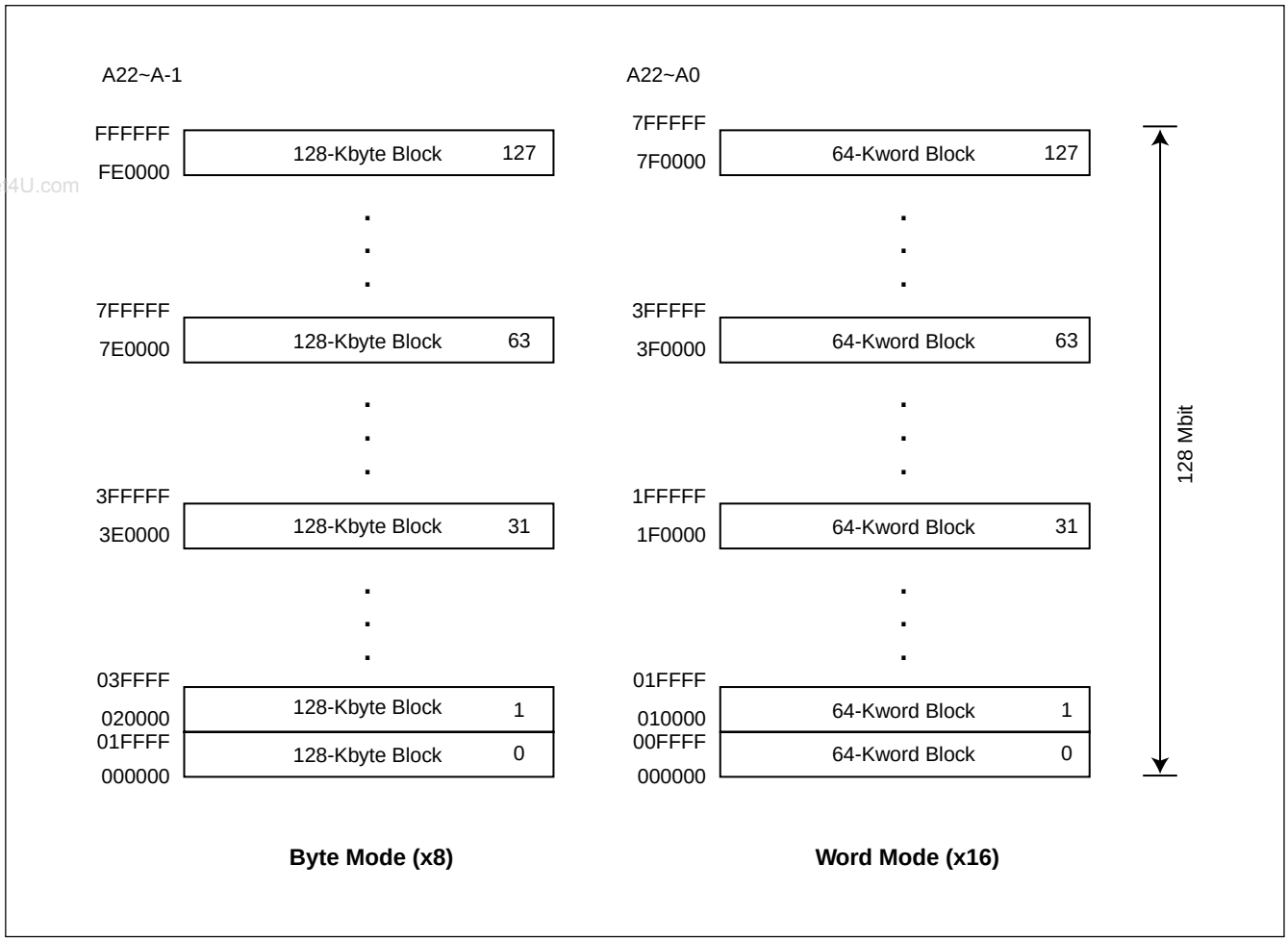


Table 1. Bus Operations

Command Sequence	Read Array	Output Disable	Standby	Read ID	Read Query	Read Status (WSM off)	Read Status (WSM on)	Write
Notes	3							6,7
$\overline{CE}$	Enabled	Enabled	Disabled	Enabled	Enabled	Enabled	Enabled	Enabled
$\overline{OE}$ (1)	VIL	VIH	X	VIL	VIL	VIL	VIL	VIH
$\overline{WE}$ (1)	VIH	VIH	X	VIH	VIH	VIH	VIH	VIL
Address	X	X	X	See Figure 2	See Table 6	X	X	X
Q (2)	Data out	High Z	High Z	Note 4	Note 5	Data out	Q7=Data out Q15-8=High Z Q6-0=High Z	Data in

NOTES:
1. $\overline{OE}$ and $\overline{WE}$ should never be enabled simultaneously.
2. DQ refers to Q0-Q7 if $\overline{BYTE}$ is low and Q0-Q15 if $\overline{BYTE}$ is high.
3. X can be VIL or VIH for control and address pins.
4. See Section , "Read Identifier Codes" for read identifier code data.
5. See Section , "Read Query Mode Command" for read query data.
6. Command writes involving block erase, program, or lock-bit configuration are reliably executed when VCC is within specification.
7. Refer to Table 2 on page 7 for valid DIN during a write operation.

FUNCTION

The device includes on-chip program/erase control circuitry. The Write State Machine (WSM) controls block erase and word/page program operations. Operational modes are selected by the commands written to the Command User Interface (CUI). The Status Register indicates the status of the WSM and when the WSM successfully completes the desired program or block erase operation.

READ

The device has three read modes, which accesses to the memory array, the Device Identifier or the Status Register. The appropriate read command are required to be written to the CUI. Upon initial device powerup or after exit from powerdown, the device automatically resets to read array mode. In the read array mode, low level input to $\overline{CE}$ and $\overline{OE}$, high level input to $\overline{WE}$ and address signals to the address inputs (A22-A-1) output the data of the addressed location to the data input/output (Q15~Q0).

When reading information in read array mode, the device defaults to asynchronous page mode. In this state, data is internally read and stored in a high-speed page buffer. A2:0 addresses data in the page buffer. The page size is 4 words or 8 bytes. Asynchronous word/byte mode is supported with no additional commands required.

WRITE

Writes to the CUI enables reading of memory array data, device identifiers and reading and clearing of the Status Register. The CUI is written when the device is enable, $\overline{WE}$ is active and $\overline{OE}$ is at high level. Address and data are latched on the earlier rising edge of $\overline{WE}$ and $\overline{CE}$. Standard micro-processor write timings are used.

OUTPUT DISABLE

When $\overline{OE}$ is at VIH, output from the devices is disabled. Data input/output are in a high-impedance(High-Z) state.

STANDBY

When $\overline{CE}$ disable the device (see table1) and place it in standby mode. The power consumption of this device is reduced. Data input/output are in a high-impedance(High-Z) state. If the memory is deselected during block erase, program or lock-bit configuration, the internal control circuits remain active and the device consume normal active power until the operation completes.

COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the CUI. Table 2 defines the valid register command sequences.

Table 2. Command Definitions

Command Sequence		Read Array	Read ID	Read Query	Read Status Register	Clear Status Register	Write to Buffer
Notes			5		6		7,8,9
Bus Write Cycles Req'd		1	≥ 2	≥ 2	2	1	> 2
First Bus Write Cycles	Operation(2)	Write	Write	Write	Write	Write	Write
	Address(3)	X	X	X	X	X	BA
	Data(4,5)	FFH	90H	98H	70H	50H	E8H
Second Bus Read Query	Operation(2)		Read	Read	Read		Write
	Address(3)		IA	QA	X		BA
	Data(4,5)		ID	QD	SRD		N

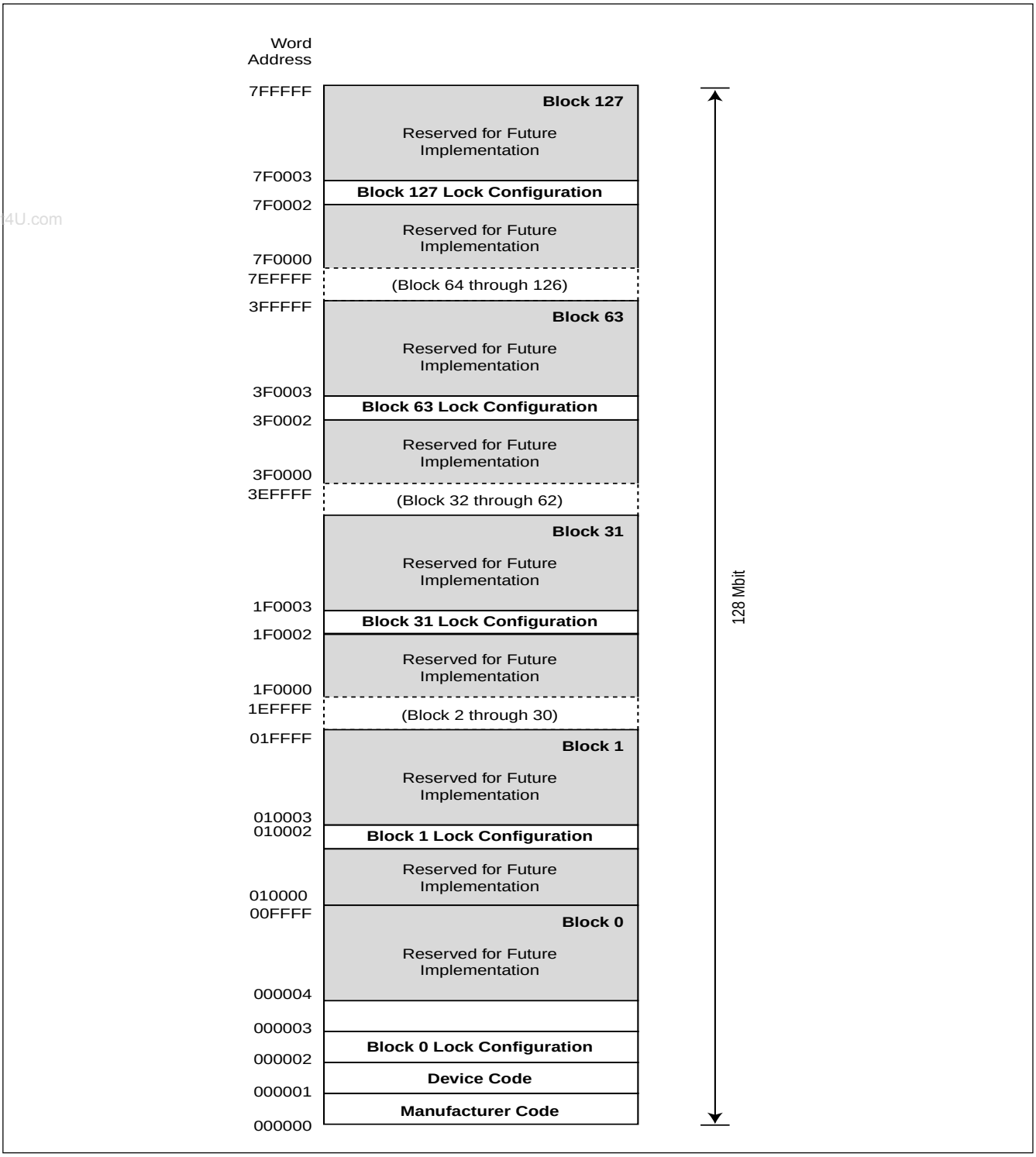
Command Sequence		Word Program	Sector Erase	Configur-ation	Set Sector Lock-Bit	Clear Sector Lock-Bit
Notes		10,11	9,10			12
Bus Write Cycles Req'd		2	2	2	2	2
First Bus Write Cycle	Operation(2)	Write	Write	Write	Write	Write
	Address(3)	X	BA	X	X	X
	Data(4,5)	40H/10H	20H	B8H	60H	60H
Second Bus Write Cycle	Operation(2)	Write	Write	Write	Write	Write
	Address(3)	PA	PA	X	BA	X
	Data(4,5)	PD	D0H	CC	01H	D0H

NOTES:

1. Bus operations are defined in Table 1.
2. X = Any valid address within the device.
   BA = Address within the block.
   IA = Identifier Code Address: see Figure 2 and Table 13.
   QA = Query database Address.
   PA = Address of memory location to be programmed.
   RCD = Data to be written to the read configuration register. This data is presented to the device on A15~A0 ; all other address inputs are ignored.

3. ID = Data read from Identifier Codes.
   QD = Data read from Query database.
   SRD = Data read from status register. See Table 14 for a description of the status register bits.
   PD = Data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
   CC = Configuration Code.
4. The upper byte of the data bus (Q8-Q15) during command writes is a "Don't Care" in x16 operation.
5. Following the Read Identifier Codes command, read operations access manufacturer, device and block lock codes. See Section 4.3 for read identifier code data.
6. If the WSM is running, only Q7 is valid; Q15-Q8 and Q6-Q0 float, which places them in a high impedance state.
7. After the Write to Buffer command is issued check the XSR to make sure a buffer is available for writing.
8. The number of bytes/words to be written to the Write Buffer = N + 1, where N = byte/word count argument. Count ranges on this device for byte mode are N = 00H to N = 1FH and for word mode are N = 0000H to N =000FH. The third and consecutive bus cycles, as determined by N, are for writing data into the Write Buffer. The Confirm command (D0H) is expected after exactly N + 1 write cycles; any other command at that point in the sequence aborts the write to buffer operation. Please see Figure 4. "Write to Buffer Flowchart" for additional information.
9. The write to buffer or erase operation does not begin until a Confirm command (D0h) is issued.
10. Attempts to issue a block erase or program to a locked block.
11. Either 40H or 10H are recognized by the WSM as the byte/word program setup.
12. The clear block lock-bits operation simultaneously clears all block lock-bits.

Figure 2. Device Identifier Code Memory Map



NOTE:

1. A-1 is not used in either x8 or x16 mode when obtaining these identifier codes. Data is always given on the low byte in x16 mode (upper byte contains 00h).

Read Array Command

The device is in Read Array mode on initial device power up and after exit from power down, or by writing FFH to the Command User Interface. The read configuration register defaults to asynchronous read page mode. The device remains enabled for reads until another command is written.

DEVICE OPERATION

SILICON ID READ

The Silicon ID Read mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the two cycle "Silicon ID Read" command is requested. (The command sequence is illustrated in Table 3.

During the "Silicon ID Read" Mode, manufacturer's code (MXIC=C2H) can be read out by setting A0=VIL and device identifier can be read out by setting A0=VIH.

To terminate the operation, it is necessary to write the read command. The "Silicon ID Read" command is valid only when the WSM is off.

Table 3. MX26L12811MC Silicon ID Codes and Verify Sector Protect Code

Type	Address (1)	Code (HEX)	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
Manufacture Code	00000	C2H	1	1	0	0	0	0	1	0
Device Code	00001	(00) 74H	0	1	1	1	0	1	0	0
Block Lock Configuration	X0002 (2)									
- Block is Unlocked		DQ0=0								
- Block is Locked		DQ0=1								
- Reserved for Future Use		DQ1-7								

Notes:
1. The lowest order address line is A0.
2. X selects the specific blocks lock configuration code.

Table 4. Status Register Definitions

Symbol	High Z When Busy?	Status	Definition		Notes
			"1"	"0"	
SR.7	No	WRITE STATE MACHINE STATUS	Ready	Busy	1
SR.6	Yes	RESERVED			
SR.5	Yes	ERASE AND CLEAR LOCK-BITS STATUS	Error in Block Erasure or Clear Lock-Bits	Successful Block Erase or Clear Lock-Bits	2
SR.4	Yes	PROGRAM AND SET LOCK-BIT STATUS	Error in Setting Lock-Bit	Successful Set Block Lock Bit	
SR.3	Yes	PROGRAMMING VOLTAGE STATUS	Low Programming Voltage Detected, Operation Aborted	Programming Voltage OK	3
SR.2	Yes	RESERVED			
SR.1	Yes	DEVICE PROTECT STATUS	Block Lock-Bit Detected, Operation Abort	Unlock	4
SR.0	Yes	RESERVED			5

Notes

1. Check STS or SR.7 to determine block erase, program, or lock-bit configuration completion. SR.6-SR.0 are not driven while SR.7 = 0
2. If both SR.5 and SR.4 are "1" after a block erase or lock-bit configuration attempt, an improper command sequence was entered.
3. SR.3 does not provide a continuous programming voltage level indication. The WSM interrogates and indicates the programming voltage level only after Block Erase, Program, Set Block Lock-Bit, or Clear Block Lock-Bits command sequences.
4. SR.1 does not provide a continuous indication of block lock-bit values. The WSM interrogates the block lock-bits only after Block Erase, Program, or Lock-Bit configuration command sequences. It informs the system, depending on the attempted operation, if the block lock-bit is set. Read the block lock configuration codes using the Read Identifier Codes command to determine block lock-bit status.
5. SR.0 is reserved for future use and should be masked when polling the status register.

Table 5. Extended Status Register Definitions

Symbol	High Z When Busy?	Status	Definition		Notes
			"1"	"0"	
XSR.7	No	WRITE BUFFER STATUS	Write buffer available	Write buffer not available	1
XSR.6-XSR.0	Yes	RESERVED			2

Notes:

1. After a Buffer-Write command, XSR.7 = 1 indicates that a Write Buffer is available.
2. XSR.6-XSR.0 are reserved for future use and should be masked when polling the status register.

READ STATUS REGISTER COMMAND

The Status Register is read after writing the Read Status Register command of 70H to the Command User Interface. Also, after starting the internal operation the device is set to the Read Status Register mode automatically.

The contents of Status Register are latched on the later falling edge of $\overline{OE}$ or the first edge of $\overline{CE}$ that enables the device $\overline{OE}$ must be toggle to VIH or the device must be disable before further reads to update the status register latch.

CLEAR STATUS REGISTER COMMAND

The Erase Status, Program Status, Block Status bits and protect status are set to "1" by the Write State Machine and can only be reset by the Clear Status Register command of 50H. These bits indicates various failure conditions.

BLOCK ERASE COMMAND

Automated block erase is initiated by writing the Block Erase command of 20H followed by the Confirm command of D0H. An address within the block to be erased is required (erase changes all block data to FFH).

Block preconditioning, erase, and verify are handled internally by the WSM (invisible to the system). The CPU can detect block erase completion by analyzing the output of status register bit SR.7. Toggle $\overline{OE}$, $\overline{CE}$ to update the status register. The CUI remains in read status register mode until a new command is issued.

WRITE TO BUFFER COMMAND

To program the device, a Write to Buffer command is issue first. A variable number of bytes, up to the buffer size, can be loaded into the buffer and written to the MTP device. First, the Write to Buffer Setup command is issued along with the Block Address (see Figure 3, Write to Buffer Flowchart on page 15). After the command is issued, the extended Status Register (XSR) can be read when $\overline{CE}$ is VIL. XSR.7 indicates if the Write Buffer is available.

If the buffer is available, the number of words/bytes to be program is written to the device. Next, the start address is given along with the write buffer data. Subsequent writes provide additional device addresses and data, depending on the count. After the last buffer data is given, a Write Confirm command must be issued. The WSM beginning copy the buffer data to the MTP array.

If an error occurs while writing, the device will stop writing, and status register bit SR.4 will be set to a "1" to indicate a program failure. The internal WSM verify only detects errors for "1" that do not successfully program to "0" . If a program error is detected, the status register should be cleared. Any time SR.4 and/or SR.5 is set, the device will not accept any more Write to Buffer commands. Reliable buffered writes can only occur when VCC is valid. Also, successful programming requires that the corresponding block lock-bit be reset.

BYTE/WORD PROGRAM COMMANDS

Byte/Word program is executed by a two-command sequence. The Byte/Word Program Setup command of 40H is written to the Command Interface, followed by a second write specifying the address and data to be written. The WSM controls the program pulse application and verify operation. The CPU can detect the completion of the program event by analyzing the STS pin or status register bit SR.7.

Successful byte/word programs require that the corresponding block lock-bit be cleared. If a byte/ word program is attempted when the corresponding block lock-bit is set, SR.1 and SR.4 will be set to "1".

Read Configuration

The device will support both asynchronous page mode and standard word/byte reads. No configuration is required. Status register and identifier only support standard word/byte single read operations.

Table 6. Read Configuration Register Definition

RM	R	R	R	R	R	R	R
15(A15)	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

	Notes
RCR.15 = READ MODE (RM) 0 = Standard Word/Byte Reads Enabled (Default) 1 = Page-Mode Reads Enabled	Read mode configuration effects reads from the MTP array. Status register, query, and identifier reads support standard word/byte read cycles.
RCR.14-1= RESERVED FOR FUTURE ENHANCEMENTS (R)	These bits are reserved for future use. Set these bits to "0".

Set Block Lock-Bit Commands

This device provided the block lock-bits, to lock and unlock the individual block. To set the block lock-bit, the two cycle Set Block Lock-Bit command is requested. This command is invalid while the WSM is running or the device is suspended. Writing the set block lock-bit command of 60H followed by confirm command and an appropriate block address. After the command is written, the device automatically outputs status register data when read. The CPU can detect the completion of the set lock-bit event by analyzing the STS pin output or status register bit SR.7. Also, reliable operations occur only when VCC is valid.

Clear Block Lock-Bits Command

All set block lock-bits can clear by the Clear Block Lock-Bits command. This command is invalid while the WSM is running or the device is suspended. To Clear the block lock-bits, two cycle command is requested . The device automatically outputs status register data when read. The CPU can detect completion of the clear block lock-bits event by analyzing status register bit SR.7. If a clear block lock-bits operation is aborted due to VCC transitioning out of valid range, block lock-bit values are left in an undetermined state. A repeat of clear block lock-bits is required to initialize block lock-bit contents to known values.

VCC--TRANSITIONS

Block erase, program, and lock-bit configuration are not guaranteed if VCC falls outside of the specified operating ranges.

The CUI latches commands issued by system software and is not altered by $\overline{CE}$ transitions, or WSM actions. Its state is read array mode upon power-up, after exit from power-down mode, or after VCC transitions below VLKO.

Figure 3. Write to Buffer Flowchart

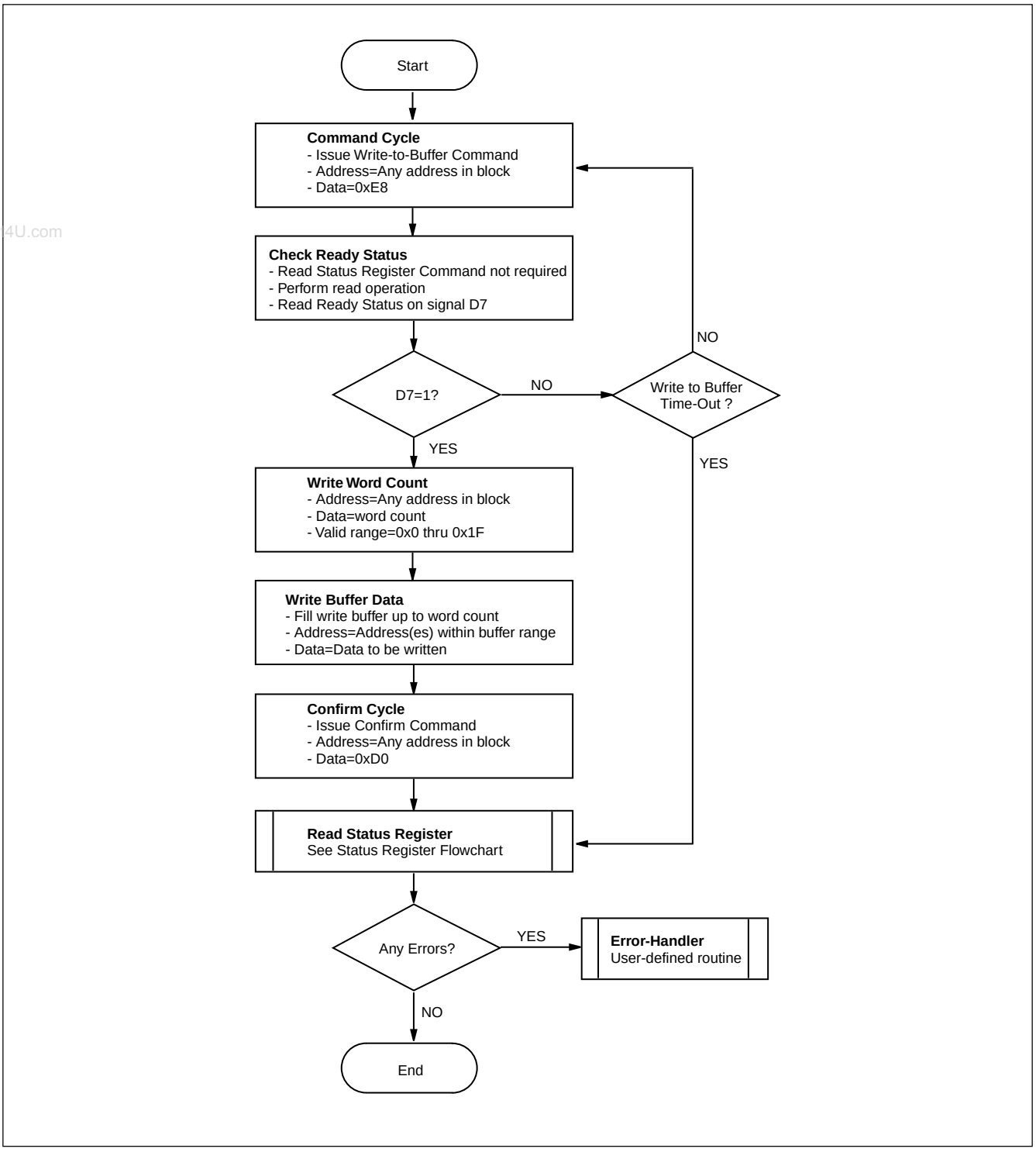


Figure 4. Status Register Flowchart

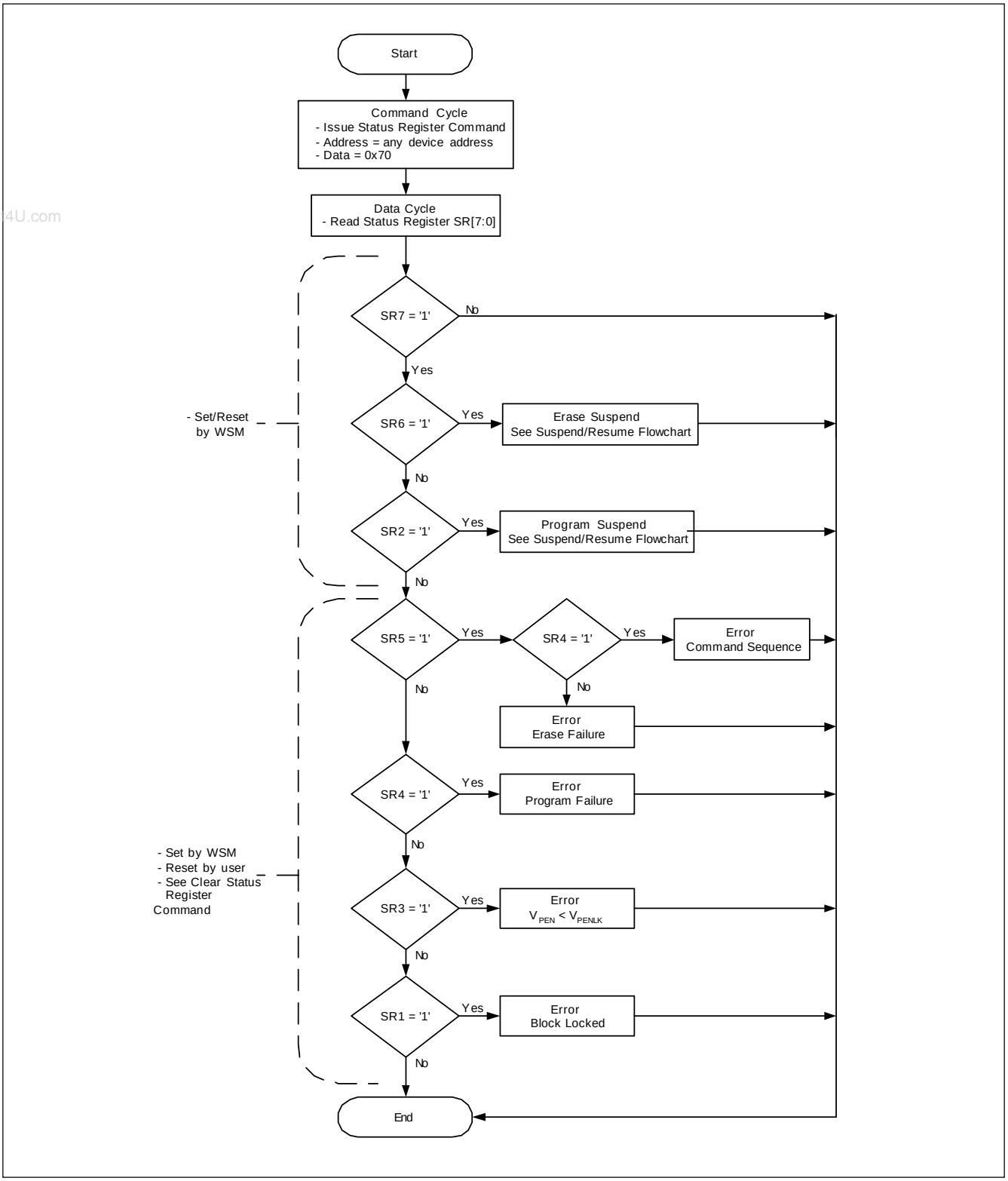
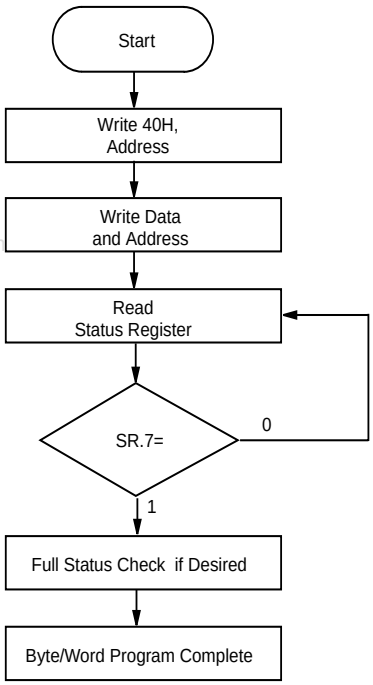


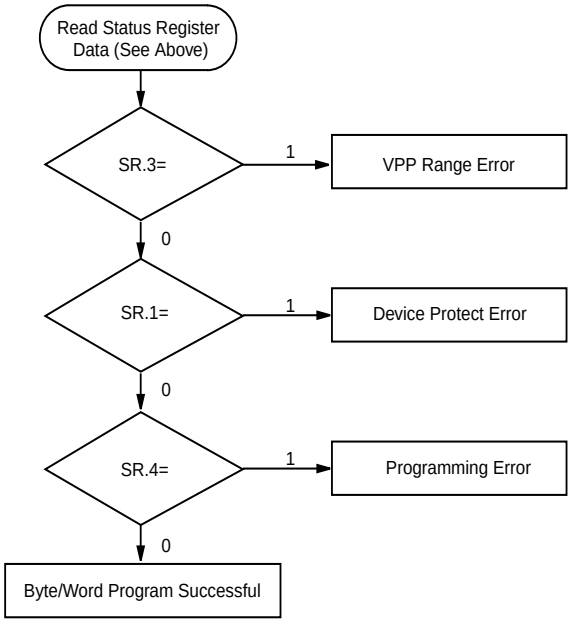
Figure 5. Byte/Word Programming Flowchart



Bus Operation	Command	Comments
Write	Setup Byte/ Word Program	Data=40H Addr=Location to Be Programmed
Write	Byte/Word Program	Data=Data to Be Programmed Addr=Location to Be Programmed
Read (Note 1)		Status Register Data
Standby		Check SR.7 1=WSM Ready 0=WSM Busy

1. Toggling $\overline{OE}$ (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.
SR full status check can be done after each program operation, or after a sequence of programming operations.
Write FFH after the last program operation to place device in read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		Check SR.3 1=Programming to Voltage Error Detect
Standby		Check SR.1 1=Device Protect Detect $\overline{RP}$=VIH, Block Lock-Bit is Set Only required for systems
Standby		Check SR.4 1=Programming Error

Toggling $\overline{OE}$ (low to high to low) updates the status register. This can be done in place of issuing the Read Status Register command. Repeat for subsequent programming operations.
SR.4, SR.3, and SR.1 are only cleared by the Clear Status Register Command in cases where multiple location are programmed before full status is checked.
If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 6. Block Erase Flowchart

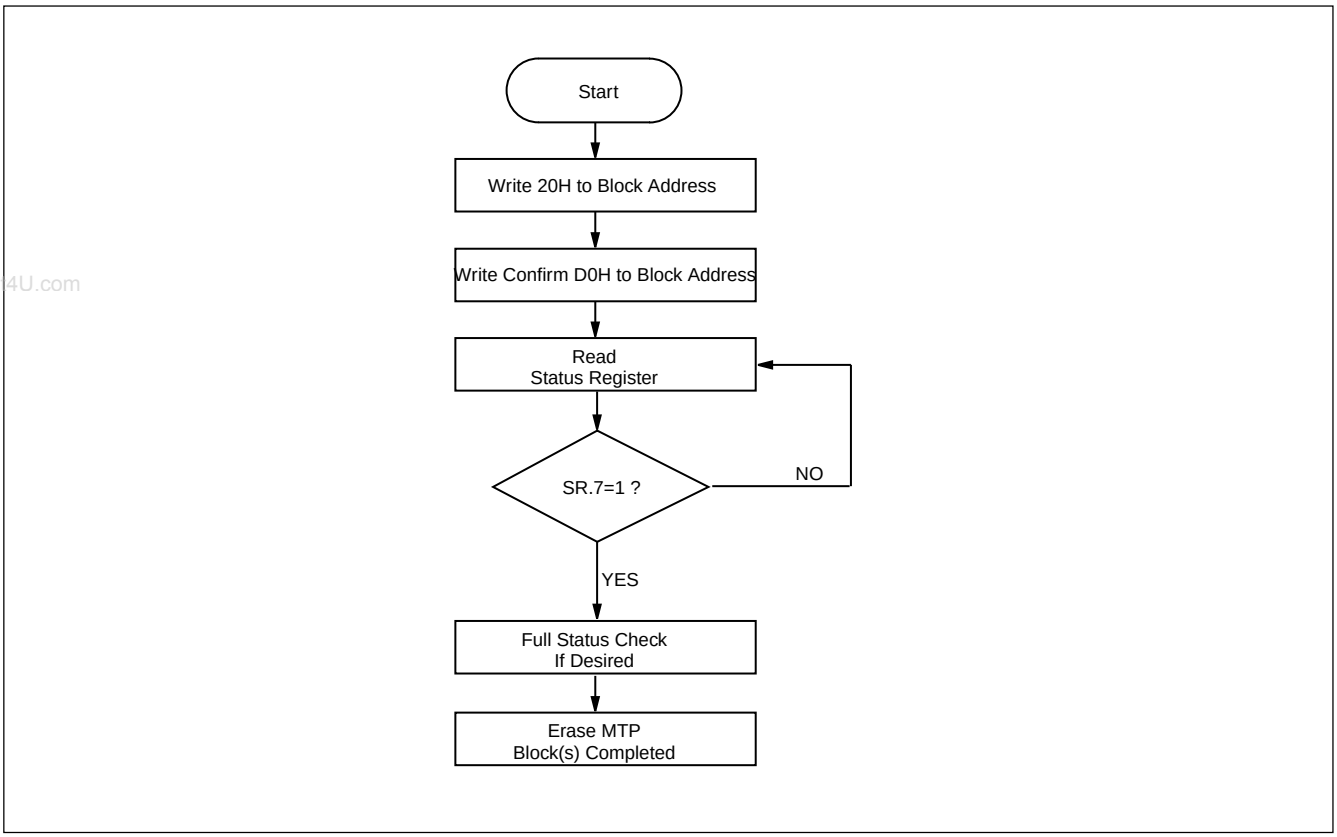


Figure 7. Set Block Lock-Bit Flowchart

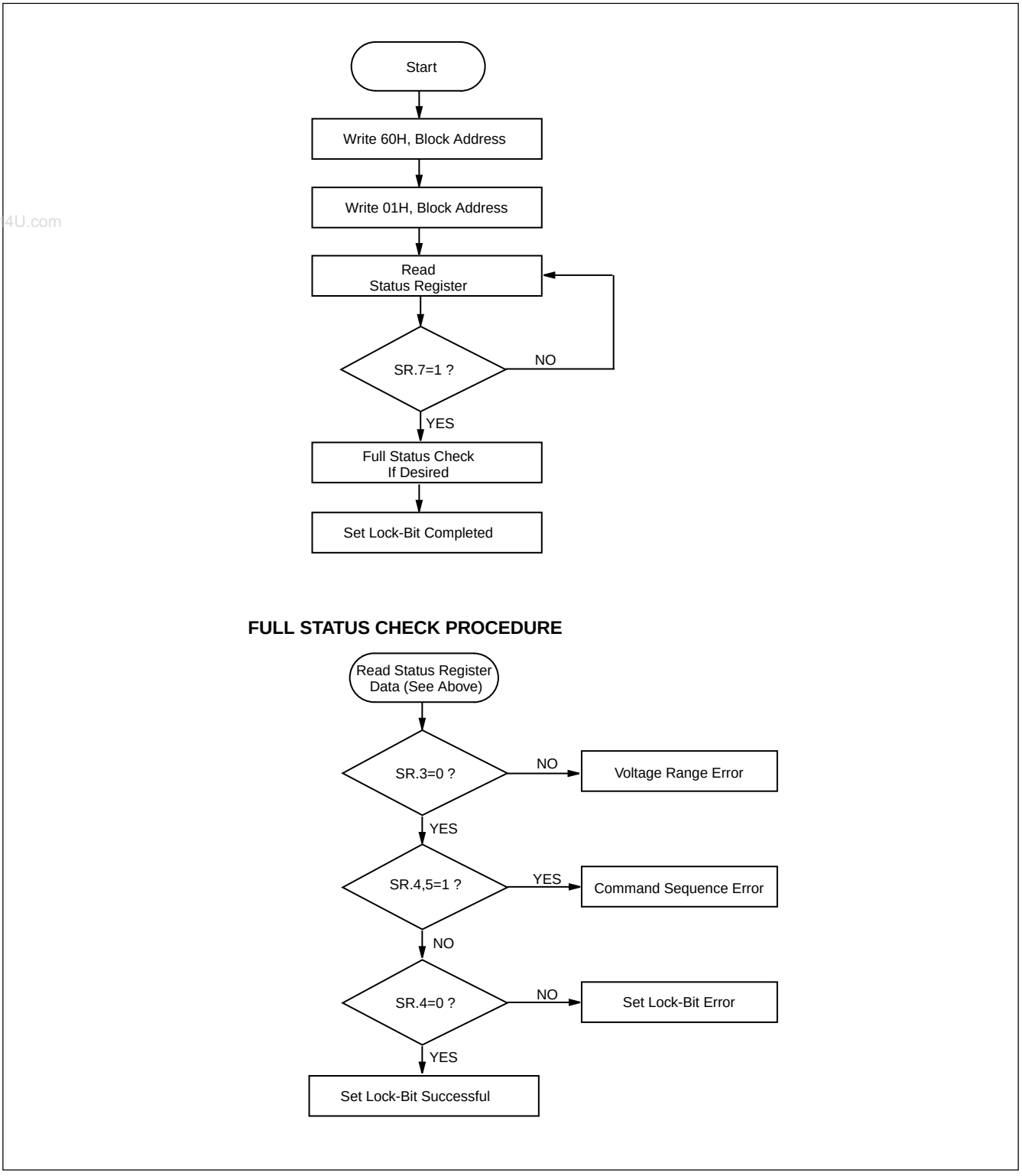
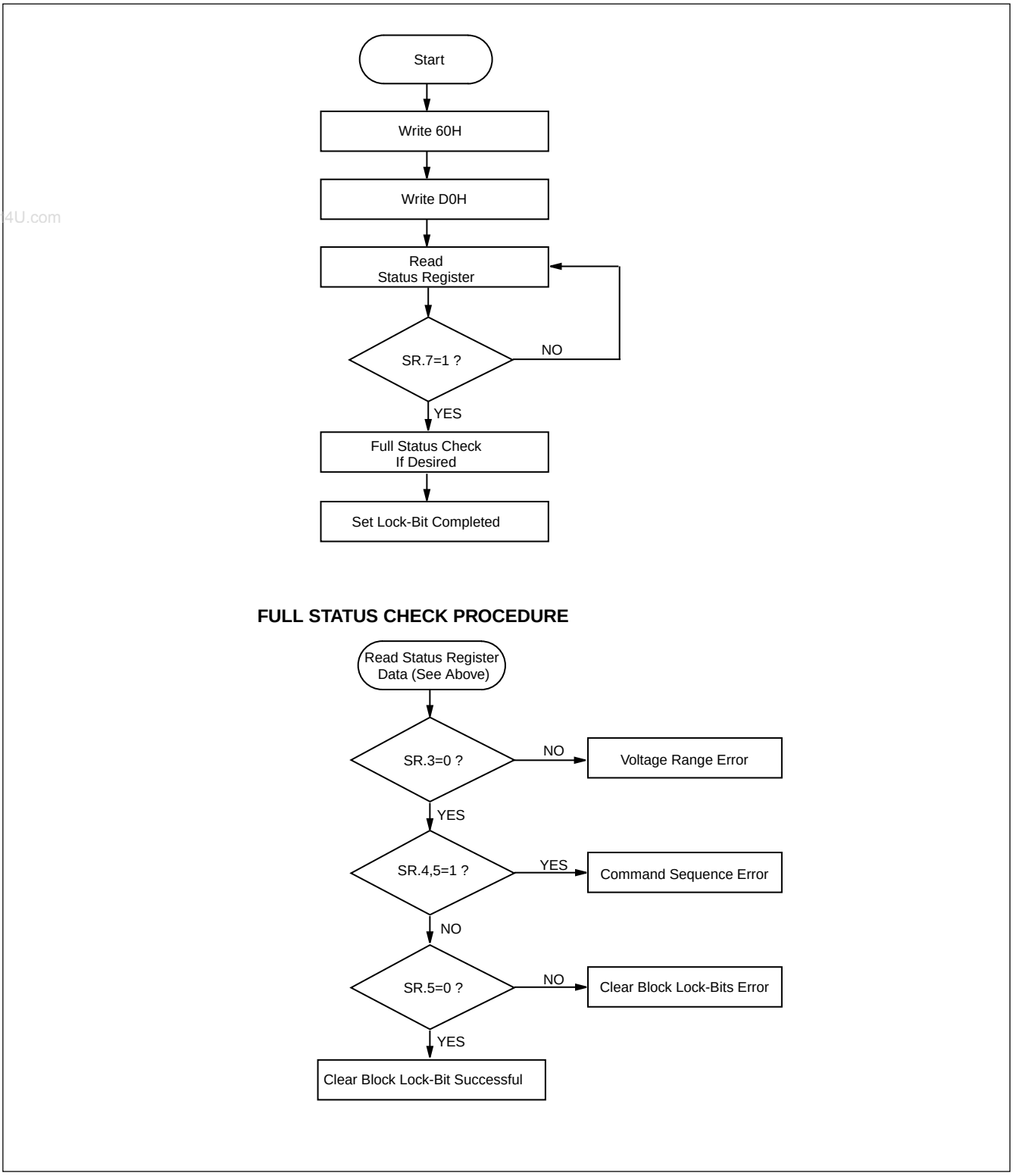


Figure 8. Clear Lock-Bit Flowchart



ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . -65°C to +150°C
Ambient Temperature
with Power Applied. . . . . -65°C to +125°C
Voltage with Respect to Ground
Voltage on any signal . . . . . -2.0 V to 5.0 V
Output Short Circuit Current (Note 2) . . . . . 100 mA

Notes:
1. Minimum DC voltage on input or I/O pins is -0.5 V and -0.2V on VCC signal. During transitions, this level may undershoot to -2.0V for periods < 20ns. Maximum DC voltage on input or I/O pins is VCC +0.5 V. During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods < 20 ns.

2. Output shorted < 1 second. No more than one output shorted at a time.

Stresses above those listed under "Absolute Maximum Rat-ings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS

Commercial (C) Devices
Ambient Temperature (T_A). . . . . 0° C to +70° C
V_{CC} Supply Voltages
V_{CC} for full voltage range. . . . . +3.0 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics

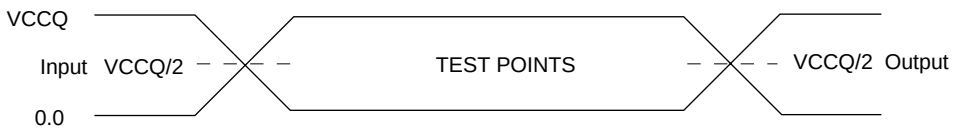
Symbol	Parameter	Notes	Typ	Max	Unit	Test Conditions
ILI	Input Leakage Current			±1	uA	VCC = VCC Max; VCCQ = VCCQ Max VIN = VCCQ or GND
ILO	Output Leakage Current			±10	uA	VCC = VCC Max; VCCQ = VCCQ Max VIN = VCCQ or GND
ICC1	VCC Standby Current	1	25	80	uA	CMOS Inputs, VCC = VCC Max, Device is disabled (see table 2)
			0.71	2	mA	TTL Inputs, VCC=VCC max, Device is disable (see table 2)
ICC3	VCC Page Mode Read Current	1	15	20	mA	CMOS Inputs, VCC=VCC Max, VCCQ=VCCQ Max Device is enabled (see Table 2) f=5MHz, IOUT=0mA
			24	29	mA	CMOS Inputs, VCC=VCC Max, VCCQ=VCCQ Max Device is enabled (see Table 2) f=33MHz, IOUT=0mA
ICC5	VCC Program or Set Lock-Bit Current	2	35	60	mA	CMOS Inputs, VPEN=VCC
			40	70	mA	TTL Inputs, VPEN=VCC
ICC6	VCC Block Erase or Clear Block Lock-Bits Current	2	35	70	mA	CMOS Inputs, VPEN=VCC
			40	80	mA	TTL Inputs, VPEN=VCC

Symbol	Parameter	Notes	Min	Max	Unit	Test Conditions
VIL	Input Low Voltage	2	-0.5	0.8	V	
VIH	Input High Voltage	2	2.0	VCCQ+0.5	V	
VOL	Output Low Voltage	2		0.4	V	VCCQ=VCCQ2/3 Min IOL=2mA
				0.2	V	VCCQ=VCCQ2/3 Min IOL=100uA
VOH	Output High Voltage	2	0.85 x VCCQ		V	VCCQ=VCCQ Min IOH=-2.5mA
			VCCQ-0.2		V	VCCQ=VCCQ Min IOH=-100uA
VLKO	VCC Lockout Voltage	3	2.2		V	

NOTES:

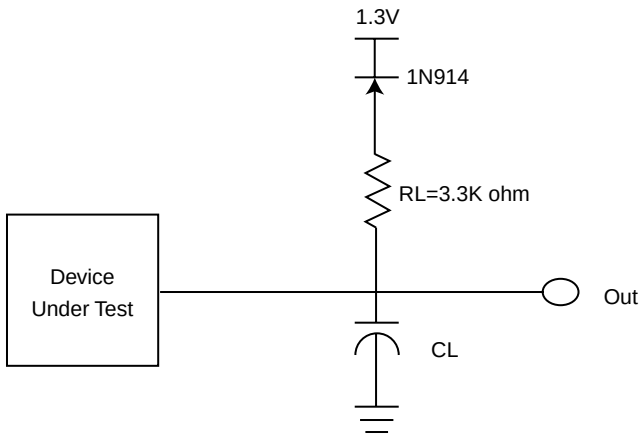
1. CMOS inputs are either VCC ±0.2 V or GND ±0.2 V. TTL inputs are either VIL or VIH .
2. Sampled, not 100% tested.
3. Block erases, programming, and lock-bit configurations are inhibited when VCC < VLKO , and not guaranteed in the range between VLKO (min) and VCC (min), and above VCC (max).

Figure 9. Transient Input/Output Reference Waveform for VCCQ=3.0V-3.6V



Note:AC test inputs are driven at VCCQ for a Logic "1" and 0.0V for a Logic "0".
Input timing being, and output timing ends, at VCCQ/2V (50% of VCCQ).
Input rise and fall times (10% tp 90%)<5ns.

Figure 10. Transient Equivalent Testing Load Circuit



NOTE: CL Includes Jig Capacitance

Test Configuration	C L (pF)
VCCQ = VCC = 3.0 V-3.6 V	30

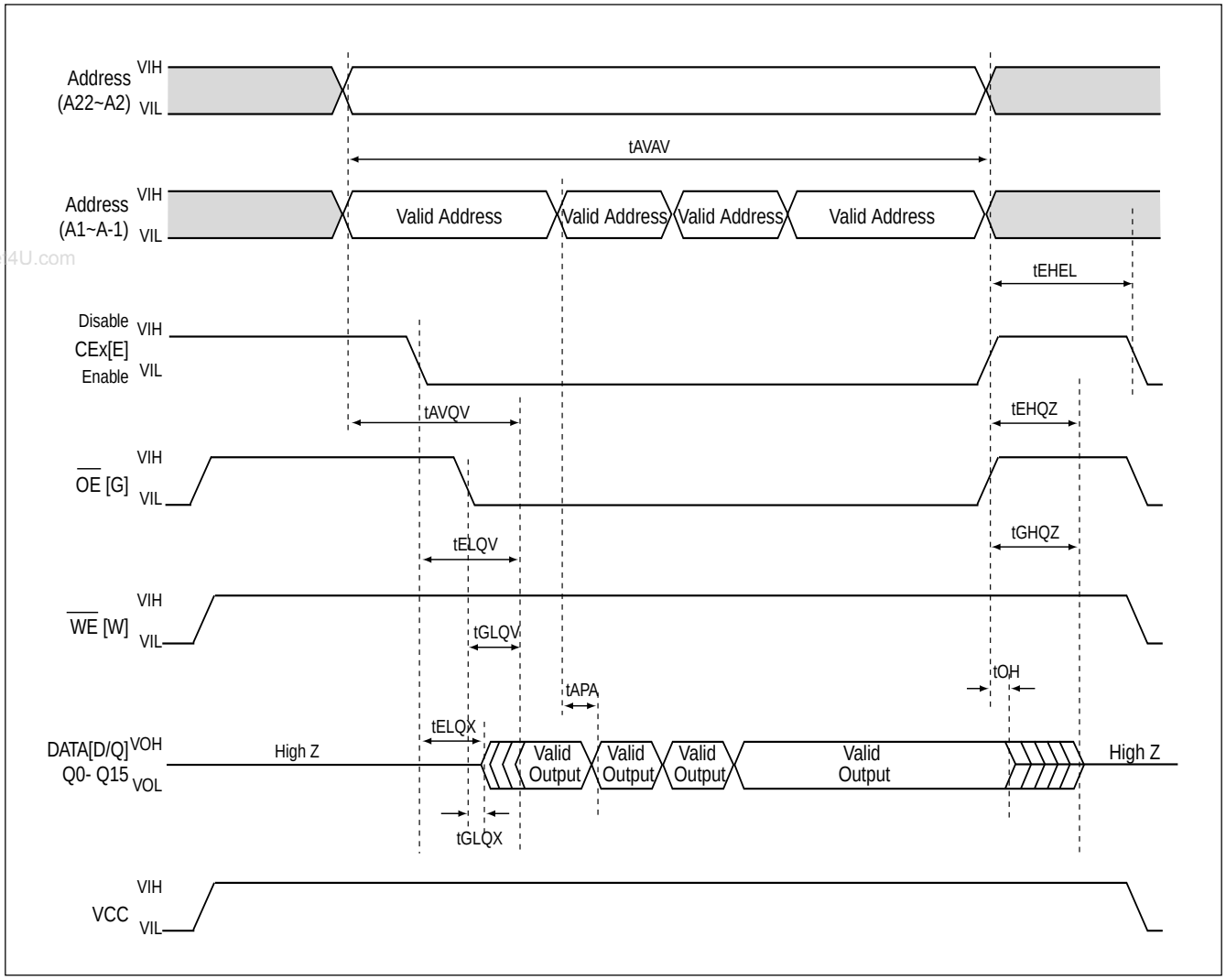
AC Characteristics --Read-Only Operations (1,2)

Versions (All units in ns unless otherwise noted)		VCC VCCQ	3.0V-3.6V(3) 3.0V-3.6V(3)	
Sym	**Parameter**	**Notes**	**Min**	**Max**
tAVAV	Read/Write Cycle Time		120	
tAVQV	Address to Output Delay			120
tELQV	CEX to Output Delay			120
tGLQV	$\overline{OE}$ to Non-Array Output Delay	2, 4		50
tELQX	CEX to Output in Low Z	5	0	
tGLQX	$\overline{OE}$ to Output in Low Z	5	0	
tEHQZ	CEX High to Output in High Z	5		35
tGHQZ	$\overline{OE}$ High to Output in High Z	5		15
tOH	Output Hold from Address, CEX, or $\overline{OE}$ Change, Whichever Occurs First	5	0	
tEHEL	CEx High to CEx Low	5	0	
tAPA	Page Address Access Time	5, 6		25
tGLQV	$\overline{OE}$ to Array Output Delay	4		25

NOTES:CEX low is defined as the first edge of $\overline{CE}$ that enables the device. CEX high is defined at the first edge of $\overline{CE}$ that disables the device (see Table 2).

1. See AC Input/Output Reference Waveforms for the maximum allowable input slew rate.
2. $\overline{OE}$ may be delayed up to t ELQV -t GLQV after the first edge of $\overline{CE}$ that enables the device (see Table 2) without impact on t ELQV .
3. See Figures 10-11, Transient Input/Output Reference Waveform for VCCQ = 3.0V - 3.6V, and Transient Equivalent Testing Load Circuit for testing characteristics.
4. When reading the MTP array a faster tGLQV (R15) applies. Non-array reads refer to status register reads, query reads, or device identifier reads.
5. Sampled, not 100% tested.
6. For devices configured to standard word/byte read mode, R14 (tAPA) will equal R1 (tAVQV).

Figure 11. AC Waveform for Both Page-Mode and Standard Word/Byte Read Operations



NOTE:

1. CE_X low is defined as the first edge of $\overline{CE}$ that enables the device. CE_X high is defined at the first edge of $\overline{CE}$ that disables the device (see Table 2).
2. For standard word/byte read operations, tAPA will equal tAVQV.
3. When reading the MTP array a faster tGLQV applies. Non-array reads refer to status register reads, query reads, or device identifier reads.

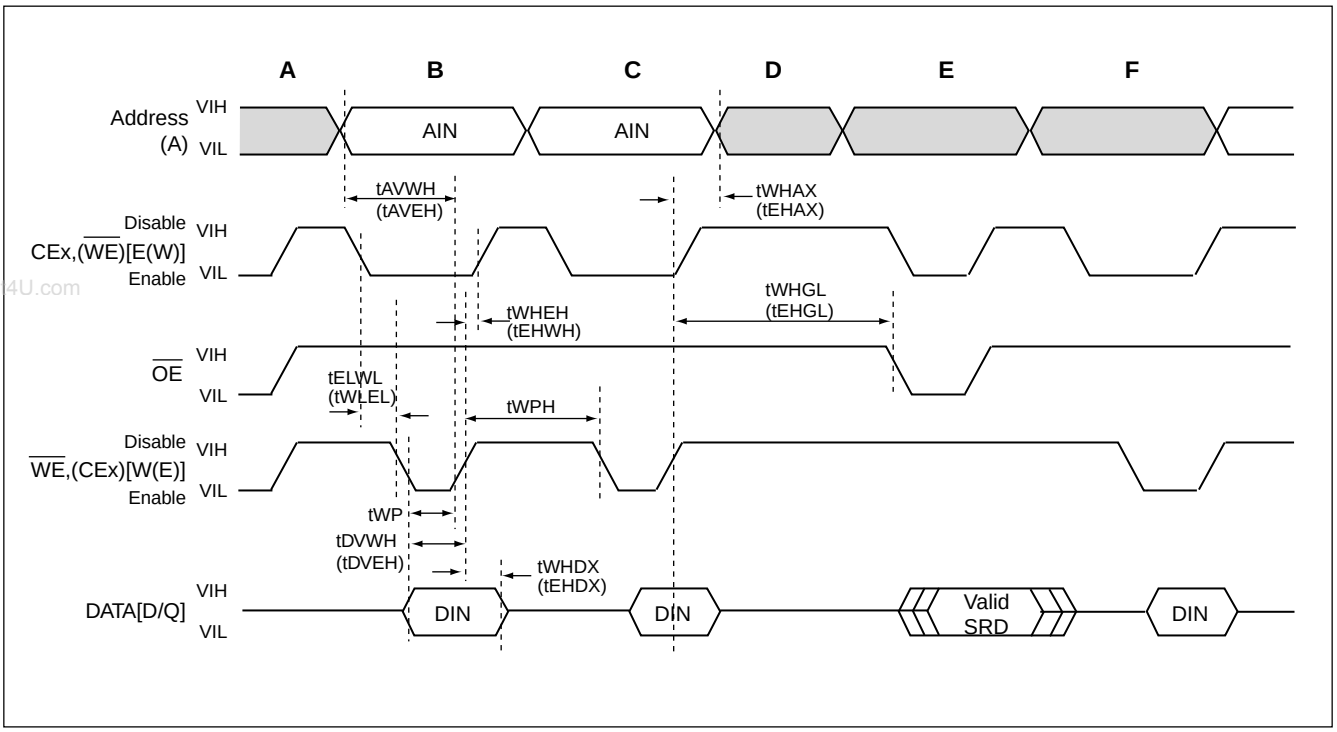
AC Characteristics--Write Operations (1,2)

Versions			Valid for All Speeds		Unit
Symbol	**Parameter**	**Notes**	**Min**	**Max**	
tELWL (tWLEL)	CEX ($\overline{WE}$) Low to $\overline{WE}$(CEX) Going Low	4	0		ns
tWP	Write Pulse Width	4	70		ns
tDVWH (tDVEH)	Data Setup to $\overline{WE}$(CEX) Going High	5	50		ns
tAVWH (tAVEH)	Address Setup to $\overline{WE}$(CEX) Going High	5	55		ns
tWHEH (tEHWH)	CEX (WE) Hold from $\overline{WE}$(CEX) High		0		ns
tWHDX (tEHDX)	Data Hold from $\overline{WE}$(CEX) High		0		ns
tWHAX (tEHAX)	Address Hold from $\overline{WE}$(CEX) High		0		ns
tWPH	Write Pulse Width High	6	30		ns
tWHGL (tEHGL)	Write Recovery before Read	7	35		ns
tWHQV5 (tEHQV5)	Set Lock-Bit Time	4	64	75/85	us
tWHQV6 (tEHQV6)	Clear Block Lock-Bits Time	4	0.5	2	sec

NOTES:
CEX low is defined as the first edge of $\overline{CE}$ that enables the device. CEX high is defined at the first edge of $\overline{CE}$ that disables the device (see Table 2).

1. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristics-Read-Only Operations.
2. A write operation can be initiated and terminated with either CE X or $\overline{WE}$.
3. Sampled, not 100% tested.
4. Write pulse width (tWP) is defined from CEX or $\overline{WE}$ going low (whichever goes low last) to CEX or $\overline{WE}$ going high (whichever goes high first). Hence, tWP = tWLWH = tELEH = tWLEH = tELWH.
5. Refer to Table 4 for valid A IN and D IN for block erase, program, or lock-bit configuration.
6. Write pulse width high (t WPH) is defined from CEX or $\overline{WE}$ going high (whichever goes high first) to CEX or $\overline{WE}$ going low (whichever goes low first). Hence, tWPH = tWHWL = tEHEL = tWHEL = tEHWL .
7. For array access, tAVQV is required in addition to tWHGL for any accesses after a write.

Figure 12. AC Waveform for Write Operations



NOTES:

1. CEX low is defined as the first edge of $\overline{CE}$ that enables the device. CEX high is defined at the first edge of $\overline{CE}$ that disables the device (see Table 1).
   a. VCC power-up and standby.
   b. Write block erase, write buffer, or program setup.
   c. Write block erase or write buffer confirm, or valid address and data.
   d. Automated erase delay.
   e. Read status register or query data.
   f. Write Read Array command.

ERASE AND PROGRAMMING PERFORMANCE(1)

PARAMETER	LIMITS			UNITS
	MIN.	TYP.(2)	MAX.	
Block Erase Time		2.0	15.0	sec
Write Buffer Byte Program Time (Time to Program 32 bytes/16 words)		218	900	us
Byte Program Time (Using Word/Byte Program Command)		210	900	us
Block Program Time (Using Write to Buffer Command)		0.8	2.4	sec
Block Erase/Program Cycles	10			Cycles

Note: 1.Not 100% Tested, Excludes external system level over head.
2.Typical values measured at 25° C,3.3V. Additionally programming typically assume checkerboard pattern.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on $\overline{OE}$	-1.0V	12.5V
Input Voltage with respect to GND on all power pins, Address pins, $\overline{CE}$ and $\overline{WE}$	-1.0V	2 VCCmax
Input Voltage with respect to GND on all I/O pins	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

CAPACITANCE TA=0° C to 70° C, VCC=3.0V~3.6V

Parameter Symbol	Parameter Description	Test Set	TYP	MAX	UNIT
CIN	Input Capacitance	VIN=0	6	7.5	pF
COUT	Output Capacitance	VOUT=0	8.5	12	pF
CIN2	Control Pin Capacitance	VIN=0	7.5	9	pF

Notes:
1. Sampled, not 100% tested.
2. Test conditions TA=25° C, f=1.0MHz

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150	10	Years
	125	20	Years

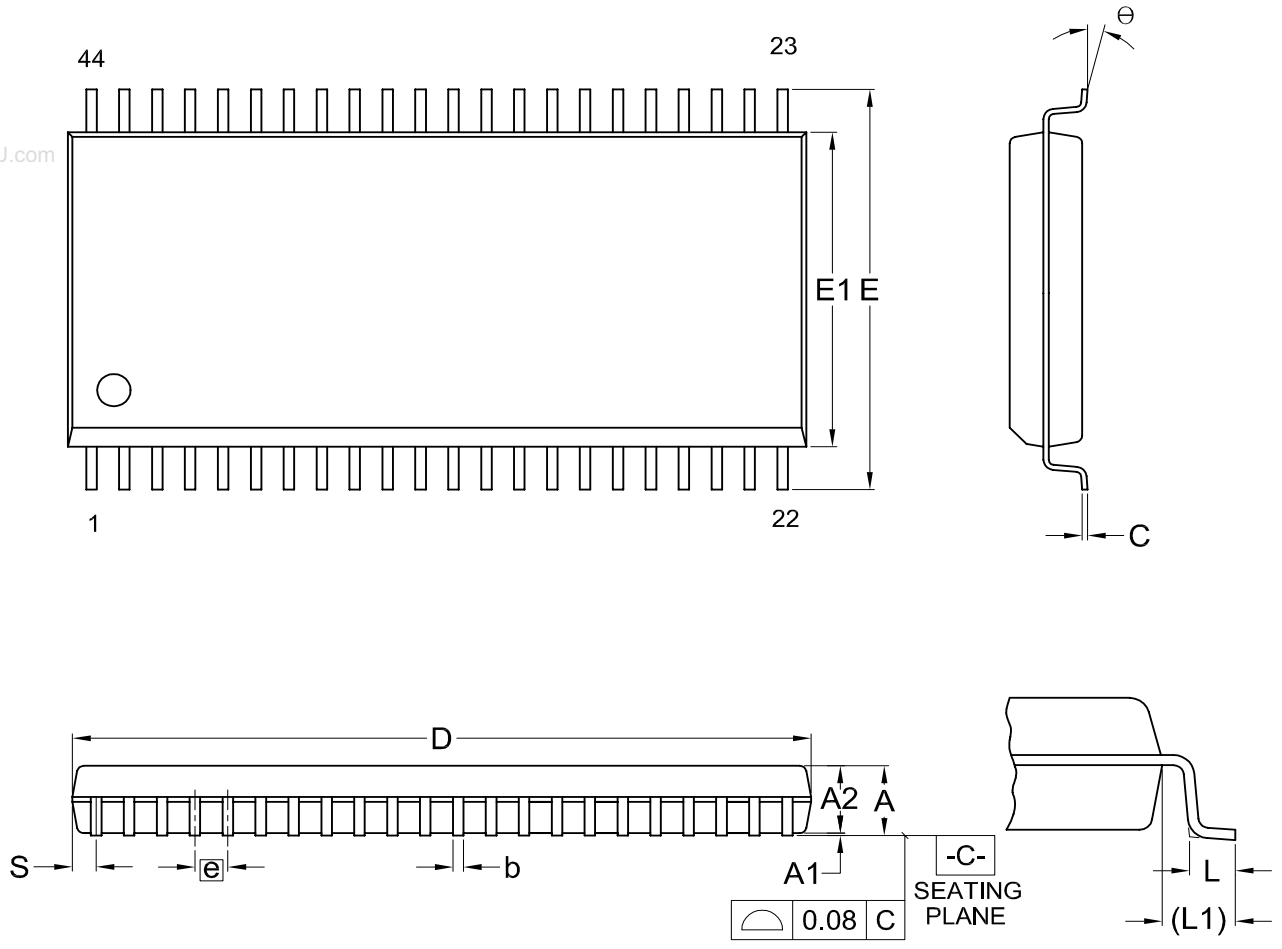
ORDERING INFORMATION

PLASTIC PACKAGE

Part NO.	Access Time (ns)	Package type
MX26L12811MC-12	120/25	44-SOP

PACKAGE INFORMATION

Title: **Package Outline for SOP 44L (500MIL)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	28.37	15.83	12.47		0.56	1.51	0.78	0
	Nom.	---	0.15	2.69	0.41	0.20	28.50	16.03	12.60	1.27	0.76	1.71	0.91	5
	Max.	3.00	0.20	2.80	0.51	0.25	28.63	16.23	12.73		0.96	1.91	1.04	10
Inch	Min.	---	0.004	0.102	0.014	0.006	1.117	0.623	0.491		0.022	0.059	0.031	0
	Nom.	---	0.006	0.106	0.016	0.008	1.122	0.631	0.496	0.050	0.030	0.067	0.036	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.127	0.639	0.501		0.038	0.075	0.041	10

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1405	6	MO-175			11-26-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Advanced Information" from title	P1	OCT/29/2003
	2. Typing error	P12	

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