



MX23L8102

8M-BIT MASK ROM

FEATURES

- Bit organization
 - 1M x 8 (byte mode)
 - 512K x 16 (word mode)
- Fast access time
 - Random access: 70ns(max.)
- Current
 - Operating: 15mA
 - Standby: 5uA
- Supply voltage
 - 2.7V ~ 3.6V
- Package
 - 48 ball mini BGA (6mm x 8mm, ball pitch 0.8mm, ball size 0.4mm)

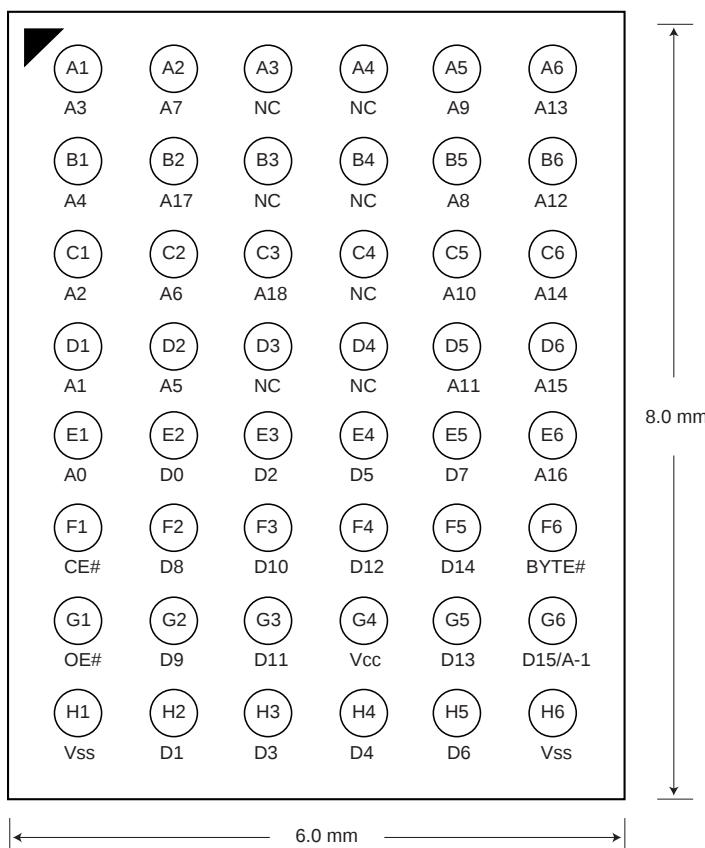
PIN DESCRIPTION

Symbol	Pin Function
A0~A18	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
CE#	Chip Enable Input
OE#	Output Enable Input
Byte#	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

PIN CONFIGURATION

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48 mini BGA (Top View, Ball Down)





MX23L8102

ORDER INFORMATION

Part No.	Speed	Package	Grade
MX23L8102XI-70	70ns	48 ball mini BGA	Industrial
MX23L8102XI-90	90ns	48 ball mini BGA	Industrial
MX23L8102XI-12	120ns	48 ball mini BGA	Industrial

Note: Industrial grade temperature: -40 ~ 85 °C
Commercial grade temperature: 0 ~ 70 °C

MODE SELECTION

CE#	OE#	Byte#	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	-40 °C to 85 °C
Storage Temperature	Tstg	-65 °C to 125 °C

DC CHARACTERISTICS (Ta = -40 °C ~ 85 °C, VCC = 2.7V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -400uA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.1V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC	-	15mA	f=5MHz, CE#=VIL, OE#=VIH all output open
Standby Current (CMOS)	ISTB	-	5uA	CE#>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25 °C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25 °C, f = 1MHZ



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AC CHARACTERISTICS (Ta = -40 °C ~ 85 °C, VCC = 2.7V~3.6V)

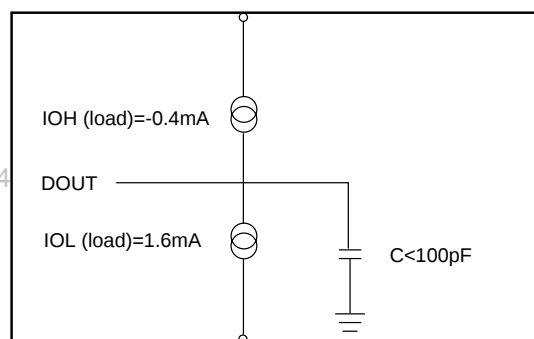
Item	Symbol	<u>23L8102-70</u>		<u>23L8102-90</u>		<u>23L8102-12</u>	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	70ns	-	90ns	-	120ns	-
Address Access Time	tAA	-	70ns	-	90ns	-	120ns
Chip Enable Access Time	tACE	-	70ns	-	90ns	-	120ns
Output Enable Time	tOE	-	30ns	-	35ns	-	50ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE# or CE# going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure

Note: 30pF output load capacitance for 70 and 90ns speed grade
100pF output load capacitance for 120ns speed grade



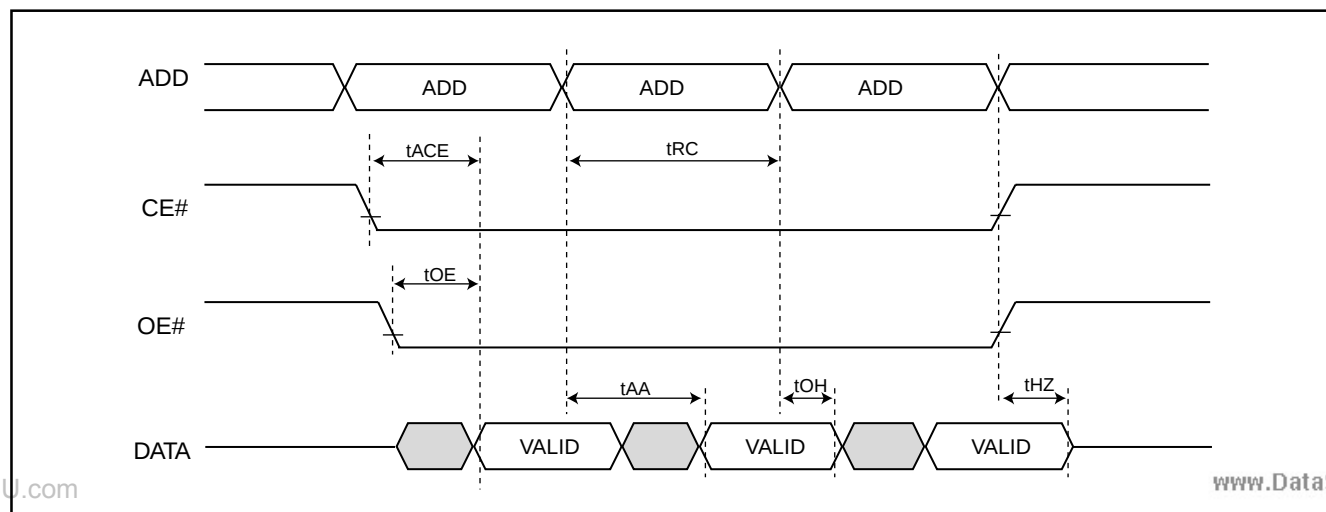
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

RANDOM READ



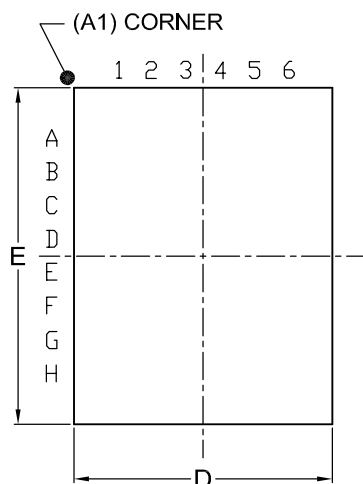


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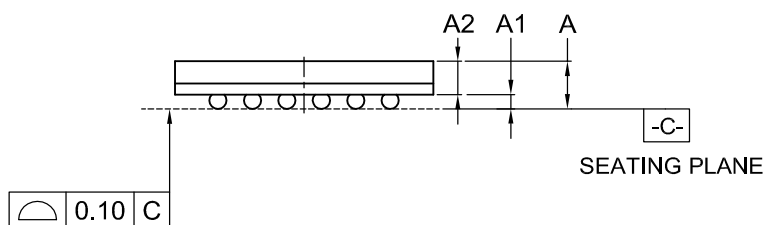
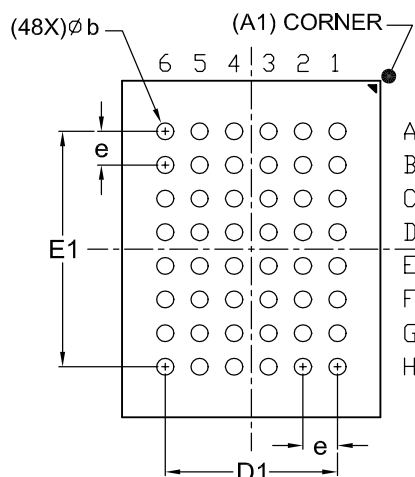
PACKAGE INFORMATION

Title: Package Outline for CSP 48BALL(6X8X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)

TOP VIEW



BOTTOM VIEW



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90		7.90		
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	5.60	0.80
	Max.	1.30	0.35	---	0.45	6.10		8.10		
Inch	Min.	---	0.010	0.026	0.014	0.232		0.311		
	Nom.	---	0.012	---	0.016	0.236	0.157	0.315	0.220	0.031
	Max.	0.051	0.014	---	0.018	0.240		0.319		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4202	3	MO-219			09-24-02

**REVISION HISTORY**

Revision No.	Description	Page	Date
1.1	Added Order Information	P2	JUL/11/2001
1.2	Correct Order Information--mis-typing	P2	AUG/20/2001
1.3	Add CE#=VIL, OE#=VIH in DC Characteristics's ICC	P2	SEP/28/2001
1.4	Modify 48-Ball BGA Package Information	P4	MAR/12/2002
1.5	Modify Package Information	P4	JUN/23/2003

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