



MX23L6413

64M-BIT FLASH COMPATIBLE MASK ROM

FEATURES

- Bit organization
 - 4M x 16 (byte mode)
- Fast access time
 - Random access:90ns(max.)
- Current
 - Operating:20mA
 - Standby:15uA
- Supply voltage
 - VCC : 2.7V~3.6V
 - VCCQ : 2.7V~3.6V
- Package
 - 48 pin TSOP (12mm x 20mm)
 - 48 ball mini BGA (8.0mm x 9.0mm, ball pitch 0.8mm, ball size 0.4mm)
- Temperature
 - -40 ~ 85℃

PIN DESCRIPTION

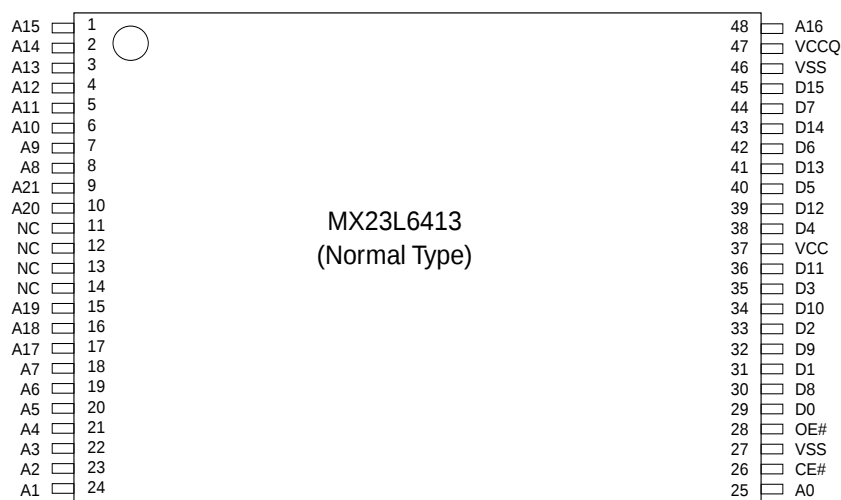
Symbol	Pin Function
A0~A20	Address Inputs
D0~D15	Data Outputs
CE#	Chip Enable Input
OE#	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
VCCQ	VCC Output Pin
NC	No Connection

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PIN CONFIGURATION

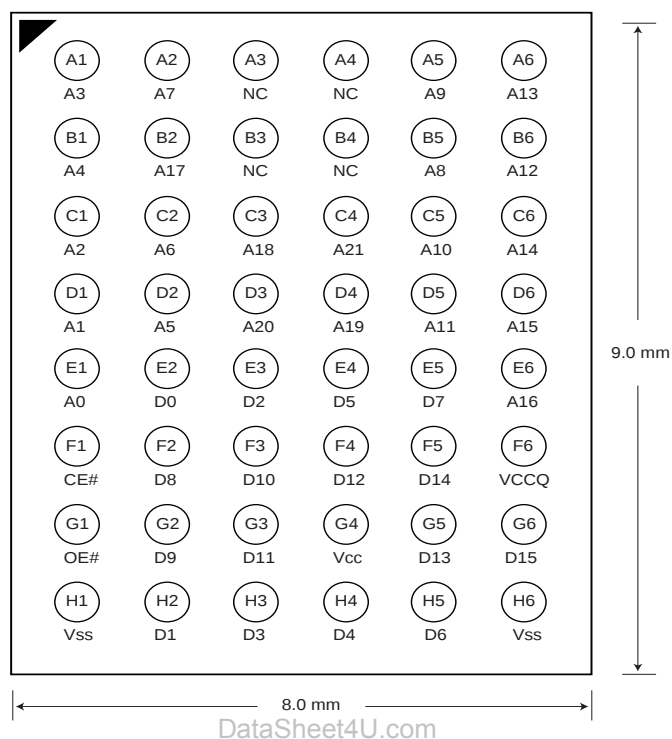
48 TSOP (Top View)





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48 mini BGA (Top View, Ball Down)



ORDER INFORMATION

Part No.	Speed	Package	Grade
MX23L6413TI-90	90ns	48 pin TSOP	Industrial
MX23L6413TI-10	100ns	48 pin TSOP	Industrial
MX23L6413TI-12	120ns	48 pin TSOP	Industrial
MX23L6413XI-90G	90ns	48 ball mini BGA (Pb free)	Industrial
MX23L6413XI-10G	100ns	48 ball mini BGA (Pb free)	Industrial
MX23L6413XI-12G	120ns	48 ball mini BGA (Pb free)	Industrial

MODE SELECTION

CE#	OE#	D0~D15	Power
H	X	High Z	Stand-by
L	H	High Z	Active
L	L	D0~D15	Active



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ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	-40 °C to 85 °C
Storage Temperature	Tstg	-65 °C to 125 °C

DC CHARACTERISTICS (Ta = -40 °C ~ 85 °C, VCC = 2.7V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.3V	-	IOH = -400uA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.1V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC	-	40mA	f=5MHz, all output open
Standby Current (CMOS)	ISTB	-	15uA	CE#>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25 °C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25 °C, f = 1MHZ

AC CHARACTERISTICS (Ta = -40 °C ~ 85 °C, VCC = 2.7V~3.6V)

Item	Symbol	<u>23L6413-90</u>		<u>23L6413-10</u>		<u>23L6413-12</u>	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	90ns	-	100ns	-	120ns	-
Address Access Time	tAA	-	90ns	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	90ns	-	100ns	-	120ns
Output Enable Time	tOE	-	25ns	-	30ns	-	50ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE# or CE# going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.



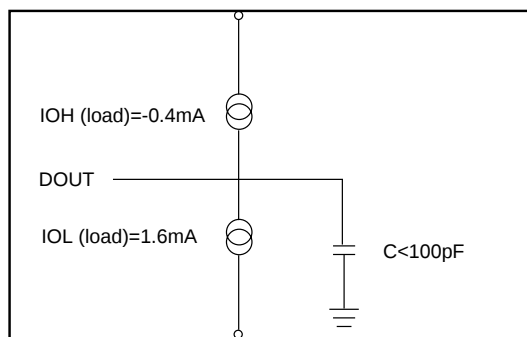
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AC Test Conditions

Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure

Note:

30pF output load capacitance for 80ns speed grade
100pF output load capacitance for 100ns and 120ns speed grade



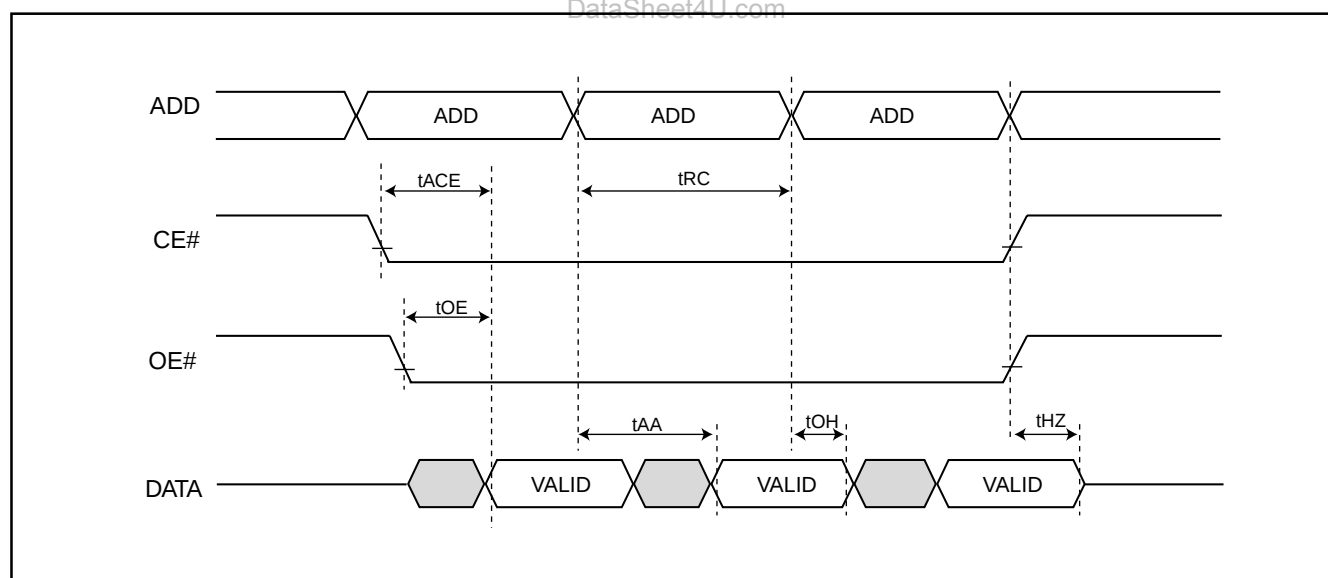
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

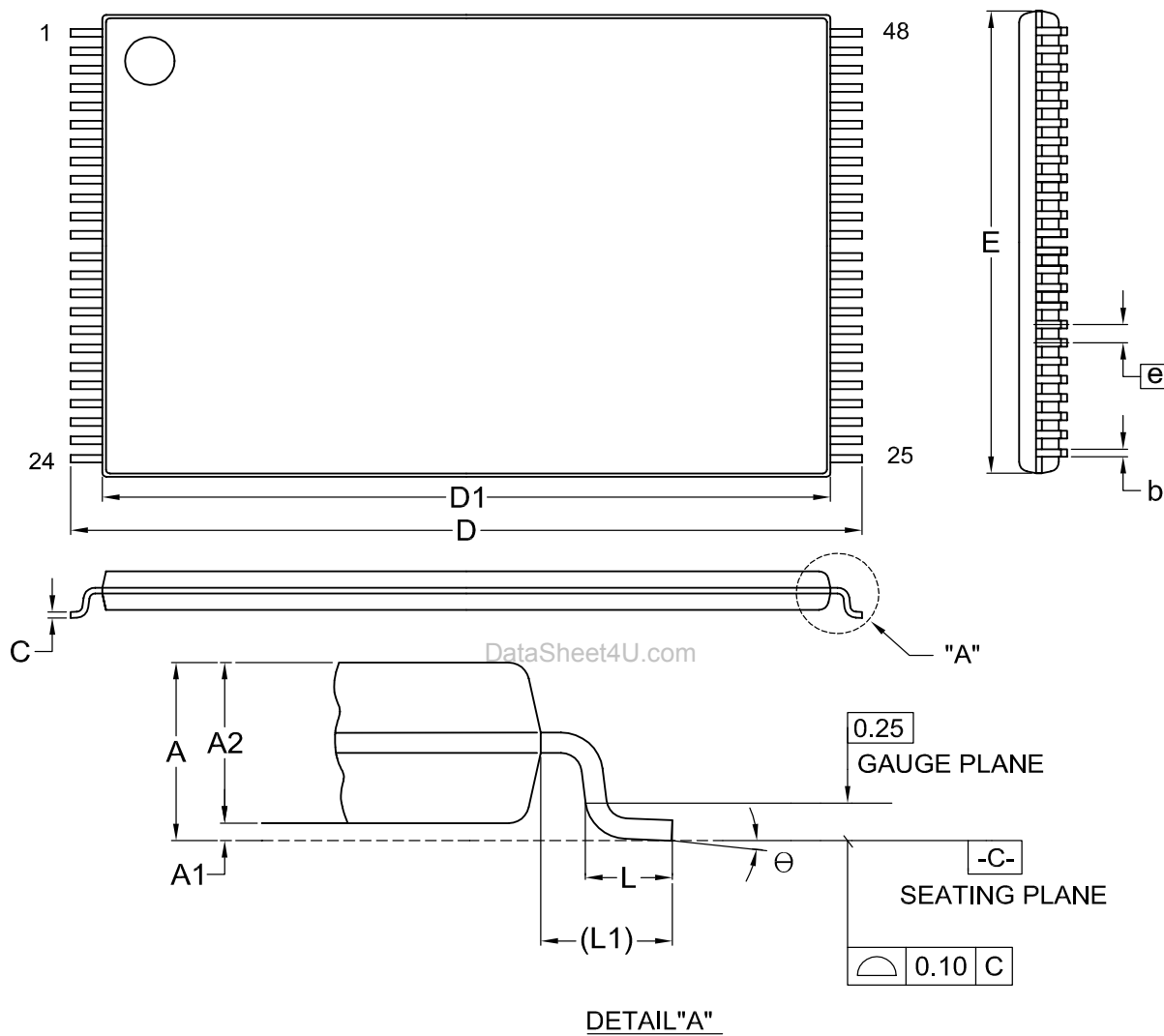
RANDOM READ





PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476		0.028	0.035	8

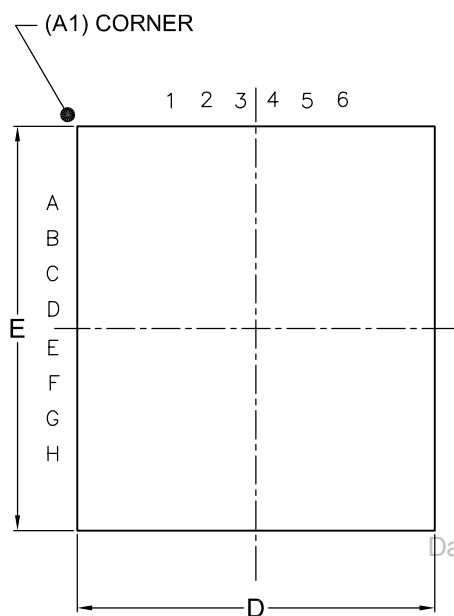
DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	6	MO-142			09-24-02



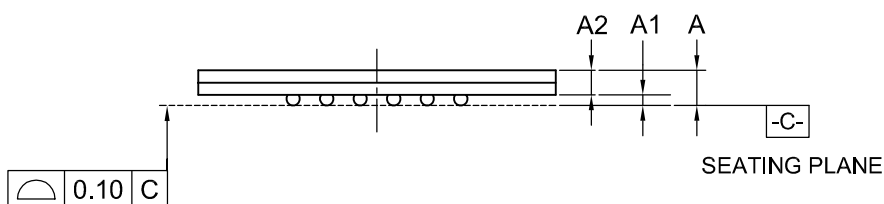
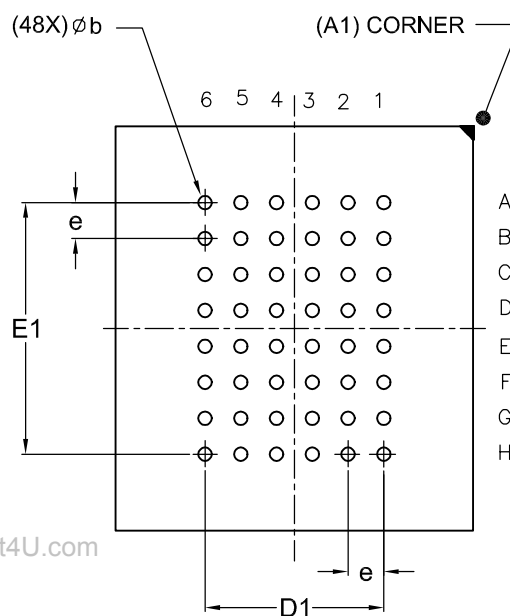
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Title: Package Outline for CSP 48BALL(8X9X1.3MM,BALL PITCH 0.8MM,BALL DIAMETER 0.4MM)

TOP VIEW



BOTTOM VIEW



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	D	D1	E	E1	e
UNIT										
mm	Min.	---	0.25	0.65	0.35	7.90		8.90		
	Nom.	---	0.30	---	0.40	8.00	4.00	9.00	5.60	0.80
	Max.	1.30	0.35	---	0.45	8.10		9.10		
Inch	Min.	---	0.010	0.026	0.014	0.311		0.350		
	Nom.	---	0.012	---	0.016	0.315	0.157	0.354	0.220	0.031
	Max.	0.051	0.014	---	0.018	0.319		0.358		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-4212	3	MO-219			09-24-02



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REVISION HISTORY

Revision No.	Description	Page	Date
1.1	1. Package information update	P5~6	NOV/08/2002

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