



MX23L4100

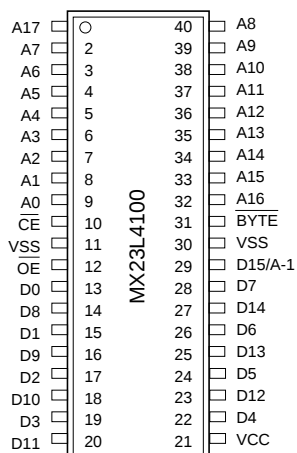
4M-BIT MASK ROM (8/16 BIT OUTPUT)

FEATURES

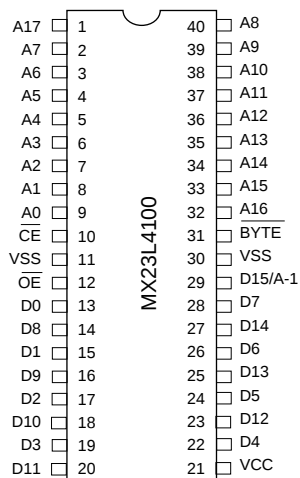
- Bit organization
 - 512K x 8 (byte mode)
 - 256K x 16 (word mode)
- Fast access time
 - Random access: 100ns
- Current
 - Operating: 30mA
 - Standby: 20uA
- Supply voltage
 - 3.3V±10%
- Package
 - 40 pin SOP (500 mil)
 - 40 pin PDIP (600 mil)

PIN CONFIGURATION

40 SOP



40 PDIP



ORDER INFORMATION

Part No.	Access Time	Package
MX23L4100MC-10	100ns	40 pin SOP
MX23L4100MC-12	120ns	40 pin SOP
MX23L4100MC-15	150ns	40 pin SOP
MX23L4100PC-10	100ns	40 pin PDIP
MX23L4100PC-12	120ns	40 pin PDIP
MX23L4100PC-15	150ns	40 pin PDIP

PIN DESCRIPTION

Symbol	Pin Function
A0~A17	Address Inputs
D0~D14	Data Outputs
CE	Chip Enable Input
OE	Output Enable Input
Byte	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

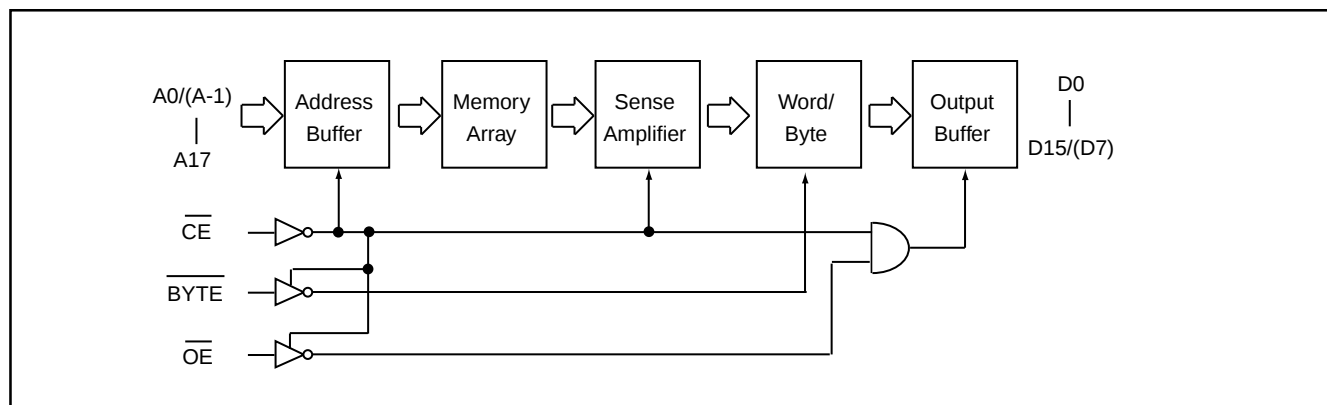
MODE SELECTION

CE	OE	Byte	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active



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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.8V to VCC+2.0V (Note)
Ambient Operating Temperature	T _{opr}	0°C to 70°C
Storage Temperature	T _{stg}	-65°C to 125°C

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Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -0.8V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (T_a = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	I _{OH} = -0.4mA
Output Low Voltage	VOL	-	0.4V	I _{OL} = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current (CE toggle)	ICC1	-	30mA	t _{RC} =100ns, all output open
Standby Current (TTL)	ISTB1	-	1mA	CE = VIH
Standby Current (CMOS)	ISTB2	-	20uA	CE > VCC - 0.2V
Input Capacitance	CIN	-	10pF	T _a = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	T _a = 25°C, f = 1MHZ



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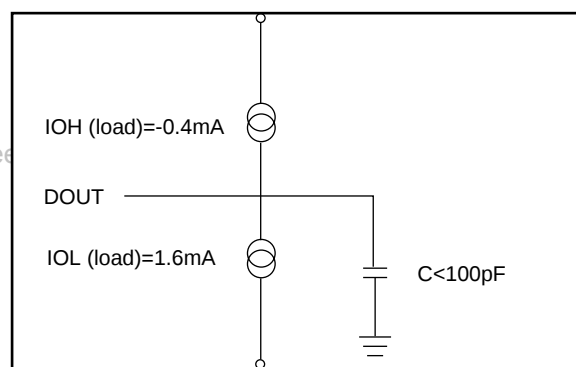
AC CHARACTERISTICS (Ta = 0 °C ~ 70 °C, VCC = 3.3V±10%)

Item	Symbol	23L4100-10		23L4100-12		23L4100-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	-	0ns	-	0ns	-	0ns
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



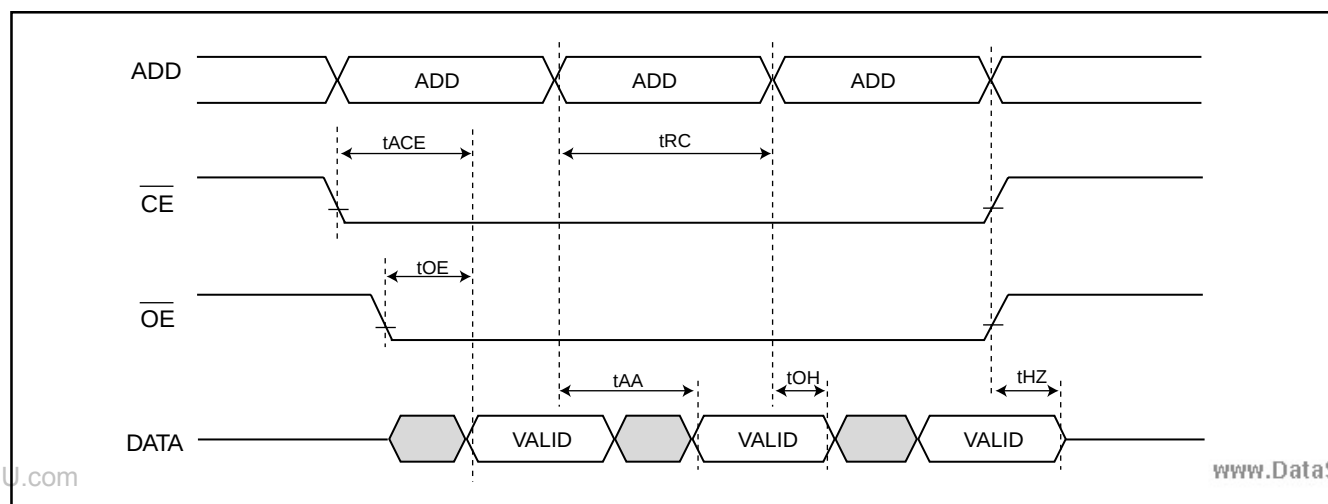
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

ACCESS TIMING

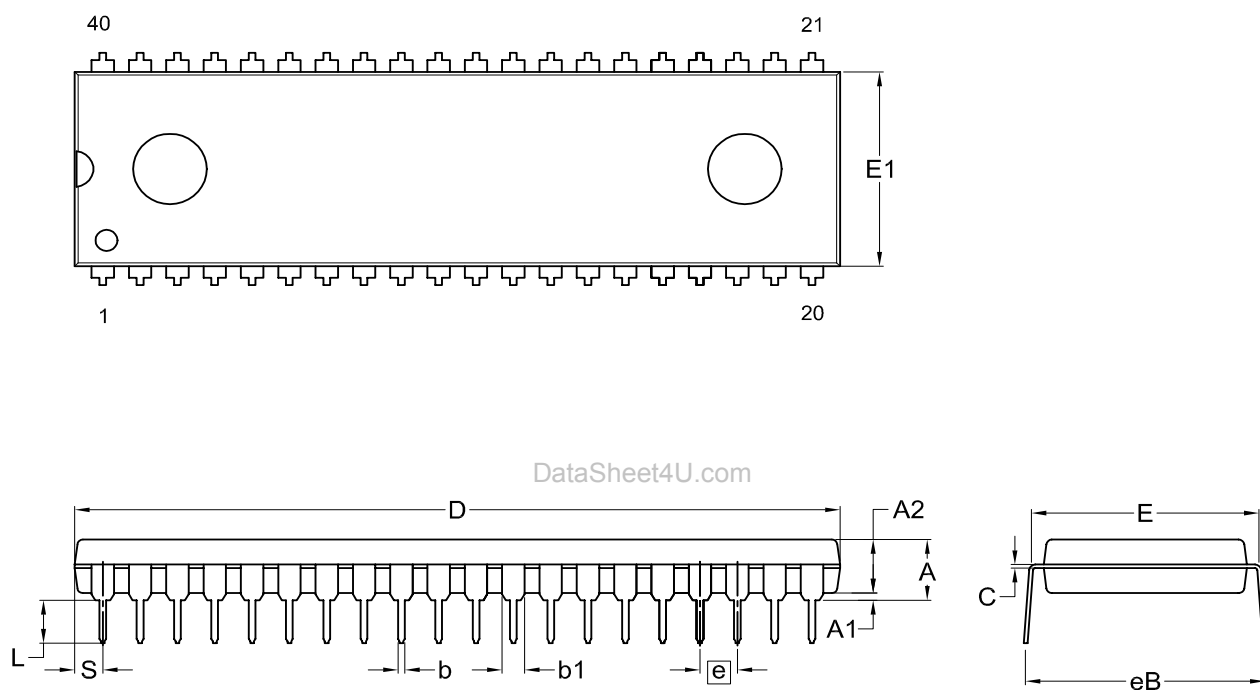




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PACKAGE INFORMATION

Title: Package Outline for PDIP 40L(600MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

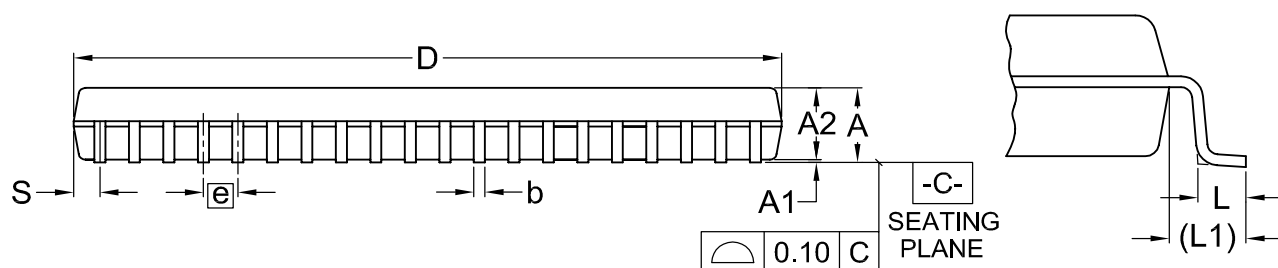
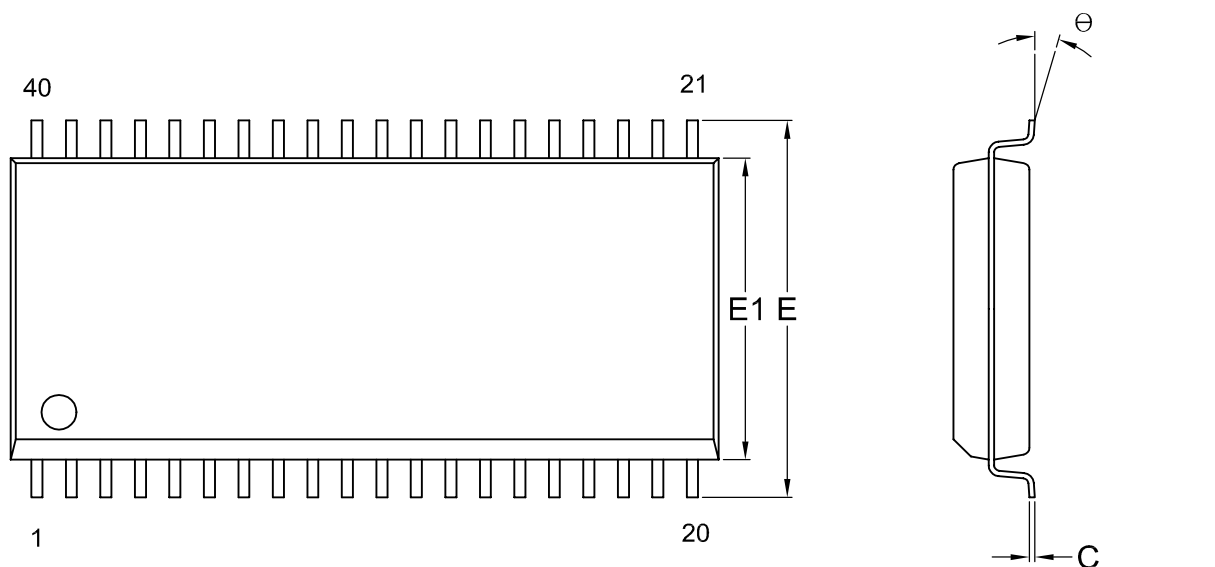
SYMBOL		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
UNIT														
mm	Min.	---	0.25	3.73	0.38	1.14	0.20	51.31	15.11	13.84		15.75	2.92	1.65
	Nom.	---	---	3.94	0.46	1.27	0.25	51.94	15.24	13.97	2.54	16.51	3.30	1.90
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	52.57	15.37	14.10		17.27	3.68	2.16
Inch	Min.	---	0.010	0.147	0.015	0.045	0.008	2.020	0.595	0.545		0.620	0.115	0.065
	Nom.	---	---	0.155	0.018	0.050	0.010	2.045	0.600	0.550	0.100	0.650	0.130	0.075
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	2.070	0.605	0.555		0.680	0.145	0.085

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.4	7				01-20-03



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Title: Package Outline for SOP 40L (450MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.10	2.59	0.36	0.15	25.93	13.92	11.17		0.56	1.20	0.84	0
	Nom.	---	0.15	2.69	0.41	0.20	26.06	14.12	11.30	1.27	0.76	1.40	0.97	5
	Max.	3.00	0.20	2.80	0.51	0.25	26.19	14.32	11.43		0.96	1.60	1.10	8
Inch	Min.	---	0.004	0.102	0.014	0.006	1.021	0.548	0.440		0.022	0.047	0.033	0
	Nom.	---	0.006	0.106	0.016	0.008	1.026	0.556	0.445	0.050	0.030	0.055	0.038	5
	Max.	0.118	0.008	0.110	0.020	0.010	1.031	0.564	0.450		0.038	0.063	0.043	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1404.1	3	MO-099			09-24-'02



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REVISION HISTORY

REVISION	DESCRIPTION	PAGE	DATE
1.3	AC CHARACTERISTICS tOH 10ns-->0ns	P3	FEB/01/1999
1.4	Modify Package Information	P4~5	JUL/16/2001
1.5	Modify Package Information	P4~5	NOV/22/2002
1.6	Modify 40-PDIP Package Information	P4	JUN/19/2003

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