32M-BIT Low Voltage, Serial Mask ROM Memory with 50MHz SPI Bus Interface

FEATURES

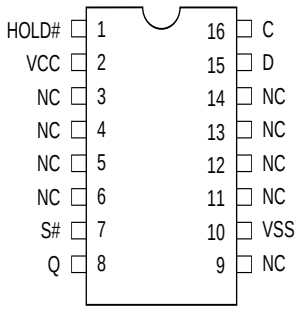
- 32Mbit of Mask ROM
- 2.7 to 3.6V Single Supply Voltage
- SPI Bus Compatible Serial Interface
- 50MHz Clock Rate (maximum)

DESCRIPTION

The MX23L3254 is a 32Mbit (4M x 8) Serial Mask ROM accessed by a high speed SPI-compatible bus.

PIN CONFIGURATIONS

16-PIN SOP (300 mil)



Note:
1. NC=No Connection
2. See page 16 (onwards) for package dimensions, and how to identify pin-1.

PIN DESCRIPTION

SYMBOL	DESCRIPTION
C	Serial Clock
D	Serial Data Input
Q	Serial Data Output
S#	Chip Select
HOLD#	Hold
VCC	Supply Voltage
VSS	Ground

ORDER INFORMATION

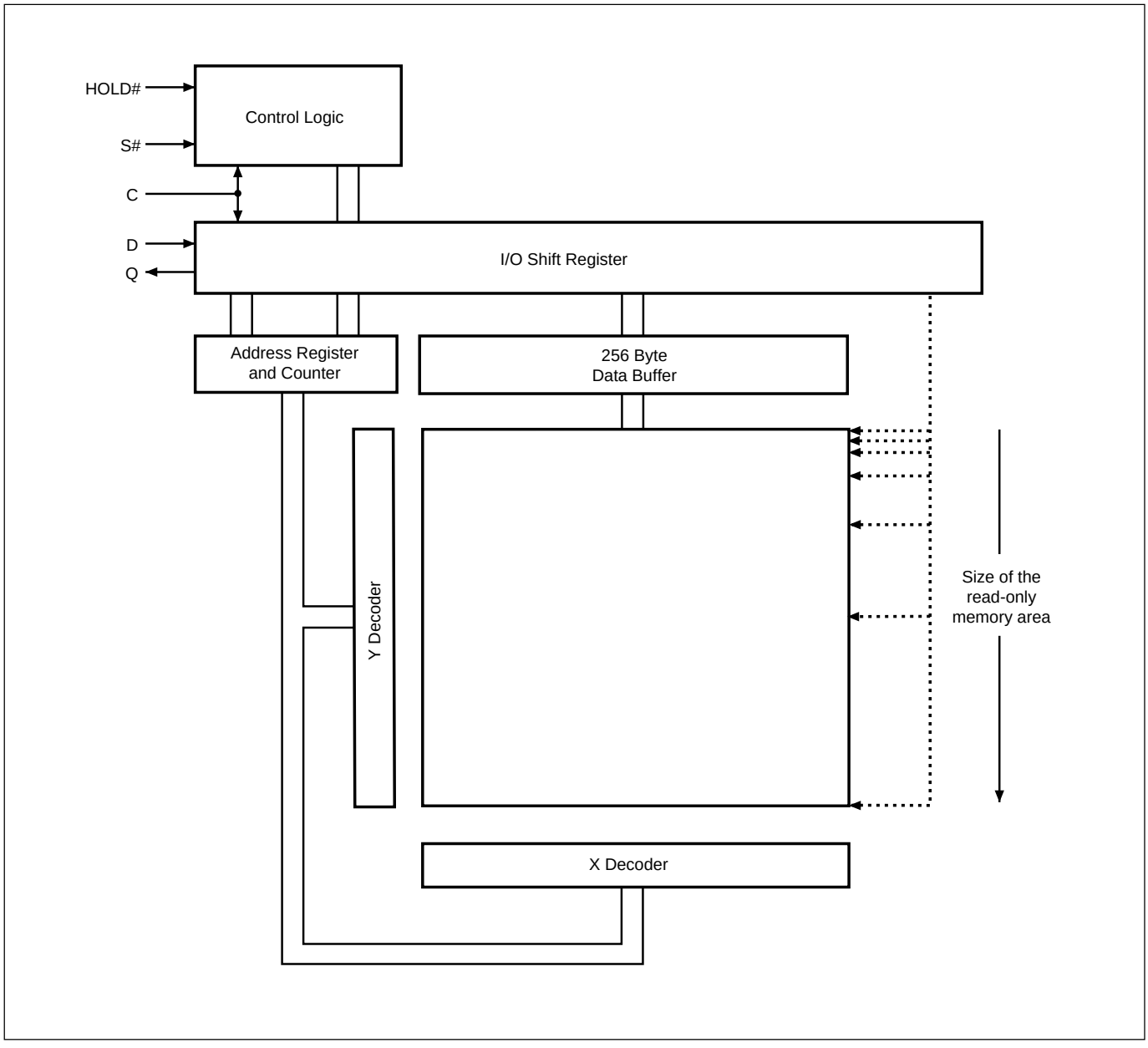
Part No.	Speed	Package	Remark
MX23L3254MC-20	20ns	16-SOP	
MX23L3254MC-20G	20ns	16-SOP	Pb-free
MX23L3254MI-20G	20ns	16-SOP	Pb-free (Industrial Grade)

Note:
* Industrial grade operating temperature: -25 ~ 85 °C
Commercial grade operating temperature: 0 ~ 70 °C

MEMORY ORGANIZATION

The memory is organized as:
- 4M bytes (8 bits each)

BLOCK DIAGRAM



SIGNAL DESCRIPTION

Serial Data Output (Q). This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

Serial Data Input (D). This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).

Serial Clock (C). This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

Chip Select (S#). When this input signal is High, the device is deselected. Driving Chip Select (S#) Low enables the device, placing it in the active power mode.

After Power-up, a falling edge on Chip Select (S#) is required prior to the start of any instruction.

Hold (HOLD#). The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select (S#) driven Low.

SPI MODES

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

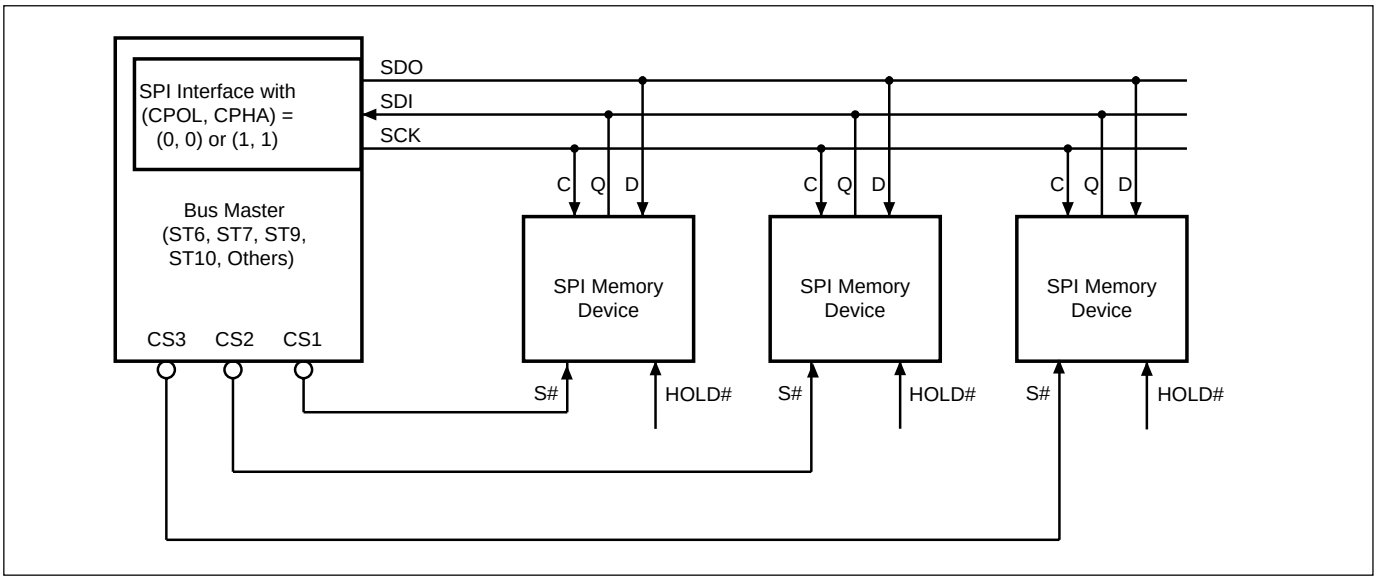
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in Figure 2, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

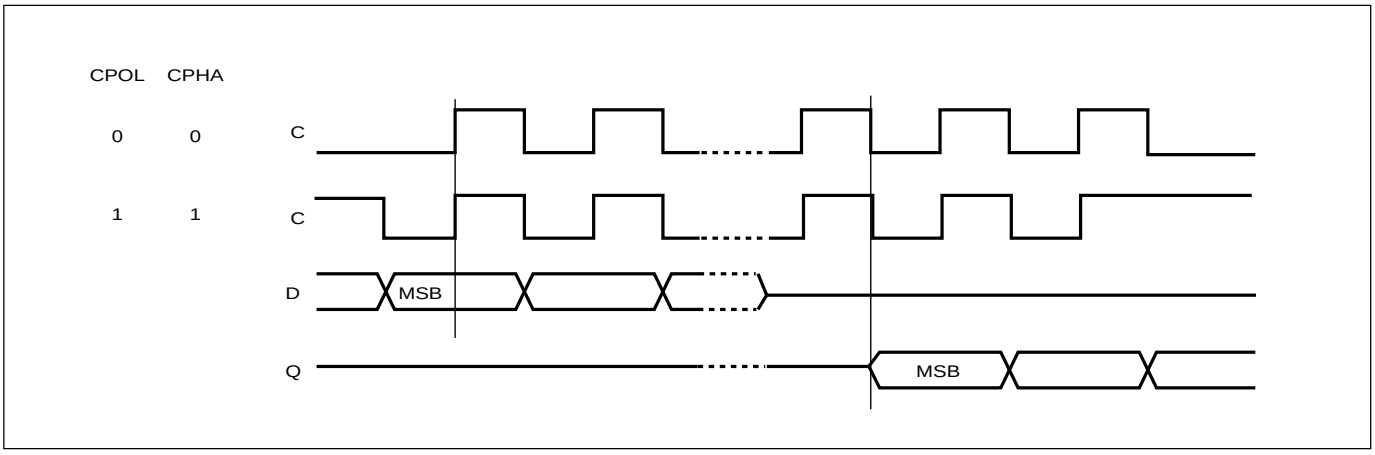
- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 1. Bus Master and Memory Devices on the SPI Bus



Note: 1. Hold (HOLD#) signals should be driven, High or Low as appropriate.

Figure 2. SPI Modes Supported



OPERATING FEATURES

Active Power, Stand-by Power

When Chip Select (S#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (S#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed. The device then goes in to the Stand-by Power mode. The device consumption drops to ICC1 .

Protection Modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the MX23L3254 boasts the following data protection mechanisms:

- Power-On Reset and an internal timer (tPUW) can provide protection against inadvertant changes while the power supply is outside the operating specification.

Hold Condition

The Hold (HOLD#) signal is used to pause any serial communications with the device without resetting the clocking sequence.

To enter the Hold condition, the device must be selected, with Chip Select (S#) Low.

The Hold condition starts on the falling edge of the Hold (HOLD) signal, provided that this coincides with Serial Clock (C) being Low (as shown in Figure 3).

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with Serial Clock (C) being Low.

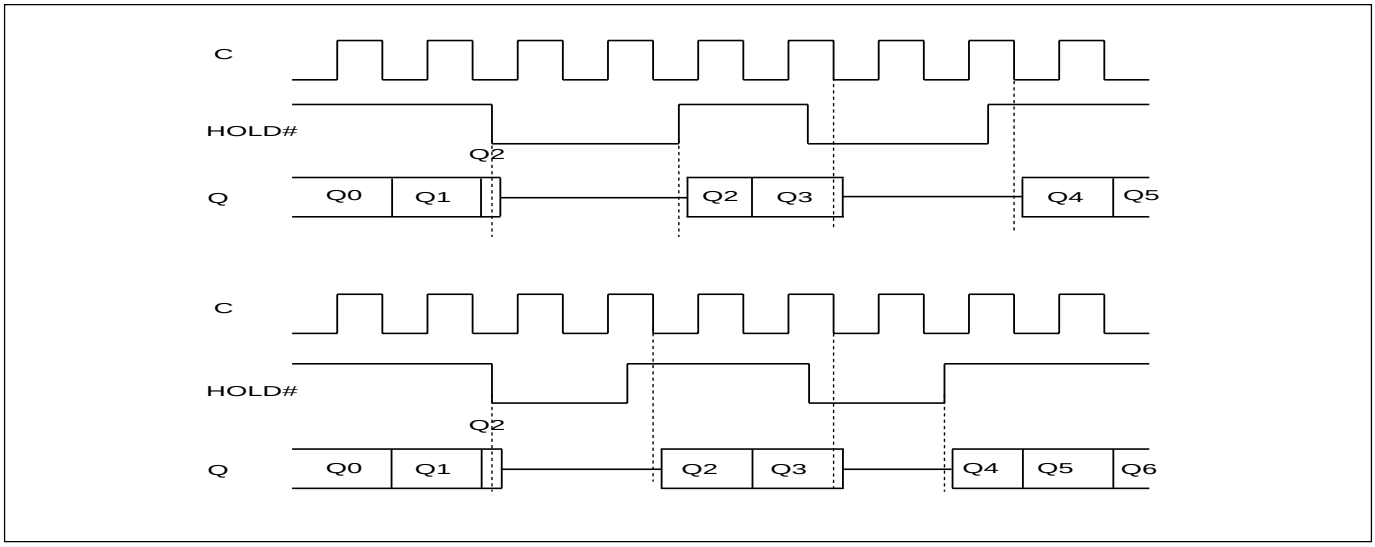
If the falling edge does not coincide with Serial Clock (C) being Low, the Hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the Hold condition ends after Serial Clock (C) next goes Low. (This is shown in Figure 2).

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

Normally, the device is kept selected, with Chip Select (S#) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (S#) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD#) High, and then to drive Chip Select (S#) Low. This prevents the device from going back to the Hold condition.

Figure 3. Hold Condition Activation (for data output only)



INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (D) is sampled on the first rising edge of Serial Clock (C) after Chip Select (S#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (D), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in Table 1.

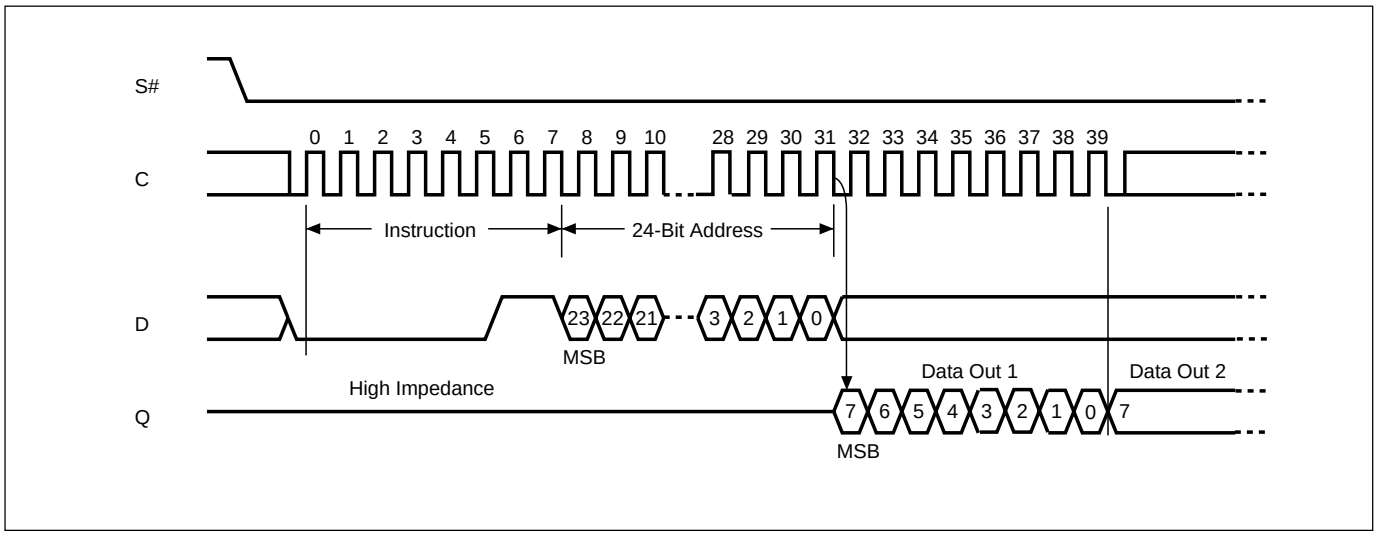
Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (S#) can be driven High after any bit of the data-out sequence is being shifted out.

Table 1. Instruction Set

Instruction	Description	One-byte Instruction Code		Address Bytes	Dummy Bytes	Data Bytes
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0Bh	3	1	1 to ∞

Figure 4. Read Data Bytes (READ) Instruction Sequence and Data-Out Sequence



Note: 1. Address bits A23,A22 is Don't Care.

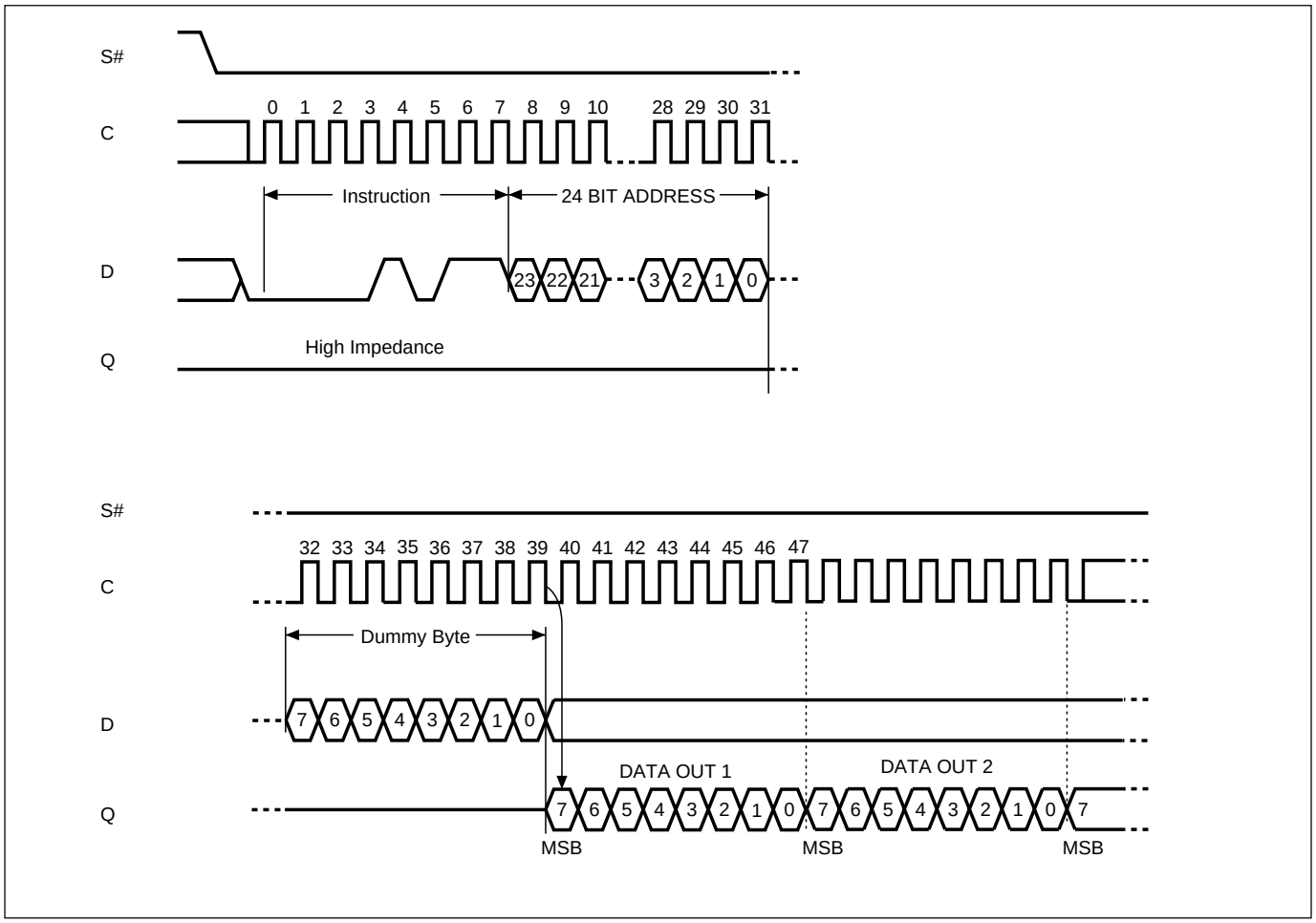
Read Data Bytes (READ)

The device is first selected by driving Chip Select (S#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency fR, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 4. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction.When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (S#) High. Chip Select (S#) can be driven High at any time during data output.

Figure 5. Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence and Data-Out Sequence



Read Data Bytes at Higher Speed (FAST_READ)

The device is first selected by driving Chip Select (S#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (Q), each bit being shifted out, at a maximum frequency fC, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 5. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (S#) High. Chip Select (S#) can be driven High at any time during data output.

POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must not be selected (that is Chip Select (S#) must follow the voltage applied on VCC) until VCC reaches the correct value:

- VCC(min) at Power-up, and then for a further delay of tVSL
- VSS at Power-down

Usually a simple pull-up resistor on Chip Select (S#) can be used to insure safe and proper Power-up and Power-down.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while VCC is less than the POR threshold value, VWI -- all operations are disabled, and the device does not respond to any instruction.

These values are specified in Table 2.

If the delay, tVSL, has elapsed, after VCC has risen above VCC (min), the device can be selected for READ instructions even if the tPUW delay is not yet fully elapsed.

At Power-up, the device is in the following state:
- The device is in the Standby mode.

Normal precautions must be taken for supply rail decoupling, to stablise the VCC feed. Each device in a system should have the VCC rail decoupled by a suitable capacitor close to the package pins.

(Generally, this capacitor is of the order of 0.1uF).

At Power-down, when VCC drops from the operating voltage, to below the POR threshold value, VWI , all operations are disabled and the device does not respond to any instruction.

Figure 6. Power-up Timing

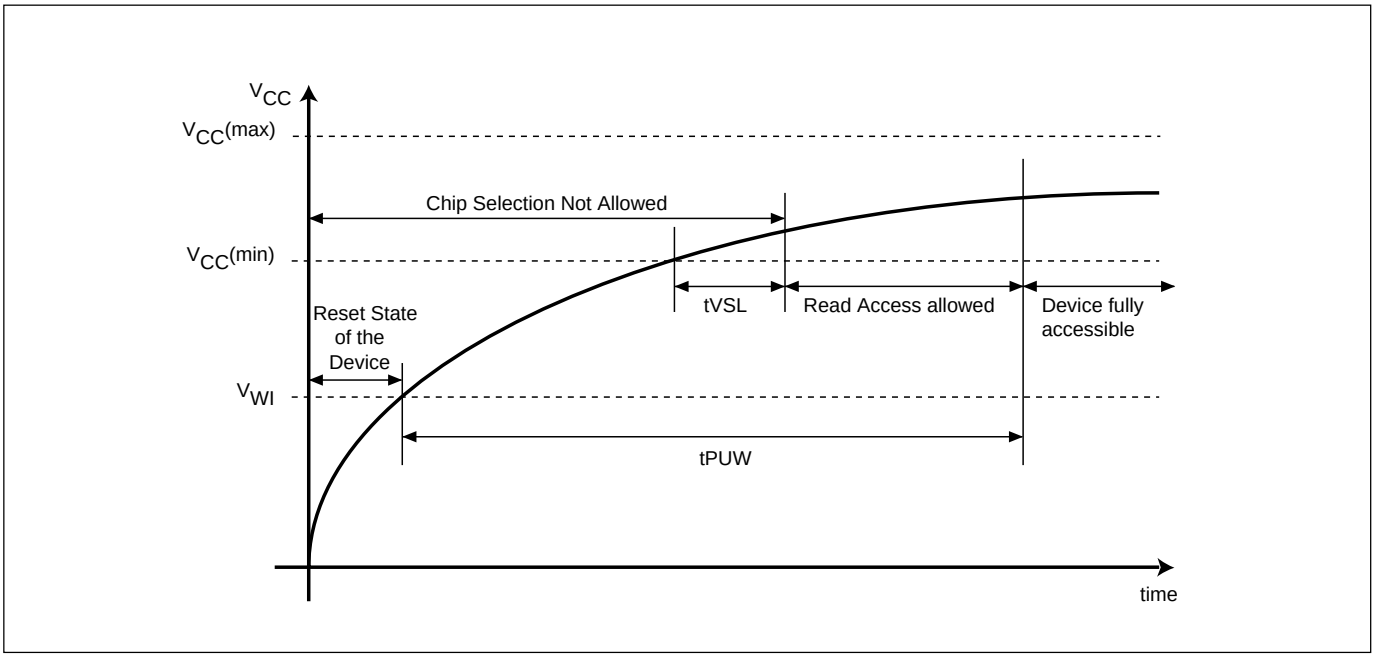


Table 2. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}[1]	V_{CC}(min) to S# low	30		us

Note: 1. These parameters are characterized only.

MAXIMUM RATING

Stressing the device above the rating listed in the"Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage Temperature	- 65	150	˚C
T_{LEAD}	Lead Temperature during Soldering [1]		260 [2]	˚C
V_{IO}	Input and Output Voltage (with respect to Ground)	- 0.6	4.0	V
V_{CC}	Supply Voltage	- 0.6	4.0	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [3]	- 2000	2000	V

Note: 1. Compliant with the ECOPACK® 7191395 specifiication for lead-free soldering processes
2. Not exceeding 250˚C for more than 30 seconds, and peaking at 260˚C
3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

DC AND AC PARAMETERS

This section summarizes the operating and mea-surement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 4. Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
T_A	Ambient Operating Temperature	-25	85	˚C

Table 5. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input Timing Reference Voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output Timing Reference Voltages	V_{CC} / 2		V

Note: 1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 7. AC Measurement I/O Waveform

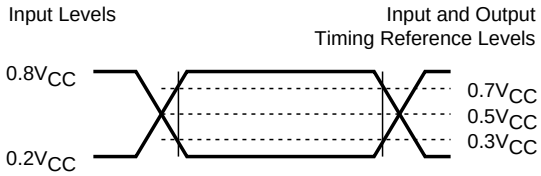


Table 6. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (Q)	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance (other pins)	V_{IN} = 0V		6	pF

Note: Sampled only, not 100% tested, at T_A=25˚C and a frequency of 20 MHz.

Table 7. DC Characteristics

Symbol	Parameter	Test Condition (in addition to those in Table 8)	Min.	Max.	Unit
I_{LI}	Input Leakage Current			± 2	uA
I_{LO}	Output Leakage Current			± 2	uA
I_{CC1}	Standby Current	S# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	uA
I_{CC2}	Operating Current (READ)	C = 0.1V_{CC} / 0.9.V_{CC} at 50MHz, Q = open		8	mA
		C = 0.1V_{CC} / 0.9.V_{CC} at 20MHz, Q = open		4	mA
V_{IL}	Input Low Voltage		- 0.5	0.3V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 uA	V_{CC}- 0.2		V

Table 8. AC Characteristics

Test conditions specified in Table 4 and Table 5						
Symbol	**Alt.**	**Parameter**	**Min.**	**Typ.**	**Max.**	**Unit**
f_C	f_C	Clock Frequency for the following instructions: FAST_READ	D.C.		50	MHz
f_R		Clock Frequency for READ instructions	D.C.		20	MHz
t_{CH} [1]	t_{CLH}	Clock High Time	9			ns
t_{CL} [1]	t_{CLL}	Clock Low Time	9			ns
t_{CLCH} [2]		Clock Rise Time[3] (peak to peak)	0.1			V/ns
t_{CHCL} [2]		Clock Fall Time[3] (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	S# Active Setup Time (relative to C)	5			ns
t_{CHSL}		S# Not Active Hold Time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{CHSH}		S# Active Hold Time (relative to C)	5			ns
t_{SHCH}		S# Not Active Setup Time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	S# Deselect Time	100			ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time			8	ns
t_{CLQV}	t_V	Clock Low to Output Valid			8	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{HLCH}		HOLD# Setup Time (relative to C)	5			ns
t_{CHHH}		HOLD# Hold Time (relative to C)	5			ns
t_{HHCH}		HOLD Setup Time (relative to C)	5			ns
t_{CHHL}		HOLD Hold Time (relative to C)	5			ns
t_{HHQX} [2]	t_{LZ}	HOLD to Output Low-Z			8	ns
t_{HLQZ} [2]	t_{HZ}	HOLD# to Output High-Z			8	ns

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/f_C$
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.

Figure 8. Serial Input Timing

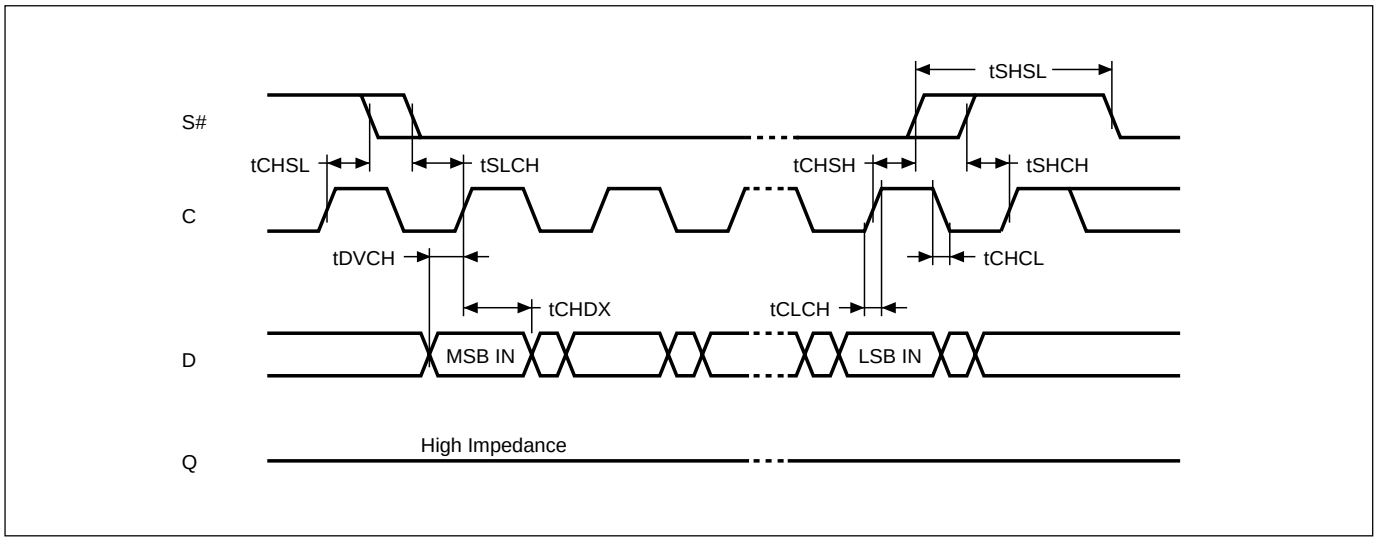


Figure 9. Hold Timing

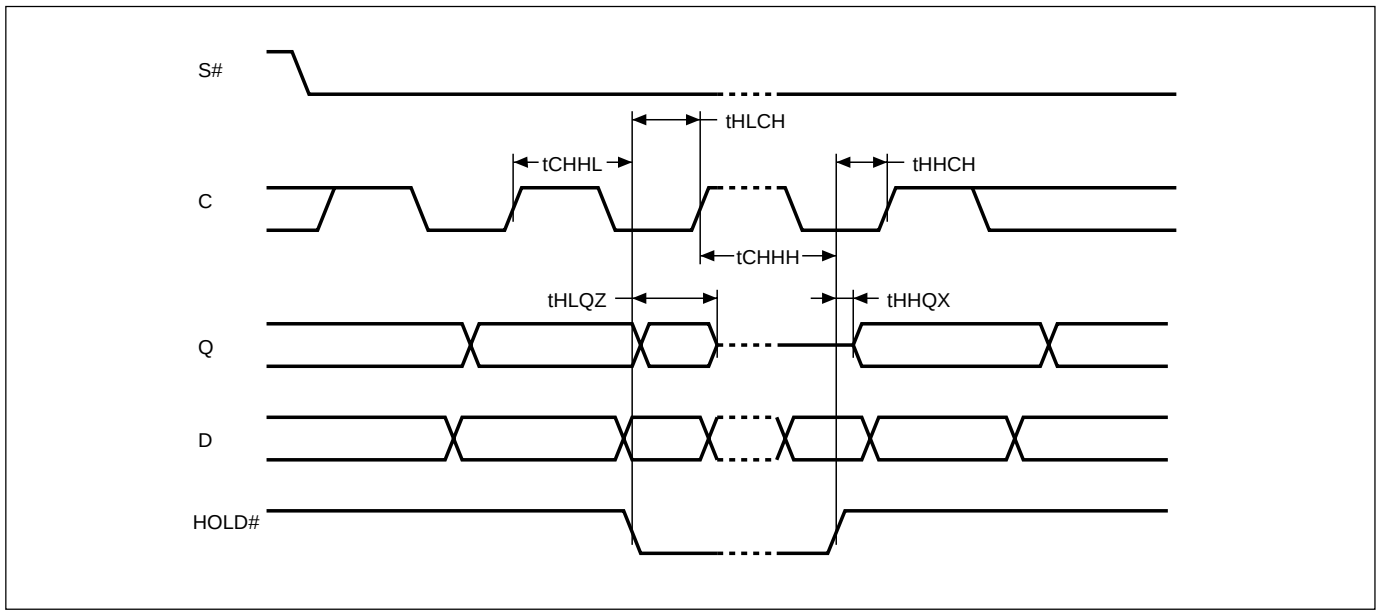
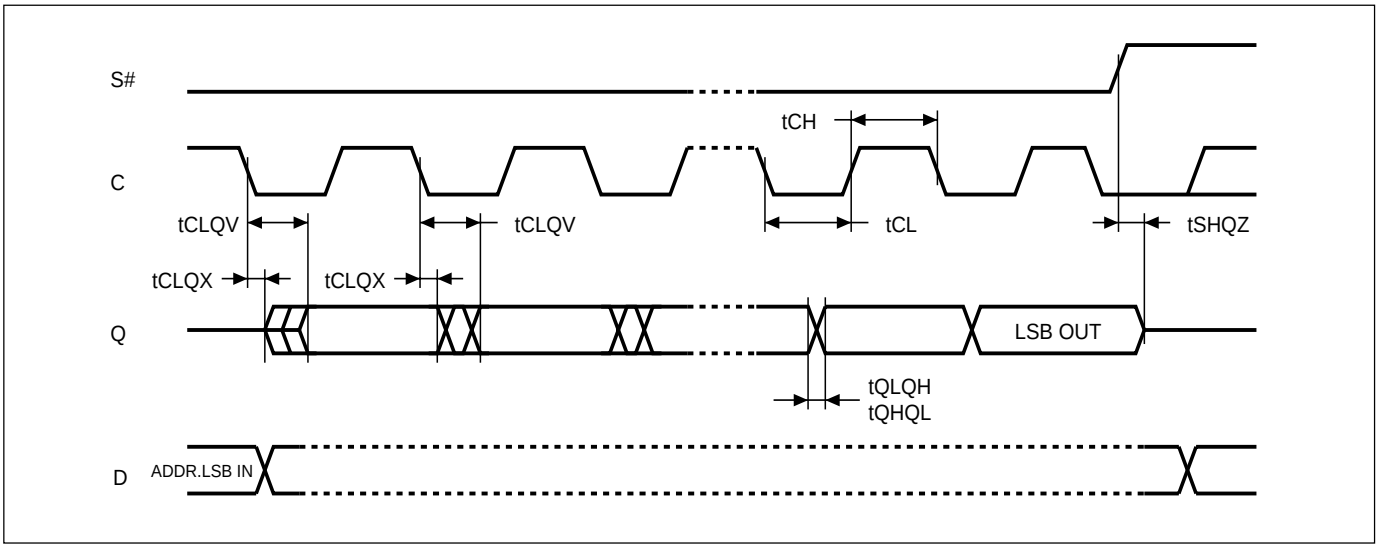
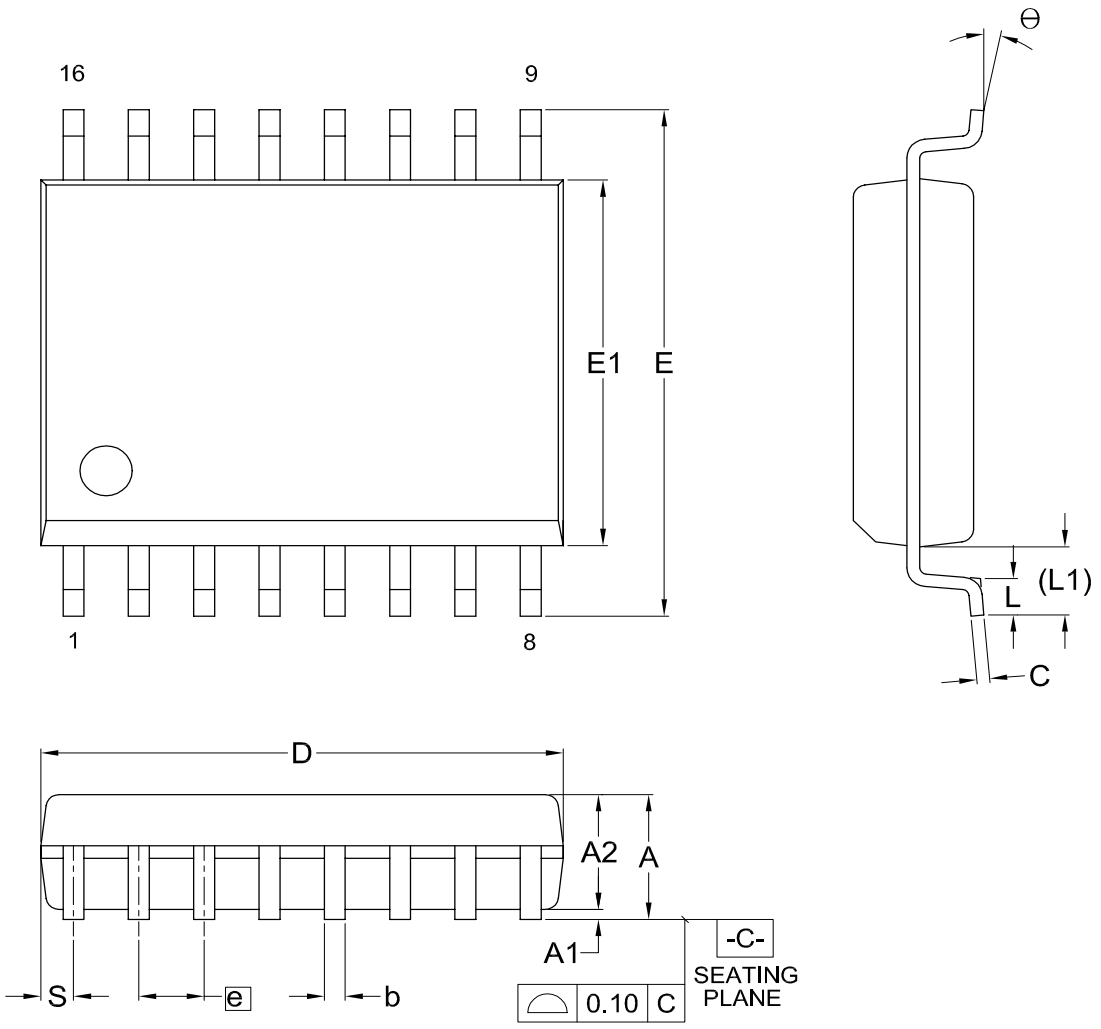


Figure 10. Output Timing



PACKAGE INFORMATION

Title: Package Outline for SOP 16L (300MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.25	0.36	0.20	10.08	10.19	7.42		0.40	1.31	0.51	0
	Nom.	---	0.20	2.31	0.41	0.25	10.16	10.31	7.52	1.27	0.84	1.44	0.64	5
	Max.	2.65	0.30	2.40	0.51	0.30	10.24	10.44	7.60		1.27	1.57	0.77	8
Inch	Min.	---	0.004	0.089	0.014	0.008	0.397	0.401	0.292		0.016	0.052	0.020	0
	Nom.	---	0.008	0.091	0.016	0.010	0.400	0.406	0.296	0.050	0.033	0.057	0.025	5
	Max.	0.104	0.012	0.094	0.020	0.012	0.403	0.411	0.299		0.050	0.062	0.030	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1402	7	MS-013			06-28-'04

REVISION HISTORY

Revision	Description	Page	Date
1.0	1. Removed "Preliminary" on page 1	P1	MAR/02/2005
1.1	1. Added "Industrial Grade"	P1,11	MAR/09/2005
1.2	1. Output timing waveform description modified	P15	JUN/08/2005

MACRONIX INTERNATIONAL CO., LTD.

Headquarters:
TEL:+886-3-578-6688
FAX:+886-3-563-2888

Europe Office :
TEL:+32-2-456-8020
FAX:+32-2-456-8021

Hong Kong Office :
TEL:+86-755-834-335-79
FAX:+86-755-834-380-78

Japan Office :
Kawasaki Office :
TEL:+81-44-246-9100
FAX:+81-44-246-9105
Osaka Office :
TEL:+81-6-4807-5460
FAX:+81-6-4807-5461

Singapore Office :
TEL:+65-6346-5505
FAX:+65-6348-8096

Taipei Office :
TEL:+886-2-2509-3300
FAX:+886-2-2509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-262-8887
FAX:+1-408-262-8810

http : //www.macronix.com