MX23L3222

32M-BIT MASK ROM (16/32 BIT OUTPUT)

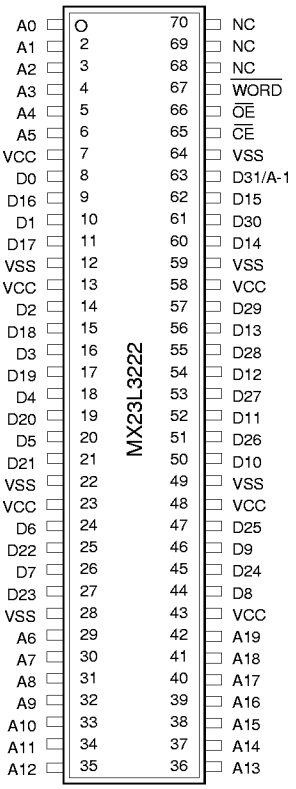
FEATURES

- Bit organization
  - 2M x 16 (word mode)
  - 1M x 32 (double word mode)
- Fast access time
  - Random access: 100ns (max.)
  - Page access: 30ns (max.)
- Page
  - 8 double words per page
- Current
  - Operating:60mA
  - Standby:50uA
- Supply voltage
  - 3.3V±10%
- Package
  - 70 pin SSOP (500mil)
  - 100 pin TQFP (14mm x 14mm)

ORDER INFORMATION

Part No.	Access Time	Page Access Time	Package
MX23L3222MC-10	100ns	30ns	70 pin SSOP
MX23L3222MC-12	120ns	45ns	70 pin SSOP
MX23L3222VC-10	100ns	30ns	100 pin TQFP
MX23L3222VC-12	120ns	45ns	100 pin TQFP

PIN CONFIGURATION



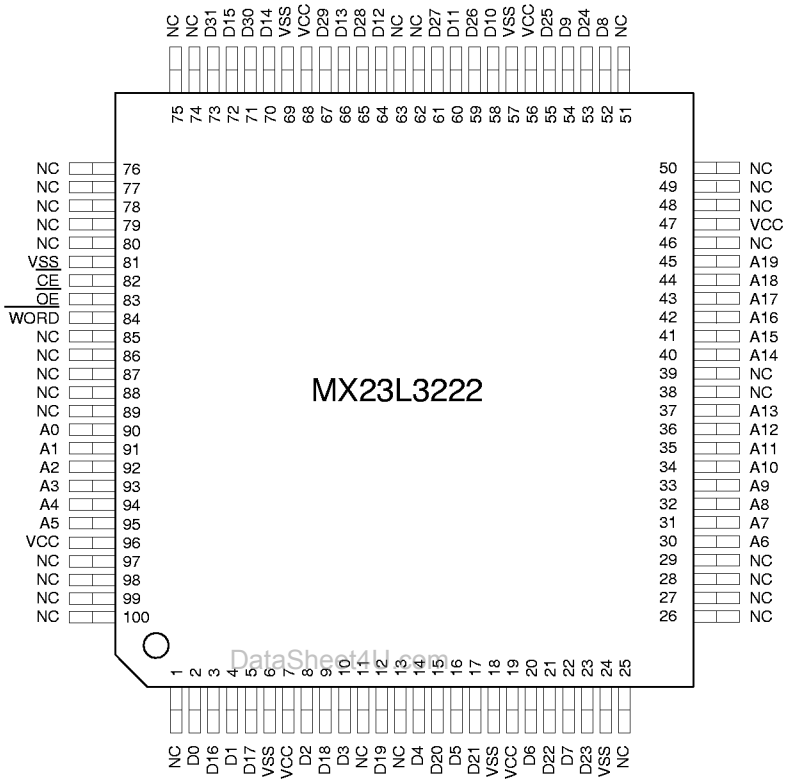
PIN DESCRIPTION

Symbol	Pin Function
A0~A19	Address Inputs
D0~D30	Data Outputs
D31/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
Byte	Double Word/ Word Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

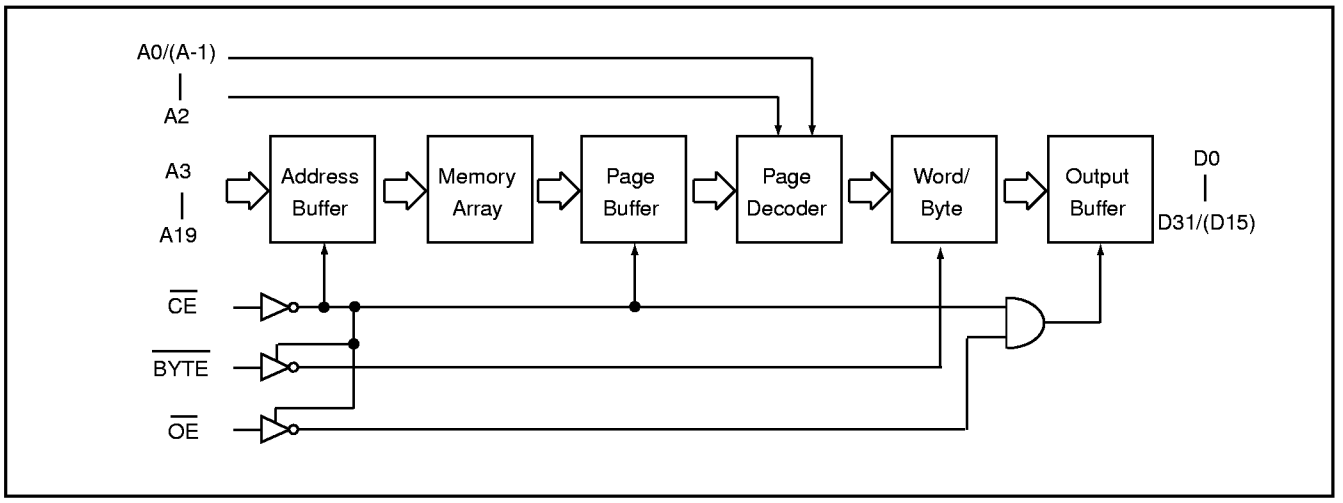
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{Word}$	D31/A-1	D0~D15	D16~D31	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D15	D16~D31	Double Word	Active
L	L	L	Input	D0~D15	High Z	Word	Active

100 TQFP



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to VCC+2.0V (Note)
Ambient Operating Temperature	Topr	0℃ to 70℃
Storage Temperature	Tstg	-65℃ to 125℃

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	60mA	tRC = 100ns, all output open
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE}$ = VIH
Standby Current (CMOS)	ISTB2	-	50uA	$\overline{CE}$>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25℃, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25℃, f = 1MHZ

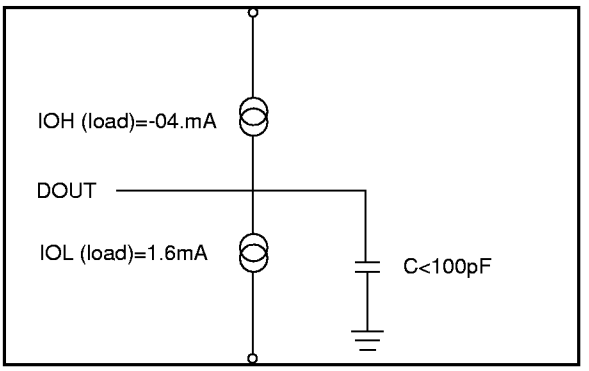
AC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 3.3V±10%)

Item	Symbol	23L3222-10		23L3222-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	30ns	-	45ns
Page Mode Access Time	tPA	-	30ns	-	45ns
Output Enable Time	tOE	-	30ns	-	45ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note:Output high-impedance delay (tHZ) is measured from $\overline{OE}$ or $\overline{CE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

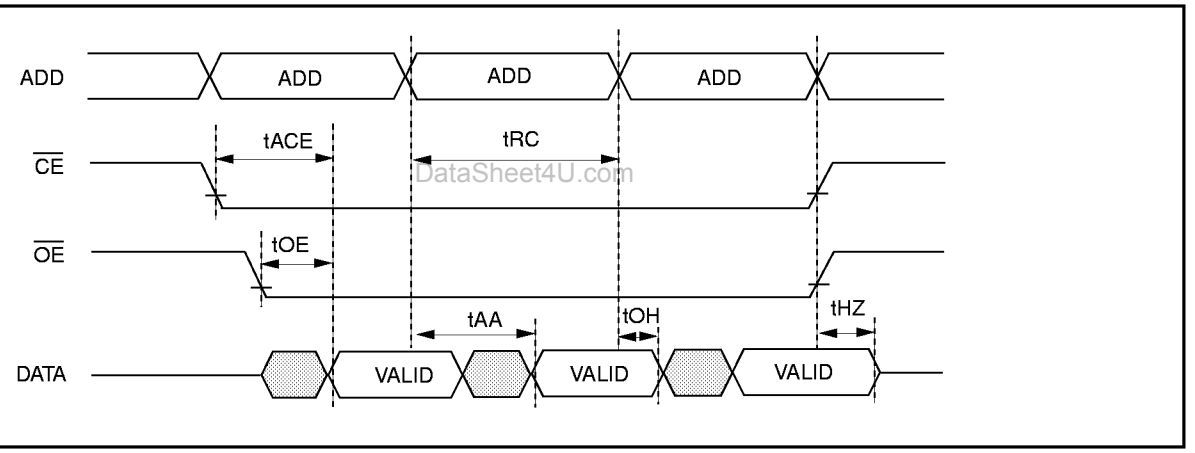
Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure



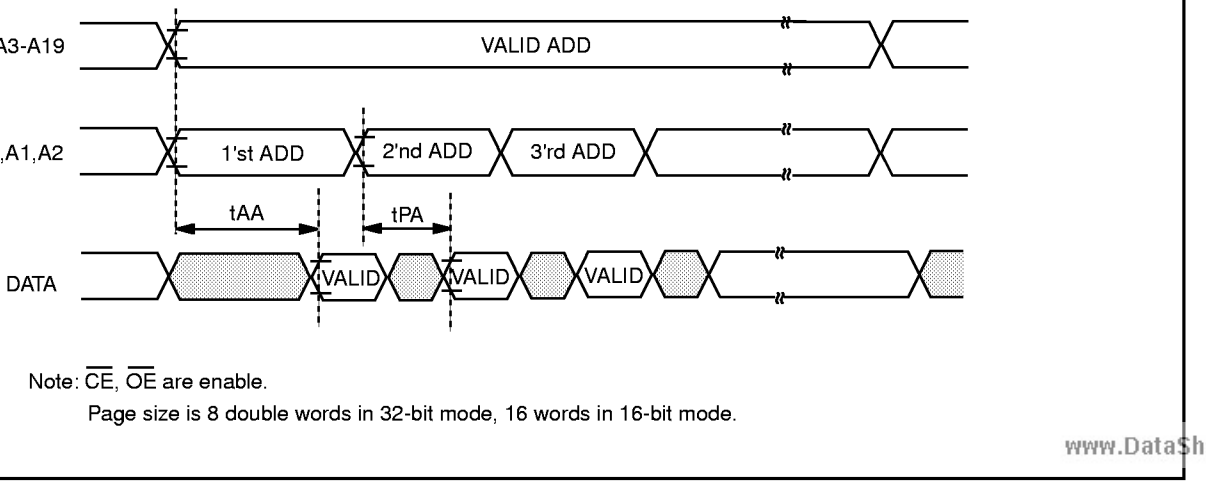
Note:No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

RANDOM READ



PAGE READ



Note: $\overline{CE}$, $\overline{OE}$ are enable.
Page size is 8 double words in 32-bit mode, 16 words in 16-bit mode.

REVISION HISTORY

Revision	Description	Page	Date
1.8	AC Characteristics: The page mode access time (tPA) and output enable time (tOE) are changed as 45ns instead of 50ns. Added 100ns speed grade. Package: Added 100 pin TQFP package, dimension is 14mm x 14mm x 1mm.		MAR/25/1998
1.9	AC CHARACTERISTICS tOH 10ns-->0ns	P3	JAN/29/1999