

DESCRIPTION

The MWS CDMA is a high-efficiency linear amplifier targeting 3V mobile handheld systems. The device is manufactured in an advanced InGaP/GaAs Heterojunction Bipolar Transistor (HBT) RF IC fab process. It is designed for use as a final RF amplifier in 3V CDMA and TDMA PCS battery-powered digital equipment (dual-mode), spread spectrum systems, and other linear applications in the 1700MHz to 1900MHz band.

There are two leadless chip carrier (LCC) package versions for this Power Amplifier family. One is a 3mm x 3mm chip scale package (CSP) with external input/output match and the other is a 6mm x 6mm internally I/O matched module.

KEY FEATURES

- Single 3V Supply
- 29dBm Linear Output Power
- 27dB Linear Gain
- 38-40% Linear Efficiency
- 70mA Idle Current

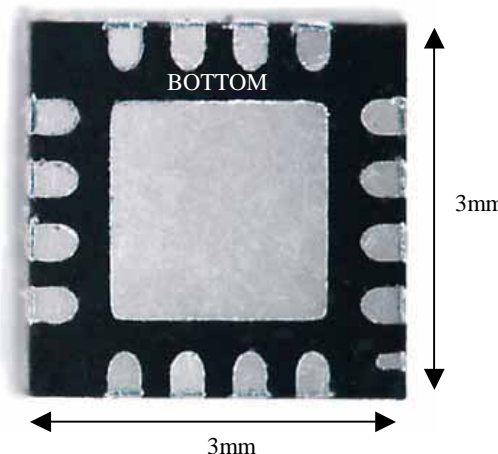
APPLICATIONS

- 3V 1710-1780MHz CDMA Handsets
- 3V 1850-1910MHz CDMA Handsets
- 3V TDMA PCS Handsets
- Spread Spectrum Systems
- Other Linear Wireless Applications

IMPORTANT: For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>

PRODUCT HIGHLIGHT

16-Pin Leadless Package




Actual Size

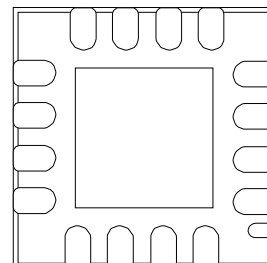
PACKAGE ORDER INFO

T_J (°C)	1700-1900MHz	3mm x 3mm Plastic MLP 16-PIN
	CDMA	MWS11-PH22-CS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{BAT})	+8.0V _{DC}
Supply Voltage ($P_{OUT} \leq 31$ dBm)	+4.5V _{DC}
Control Voltage (V_{REF})	+3.2V _{DC}
Input RF Power	+6dBm
Operating Case Temperature	-30°C to 100°C
Storage Temperature	-65°C to 150°C

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

PACKAGE PIN OUT

FUNCTIONAL PIN DESCRIPTION (16 PIN) THREE STAGE VERSION

PIN NAME	DESCRIPTION
RF IN	RF input. An external series capacitor is required as a DC block. The input match can be improved to < 2:1 by using a series capacitor and shunt inductor.
VCC1	Power supply for first stage and interstage match. V_{CC} should be fed through an inductor terminated with a capacitor on the supply side.
VCC2	Power supply for Second stage and interstage match. V_{CC} should be fed through an inductor terminated with a capacitor on the supply side.
VCC	Supply for bias reference circuits.
VB1	First stage control voltage. The VB1 pin can be connected with the other stage control voltages into a single reference voltage through an external resistor bridge.
VB2	Second stage control voltage. The VB2 pin can be connected with the other stage control voltages into a single reference voltage through an external resistor bridge.
RF OUT	RF Output and Power supply for final stage. This is the unmatched collector output of the third stage. A DC Block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1920MHz to 1980 MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability. There are three pins designated as RF OUT.
GND	This is a bias circuit level ground, isolated from the backside ground contact.
GND1	Ground for First Stage. This ground should be isolated from the backside ground contact.
GND2	Ground for Second Stage. This ground should be isolated from the backside ground contact.
PKG GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature $-35^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ except where otherwise noted. Test Conditions: $T=25^{\circ}\text{C}$, $V_{CC}=3.4\text{V}$, $P_{out}=29\text{dBm}$.

Parameter	Symbol	Test Conditions	MWS11-PH22-CS			Units
			Min	Typ	Max	
Usable Frequency Range			1750		1910	MHz
Typical Frequency Range		Tuned I/O matching network		1750 - 1780 1850 - 1910		
Linear Power Gain	G_P		24	26	28	dB
CDMA Adjacent Channel Power Rejection	ACPR	1.25MHz offset as defined by IS-95		-46	-44	dBc
Second Harmonic				-35		dBc
Third Harmonic				-40		dBc
Fourth Harmonic				-45		dBc
CDMA Noise Power		80MHz offset		-139		dBm/Hz
Linear Power-Added Efficiency	PAE		36	38	40	%
Quiescent Current	I_{CQ}	V_{REF} range: 2.6 to 2.9V	60	70	90	mA
CDMA Noise Power		80MHz offset		-139		dBm/Hz
Input VSWR				< 2:1		
Output Load VSWR		No damage			10:1	
Stability			5:1			
Power Supply Voltage	V_{CC}		3.0	3.4	4.5	V

APPLICATION

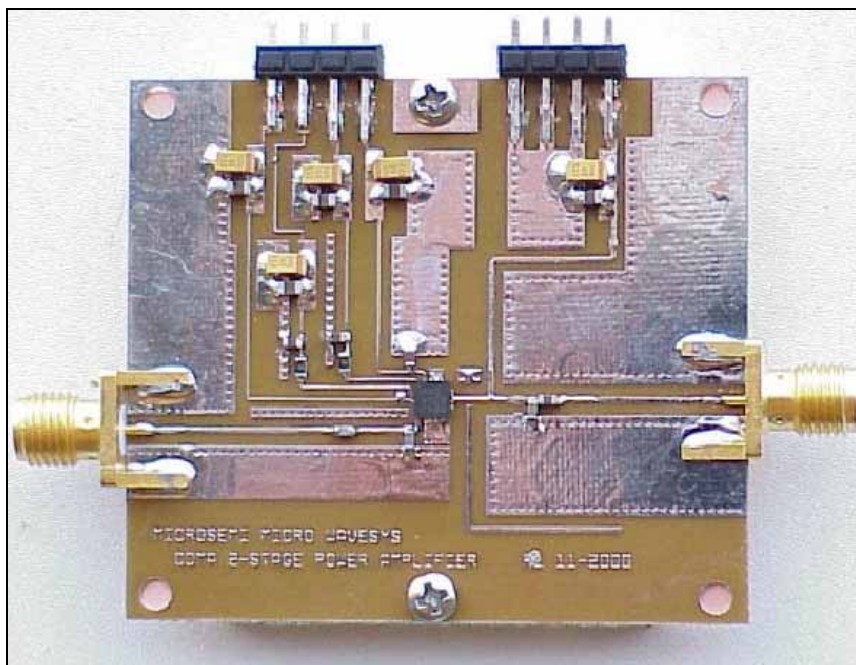


Figure 1 – Evaluation Board for the CDMA Power Amp

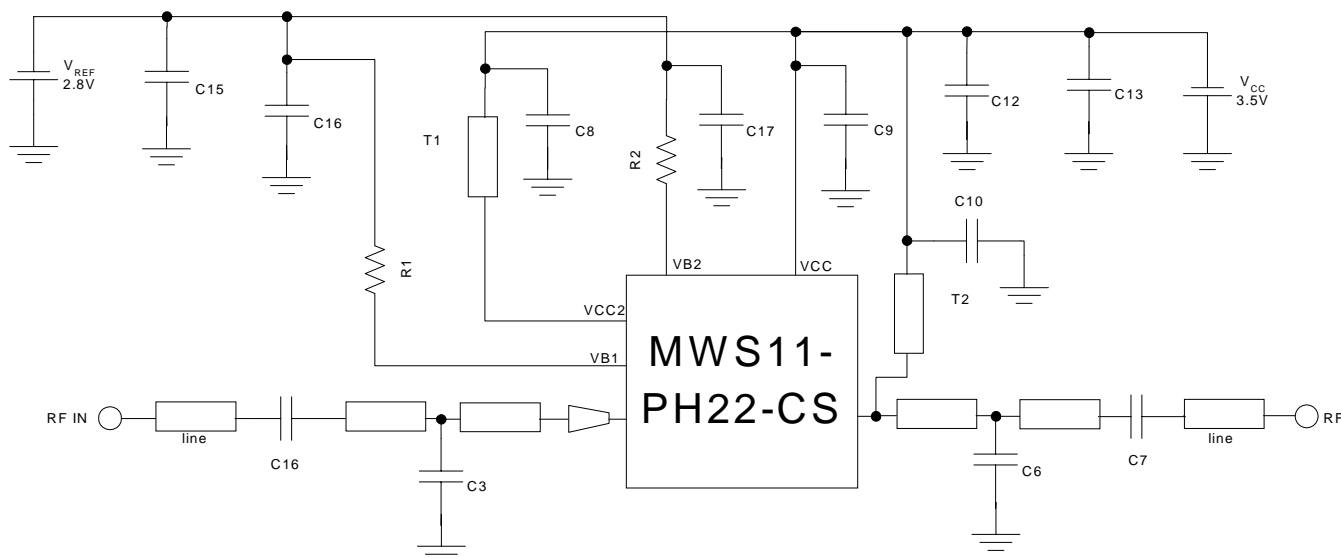


Figure 2 – Evaluation Board for the CDMA Schematic

NOTES

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