MVTX2803

Unmanaged 8-Port 1000 Mbps Ethernet Switch

Data Sheet

October 2003

Features

- Eight Gigabit Ports with GMII and PCS interface
  - Gigabit Port can also support 100/10 Mbps MII interface
- High Performance Layer 2 Packet Forwarding (23.808M packets per second) and Filtering at Full-Wire Speed
- Maximum throughput is 8 Gbps non-blocking
- Centralized shared-memory architecture
- Consists of two Memory Domains at 133 MHz
  - Frame Buffer Domain: Two banks of ZBT-SRAM with 2M/4MB total
  - Switch Database Domain with 256K/512K SRAM
- Up to 64K MAC addresses to provide large node aggregation in wiring closet switches

Ordering Information

MVTX2803AG 596 Pin HSBGA

-40°C to +85°C

Traffic Classification

- Classify traffic into 8 transmission priorities per port
- Supports Delay bounded, Strict Priority and WFQ
- Provides 2 level dropping precedence with WRED mechanism
  - User controlled thresholds for WRED
- Classification based on layer 2, 3 markings
  - VLAN Priority field in VLAN tagged frame
  - DS/TOS field in IP packet
- The precedence of above two classifications can be programmable

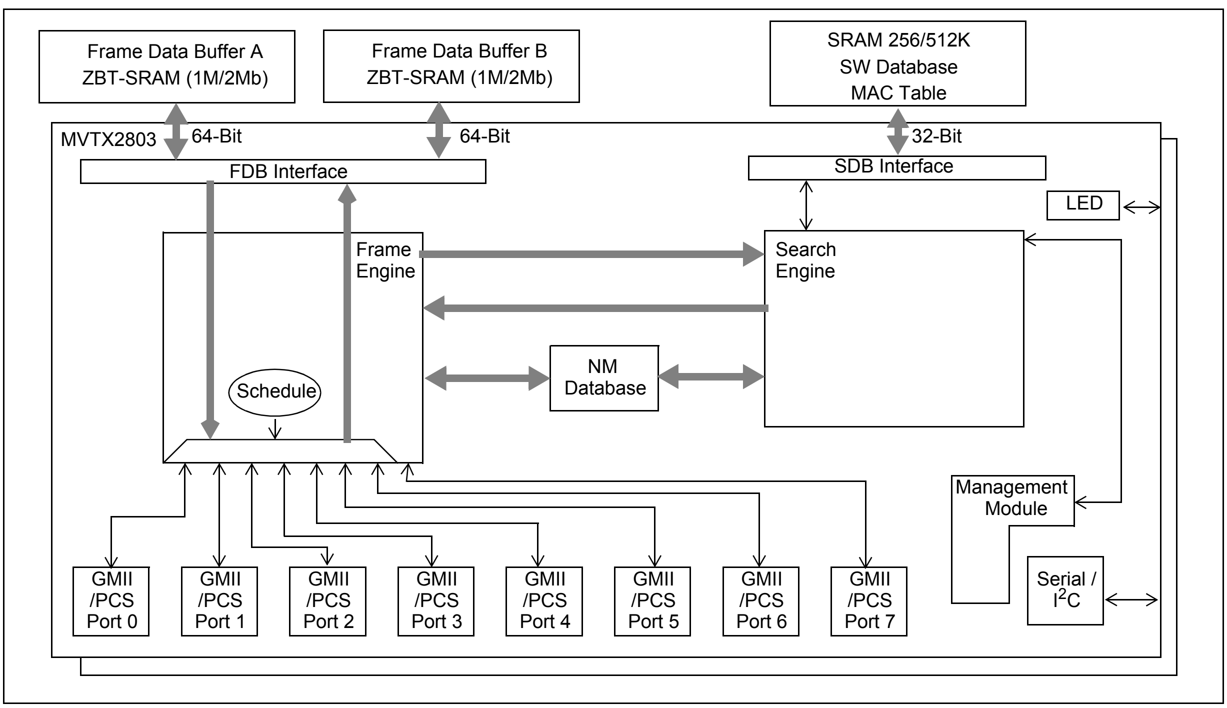

Figure 1 - MVTX2803AG Block Diagram

QoS Support

- Supports IEEE 802.1p/Q Quality of Service with 8 Priority
- Buffer Management: reserve buffers on per class and per port basis
- Port-based Priority: VLAN Priority with Tagged frame can be overwritten by the priority of PVID
- QoS features can be configured on a per port basis
- Full Duplex Ethernet IEEE 802.3x Flow Control
- Provides Ethernet Multicast and Broadcast Control
- 4 Port Trunking groups, max of 3 ports per group (Trunking can be based on source MAC and/or destination MAC and source port)
- LED signals provided by a serial or parallel interface
- Synchronous Serial Interface and I2C interface in unmanaged mode.
- Hardware auto-negotiation through serial management interface (MDIO) for Gigabit Ethernet ports, supports 10/100/1000 Mbps
- BIST for internal and external SRAM-ZBT
- I^2C EEPROM or synchronous serial port for configuration
- Packaged in 596-pin BGA

Description

The MVTX2800 family is a group of 1000 Mbps non-blocking Ethernet switch chips with on-chip address memory. A single chip provides a maximum of eight 1000 Mbps ports and a dedicated CPU interface with a 16/8 bit bus for managed and unmanaged switch applications. The MVTX2800 family consists of the following four products:

- MVTX2804 8 Gigabit ports Managed
- MVTX2803 8 Gigabit ports Unmanaged
- MVTX2802 4 Gigabit ports Managed
- MVTX2801 4 Gigabit ports Unmanaged

The MVTX2803 supports up to 64K MAC addresses to aggregate traffic from multiple wiring closet stacks. The centralized shared-memory architecture allows a very high performance packet-forwarding rate of 11.904M packets per second at full wire speed. The chip is optimized to provide a low-cost, high performance workgroup, and wiring closet, layer 2 switching solution with 8 Gigabit Ethernet ports.

Two Frame Buffer Memory domains utilize cost effective, high–performance ZBT-SRAM with aggregated bandwidth of 16Gbps to support full wire speed on all external ports simultaneously.

With Strict priority, Delay Bounded, and WRR transmission scheduling, plus WRED memory congestion scheme, the chip provides powerful QoS functions for convergent network multimedia and mission-critical applications. The chip provides 8 transmission priorities and 2 level drop precedence. Traffic is assigned its transmission priority and dropping precedence based on the frame VLAN Tag priority.

The MVTX2803AG supports port trunking/load sharing on the 1000 Mbps ports with fail-over capability. The port trunking/load sharing can be used to group ports between interlinked switches to increase the effective network bandwidth.

In full-duplex mode, IEEE 802.3x flow control is provided. The Physical Coding Sublayer (PCS) is integrated on-chip to provide a direct 10-bit GMII interface, or the PCS can be bypassed to provide an interface to existing fiber-based Gigabit Ethernet transceivers.

The MVTX2803AG is fabricated using 0.25µm technology. Inputs, however, are 3.3V tolerant and the outputs are capable of directly interfacing to LVTTL levels. The MVTX2803AG is packaged in a 596-pin Ball Grid Array package.

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1.0 Block Functionality

1.1 Frame Data Buffer (FDB) Interfaces

The FDB interface supports pipelined ZBT-SRAM memory at 133 MHz. To ensure a non-blocking switch, two memory domains are required. Each domain has a 64-bit wide memory bus. At 133 MHz, the aggregate memory bandwidth is 17 Gbps, which is enough to support 8 Gigabit ports at full wire speed switching. A patent pending scheme is used to access the FDB memory. Each slot has one tick to read or write 8 bytes.

1.2 Switch Database (SDB) Interface

A pipelined synchronous burst SRAM (SBRAM) memory is used to store the switch database information including MAC Table. Search Engine accesses the switch database via SDB interface. The SDB bus has 32-bit wide bus at 133MHz.

1.3 GMII/PCS MAC Module (GMAC)

The GMII/PCS Media Access Control (MAC) module provides the necessary buffers and control interface between the Frame Engine (FE) and the external physical device (PHY). The MVTX2803AG has two interfaces, GMII or PCS. The MAC of the MVTX2803AG meets the IEEE 802.3z specification and supports the MII interface. It is able to operate 10M/100M/1G in Full Duplex mode with a back pressure/flow control mechanism. It has the options to insert Source Address/CRC/VLAN ID to each frame. The GMII/PCS Module also supports hot plug detection.

1.4 Frame Engine

The main function of the frame engine is to forward a frame to its proper destination port or ports. When a frame arrives, the frame engine parses the frame header (64 bytes) and formulates a switching request which is sent to the search engine, to resolve the destination port. The arriving frame is moved to the FDB. After receiving a switch response from the search engine, the frame engine performs transmission scheduling based on the frame's priority. The frame engine forwards the frame to the MAC module when the frame is ready to be sent.

1.5 Search Engine

The Search Engine resolves the frame's destination port or ports according to the destination MAC address (L2) by searching the database. It also performs MAC learning, priority assignment, and trunking functions.

1.6 LED Interface

The LED interface can be operated in a serial mode or a parallel mode. In the serial mode, the LED interface uses 3 pins for carrying 8 port status signals. In the parallel mode, the interface can drive LEDs by 8 status pins. The LED port is shared with bootstrap pins. In order to avoid error when reading the bootstraps, a buffer must be used to isolate the LED circuitry from the bootstrap pins during bootstrap cycle (the bootstrap pins are sampled at the rising edge of the Reset).

1.7 Internal Memory

Several internal tables are required and are described as follows:

- Frame Control Block (FCB) - Each FCB entry contains the control information of the associated frame stored in the FDB, e.g. frame size, read/write pointer, transmission priority, etc.
- MCT Link Table - The MCT Link Table stores the linked list of MCT entries that have collisions in the external MAC Table.

2.0 System Configuration

The MVTX2803AG can be configured by EEPROM (24C02 or compatible) via an I^2C interface at boot time, or via a synchronous serial interface during operation.

2.1 I^2C Interface

The I^2C interface uses two bus lines, a serial data line (SDA) and a serial clock line (SCL). The SCL carries the control signals that facilitate the transfer of information from the EEPROM to the switch. Data transfer is a bidirectional 8-bit serial at a rate of 50 Kbps. Data transfer is performed between master and slave IC using a request / acknowledgment style of protocol. The master IC generates the timing signals and terminates data transfer. The figure below shows the data transfer format.

START	SLAVE ADDRESS	R/W	ACK	DATA 1 (8 bits)	ACK	DATA 2 (8 bits)	ACK	DATA M (8 bits)	ACK	STOP

Figure 2 - Data Transfer Format for I^2C Interface

2.1.1 Start Condition

Generated by the master, the MVTX2803AG. The bus is considered to be busy after the Start condition is generated. The Start condition occurs if, while the SCL line is High, there is a High-to-Low transition of the SDA.

Other than in the Start condition (and Stop condition), the data on the SDA line must be stable during the High period of SCL. The High or Low state of SDA can only change when SCL is Low. In addition, when the I^2C bus is free, both lines are High.

2.1.2 Address

The first byte after the Start condition determines which slave the master will select. The slave in our case is the EEPROM. The first seven bits of the first data byte make up the slave address.

2.1.3 Data Direction

The eighth bit in the first byte after the Start condition determines the direction (R/W) of the message. A master transmitter sets this bit to W; a master receiver sets this bit to R.

2.1.4 Acknowledgment

Like all clock pulses, the master generates the acknowledgment-related clock pulse. However, the transmitter releases the SDA (High) during the acknowledgment clock pulse. Furthermore, the receiver must pull down the SDA during the acknowledge pulse so that it remains stable Low during the High period of this clock pulse. An acknowledgment pulse follows every byte transfer.

If a slave receiver does not acknowledge after any byte, then the master generates a Stop condition and aborts the transfer.

If a master receiver does not acknowledge after any byte, then the slave transmitter must release the SDA line to let the master generate the Stop condition.

2.1.5 Data

After the first byte containing the address, all bytes that follow are data bytes. Each byte must be followed by an acknowledge bit. Data is transferred MSB-first.

2.1.6 Stop Condition

Generated by the master, the MVTX2803AG. The bus is considered to be free after the Stop condition is generated. The Stop condition occurs if while the SCL line is High, there is a Low-to-High transition of the SDA.

The I^2C interface serves the function of configuring the MVTX2803AG at boot time. The master is the MVTX2803AG, and the slave is the EEPROM memory.

2.2 Synchronous Serial Interface

The synchronous serial interface serves the function of configuring the MVTX2803AG *not* at boot time but via a PC. The PC serves as master and the MVTX2803AG serves as slave. The protocol for the synchronous serial interface is nearly identical to the I^2C protocol. The main difference is that there is no acknowledgment bit after each byte of data transferred.

The unmanaged MVTX2803AG uses a synchronous serial interface to program the internal registers. To reduce the number of signals required, the register address, command and data are shifted in serially through the PS_DI pin. PS_STROBE pin is used as the shift clock. PS_DO pin is used as data return path.

Each command consists of four parts.

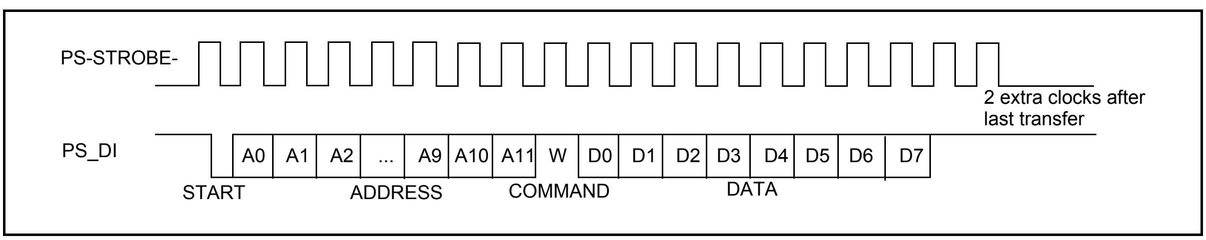
- START pulse
- Register Address
- Read or Write command
- Data to be written or read back

Any command can be aborted in the middle by sending an ABORT pulse to the MVTX2803AG.

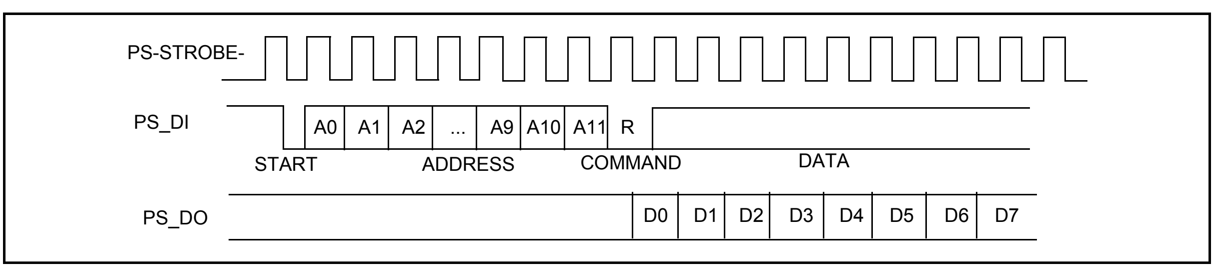
A START command is detected when PS_DI is sampled high at PS_STROBE - leading edge, and PS_DI is sampled low when STROBE- falls.

An ABORT command is detected when PS_DI is sampled low at PS_STROBE - leading edge, and PS_DI is sampled high when PS_STROBE - falls.

2.2.1 Write Command



2.2.2 Read Command



All registers in the MVTX2803AG can be modified through this synchronous serial interface.

3.0 Data Forwarding Protocol

3.1 Unicast Data Frame Forwarding

When a frame arrives, it is assigned a handle in memory by the Frame Control Buffer Manager (FCB Manager). A FCB handle will always be available, because of advance buffer reservations.

The memory (ZBT-SRAM) interface is two 64-bit buses, connected to two ZBT-SRAM domains, A and B. The Receive (RxDMA) is responsible for multiplexing the data and the address. On a port’s “turn,” the RxDMA will move 8 bytes (or up to the end-of-frame) from the port’s associated Receive FIFO (RxFIFO) into memory (Frame Data Buffer, or FDB).

Once an entire frame has been moved to the FDB, and a good end-of-frame (EOF) has been received, the Rx interface makes a switch request. The RxDMA arbitrates among multiple switch requests.

The switch request consists of the first 64 bytes of a frame, containing the source and destination MAC addresses of the frame. The search engine places a switch response in the switch response queue of the frame engine when done. Among other information, the search engine will have resolved the destination port of the frame and will have determined that the frame is unicast.

After processing the switch response, the Transmission Queue Manager (TxQ manager) of the frame engine is responsible for notifying the destination port that it has a frame to forward. But first, the TxQ manager has to decide whether or not to drop the frame, based on global FDB reservations and usage, as well as TxQ occupancy at the destination. If the frame is not dropped, then the TxQ manager links the frame’s FCB to the correct per-port-per-class TxQ. Unicast TxQ’s are linked lists of transmission jobs, represented by their associated frames’ FCB’s. There is one linked list for each transmission class for each port. There are 8 classes for each of the 8 Gigabit ports – a total of 32 unicast queues.

The TxQ manager is responsible for scheduling transmission among the queues representing different classes for a port. When the port control module determines that there is room in the MAC Transmission FIFO (TxFIFO) for another frame, it requests the handle of a new frame from the TxQ manager. The TxQ manager chooses among the head-of-line (HOL) frames from the per-class queues for that port, using a Zarlink Semiconductor scheduling algorithm.

At the transmit end, each of the 8 ports has time slots devoted solely to reading data from memory at the address calculated by port control. The Transmission DMA (TxDMA) is responsible for multiplexing the data and the address. On a port’s turn, the TxDMA will move 8 bytes (or up to the EOF) from memory into the port’s associated TxFIFO. After reading the EOF, the port control requests a FCB release for that frame. The TxDMA arbitrates among multiple buffer release requests.

The frame is transmitted from the TxFIFO to the line.

3.2 Multicast Data Frame Forwarding

After receiving the switch response, the TxQ manager has to make the dropping decision. A global decision to drop can be made, based on global FDB utilization and reservations. If so, then the FCB is released and the frame is dropped. In addition, a selective decision to drop can be made, based on the TxQ occupancy at some subset of the multicast packet’s destinations. If so, then the frame is dropped at some destinations but not others, and the FCB is not released.

If the frame is not dropped at a particular destination port, then the TxQ manager formats an entry in the multicast queue for that port and class. Multicast queues are physical queues (unlike the linked lists for unicast frames). There are 4 multicast queues for each of the 8 Gigabit ports. There is one multicast queue for every two unicast classes.

During scheduling, the TxQ manager treats the unicast queue and the multicast queue of the same class as one logical queue.

The port control requests a FCB release only after the EOF for the multicast frame has been read by all ports to which the frame is destined.

4.0 Memory Interface

4.1 Overview

Figure 3 illustrates the first part of the ZBT-SRAM interface for the MVTX2803AG. As shown, two ZBT-SRAM banks, A and B, are used, with a 64-bit bus connected to each. Each DMA can read and write from both bank A and bank B. During each tick, two memory operations will take place in parallel – one for bank A, and one for bank B. Because the clock frequency is 133 MHz, the total memory bandwidth is 128 bits $\times$ 133 MHz = 17 Gbps, for frame data buffer (FDB) access.

In addition, the figure shows that the 8 Gigabit ports are actually grouped into sets of 4. If TxDMA 0 is using bank B during a given memory slot, then TxDMA's 1-3 will never be using bank A during this same slot. As a result, TxDMA's 0-3 can share the same bank selector.

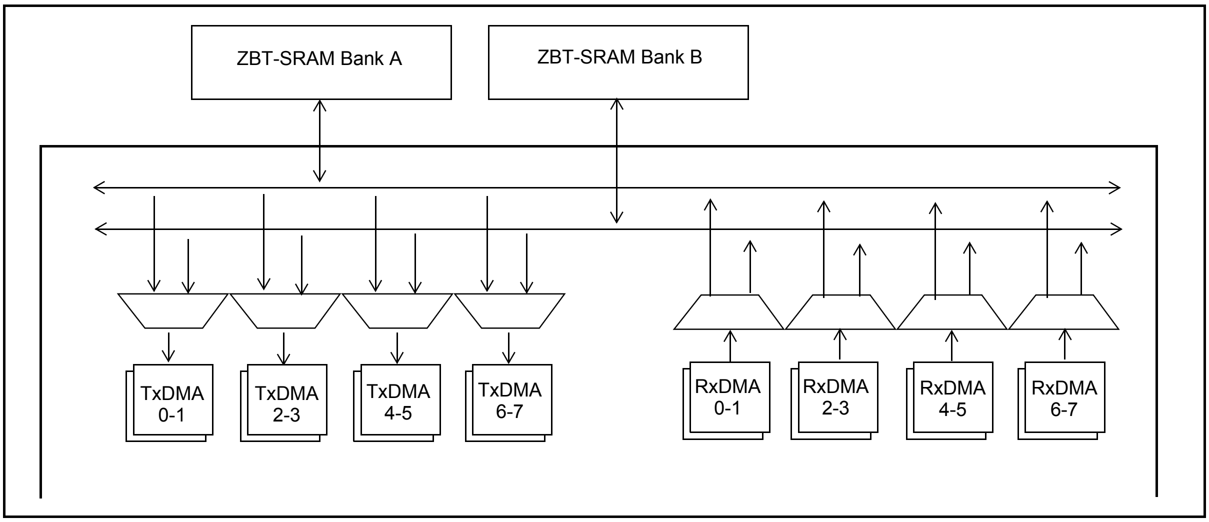


Figure 3 - MVTX2803AG SRAM Interface Block Diagram (DMAs for Gigabit Ports)

4.2 Detailed Memory Information

Because the bus for each bank is 64 bits wide, frames are broken into 8-byte granules, written to and read from memory. The first 8-byte granule gets written to Bank A, the second 8-byte granule gets written to Bank B, and so on in alternating fashion. When reading frames from memory, the same procedure is followed, first from A, then from B, and so on.

The reading and writing from alternating memory banks can be performed with minimal waste of memory bandwidth. For any speed port, in the worst case, a 1-byte-long EOF granule gets written to Bank A. This means that a 7-byte segment of Bank A bandwidth is idle, and furthermore, the next 8-byte segment of Bank B bandwidth is idle, because the first 8 bytes of the next frame will be written to Bank A, not B. This scenario results in a maximum 15 bytes of waste per frame, which is always acceptable because the interframe gap is 20 bytes.

Search engine data is written to both banks in parallel. In this way, a search engine read operation could be performed by either bank at any time without a problem.

5.0 Search Engine

5.1 Search Engine Overview

The MVTX2803AG search engine is optimized for high throughput searching, with enhanced features to support:

- Up to 64K MAC addresses
- 4 groups of port trunking
- Traffic classification into 8 transmission priorities, and 2 drop precedence levels

5.2 Basic Flow

Shortly after a frame enters the MVTX2803AG and is written to the Frame Data Buffer (FDB), the frame engine generates a Switch Request, which is sent to the search engine. The switch request consists of the first 64 bytes of the frame, which contain all the necessary information for the search engine to perform its task. When the search engine is done, it writes to the Switch Response Queue, and the frame engine uses the information provided in that queue for scheduling and forwarding.

In performing its task, the search engine extracts and compresses the useful information from the 64-byte switch request. Among the information extracted are the source and destination MAC addresses, the transmission and discard priorities and whether the frame is unicast or multicast. Requests are sent to the external SRAM Switch Database to locate the associated entries in the external MCT table.

When all the information has been collected from external SRAM, the search engine has to compare the MAC address on the current entry with the MAC address for which it is searching. If it is not a match, the process is repeated on the internal MCT Table. All MCT entries, other than the first of each linked list, are maintained internal to the chip. If the desired MAC address is still not found, then the result is either learning (source MAC address unknown) or flooding (destination MAC address unknown).

If the destination MAC address belongs to a port trunk, then the trunk number is retrieved instead of the port number. But on which port of the trunk will the frame be transmitted? This is easily computed using a hash of the source and destination MAC addresses.

When all the information is compiled, the switch response is generated, as stated earlier.

5.3 Search, Learning, and Aging

5.3.1 MAC Search

The search block performs source MAC address and destination MAC address searching. As indicated earlier, if a match is not found, then the next entry in the linked list must be examined, and so on until a match is found or the end of the list is reached.

In port based VLAN mode, a bitmap is used to determine whether the frame should be forwarded to the outgoing port. The bitmap is not dynamic. Ports cannot enter and exit groups dynamically.

The MAC search block is also responsible for updating the source MAC address timestamp, used for aging.

5.3.2 Learning

The learning module learns new MAC addresses and performs port change operations on the MCT database. The goal of learning is to update this database as the networking environment changes over time. Learning and port change will be performed based on memory slot availability only.

5.3.3 Aging

Aging time is controlled by register 400h and 401h.

The aging module scans and ages MCT entries based on a programmable "age out" time interval. As indicated earlier, the search module updates the source MAC address and VLAN port association timestamps for each frame it processes. When an entry is ready to be aged, the entry is removed from the table.

5.3.4 Data Structure

The MCT data structure is used when searching for MAC addresses. The structure is maintained by hardware in the search engine. The database is essentially a hash table, with collisions resolved by chaining. The database is partial external, and partial internal, as described earlier: the first MCT entry of each linked list is always located in the external SRAM, and the subsequent MCT's are located internally.

6.0 Frame Engine

6.1 Data Forwarding Summary

Data enters the device at the RxMAC, the RxDMA will move the data from the MAC RxFIFO to the FDB. Data is moved in 8-byte granules in conjunction with the scheme for the SRAM interface.

- A switch request is sent to the Search Engine. The Search Engine processes the switch request.
- A switch response is sent back to the Frame Engine and indicates whether the frame is unicast or multicast, and its destination port or ports.
- A Transmission Scheduling Request is sent in the form of a signal notifying the TxQ manager. Upon receiving a Transmission Scheduling Request, the device will format an entry in the appropriate Transmission Scheduling Queue (TxSch Q) or Queues. There are 8 TxSch Queues for each Gigabit port, one for each priority. Creation of a queue entry either involves linking a new job to the appropriate linked list if unicast, or adding an entry to a physical queue if multicast.
- When the port is ready to accept the next frame, the TxQ manager will get the head-of-line (HOL) entry of one of the TxSch Qs, according to the transmission scheduling algorithm (so as to ensure per-class quality of service). The unicast linked list and the multicast queue for the same port-class pair are treated as one logical queue.
- The TxDMA will pull frame data from the memory and forward it granule-by-granule to the MAC TxFIFO of the destination port.

6.2 Frame Engine Details

This section briefly describes the functions of each of the modules of the MVTX2803AG frame engine.

6.2.1 FCB Manager

The FCB manager allocates FCB handles to incoming frames, and releases FCB handles upon frame departure. The FCB manager is also responsible for enforcing buffer reservations and limits. The default values can be determined by referring to Chapter 8. In addition, the FCB manager is responsible for buffer aging, and for linking unicast forwarding jobs to their correct TxSch Q. The buffer aging can be enabled or disabled by the bootstrap pin and the aging time is defined in register FCBAT.

6.2.2 Rx Interface

The Rx interface is mainly responsible for communicating with the RxMAC. It keeps track of the start and end of frame and frame status (good or bad). Upon receiving an end of frame that is good, the Rx interface makes a switch request.

6.2.3 RxDMA

The RxDMA arbitrates among switch requests from each Rx interface. It also buffers the first 64 bytes of each frame for use by the search engine when the switch request has been made.

6.2.4 TxQ Manager

First, the TxQ manager checks the per-class queue status and global Reserved resource situation, and using this information, makes the frame dropping decision after receiving a switch response. If the decision is not to drop, the TxQ manager requests that the FCB manager link the unicast frame's FCB to the correct per-port-per-class TxQ. If multicast, the TxQ manager writes to the multicast queue for that port and class. The TxQ manager can also trigger source port flow control for the incoming frame's source if that port is flow control enabled. Second, the TxQ manager handles transmission scheduling; it schedules transmission among the queues representing different classes for a port. Once a frame has been scheduled, the TxQ manager reads the FCB information and writes to the correct port control module.

6.3 Port Control

The port control module calculates the SRAM read address for the frame currently being transmitted. It also writes start of frame information and an end of frame flag to the MAC TxFIFO. When transmission is done, the port control module requests that the buffer be released.

6.4 TxDMA

The TxDMA multiplexes data and address from port control, and arbitrates among buffer release requests from the port control modules.

7.0 Quality of Service and Flow Control

7.1 Model

Quality of service (QoS) is an all-encompassing term for which different people have different interpretations. In this chapter, quality of service assurances means the allocation of chip resources so as to meet the latency and bandwidth requirements associated with each traffic class. There is nothing presupposed about the offered traffic pattern. If the traffic load is light, then ensuring quality of service is straightforward. But if the traffic load is heavy, the MVTX2803AG must intelligently allocate resources so as to assure quality of service for high priority data.

The network manager must assign importance for the application types, such as voice, file transfer, or web browsing. The manager can then subdivide the applications into classes and set up a service contract with each. The contract may consist of bandwidth or latency assurances per class. Sometimes it may even reflect an estimate of the traffic mix offered to the switch, though this is not required.

The table below shows examples of QoS applications with eight transmission priorities, including best effort traffic for which no bandwidth or latency assurances are provided.

Class	Example Assured Bandwidth (user defined)	Low Drop Subclass (If class is oversubscribed, these packets are the last to be dropped)	High Drop Subclass (If class is oversubscribed, these packets are the first to be dropped)
Highest transmission priorities, P7 **Latency < 200 µs**	300 Mbps	**Sample application:** control information	

Table 1 - Two-dimensional World Traffic

Class	Example Assured Bandwidth (user defined)	Low Drop Subclass (If class is oversubscribed, these packets are the last to be dropped)	High Drop Subclass (If class is oversubscribed, these packets are the first to be dropped)
Highest transmission priorities, P6 **Latency < 200 µs**	200 Mbps	**Sample applications:** phone calls; circuit emulation	**Sample application:** training video; other multimedia
Middle transmission priorities, P5 **Latency < 400 µs**	125 Mbps	**Sample application:** interactive activities	**Sample application:** non-critical interactive activities
Middle transmission priorities, P4 **Latency < 800 µs**	250 Mbps	**Sample application:** web business	
Low transmission priorities, P3 **Latency < 1600 µs**	80 Mbps	**Sample application:** file backups	
Low transmission priorities, P2 **Latency < 3200 µs**	45 Mbps	**Sample application:** email	**Sample application:** web research
Best effort, P1-P0	–	**Sample application:** casual web browsing	
TOTAL	1 Gbps		

Table 1 - Two-dimensional World Traffic (continued)

It is possible that a class of traffic may attempt to monopolize system resources by sending data at a rate in excess of the contractually assured bandwidth for that class. A well-behaved class offers traffic at a rate no greater than the agreed-upon rate. By contrast, a misbehaving class offers traffic that exceeds the agreed rate. A misbehaving class is formed from an aggregation of misbehaving microflows. To achieve high link utilization, a misbehaving class is allowed to use any idle bandwidth. However, the quality of service (QoS) received by well-behaved classes must never suffer.

As Table 1 illustrates, each traffic class may have its own distinct properties and applications. As shown, classes may receive bandwidth assurances or latency bounds. In the example, P7, the highest transmission class, requires that all frames be transmitted within 0.2 ms, and receives 30% of the 1 Gbps of bandwidth at that port.

Best-effort (P1-P0) traffic forms a lower tier of service that only receives bandwidth when none of the other classes have any traffic to offer.

In addition, each transmission class has two subclasses, high-drop and low-drop. Well-behaved users should not lose packets. But poorly behaved users – users who send data at too high a rate – will encounter frame loss, and the first to be discarded will be high-drop. Of course, if this is insufficient to resolve the congestion, eventually some low-drop frames are dropped as well.

Table 1 shows that different types of applications may be placed in different boxes in the traffic table. For example, web search may fit into the category of high-loss, high-latency-tolerant traffic, whereas VoIP fits into the category of low-loss, low-latency traffic.

7.2 Four QoS Configurations

There are four basic pieces to QoS scheduling in the MVTX2803AG: strict priority (SP), delay bound, weighted fair queuing (WFQ), and best effort (BE). Using these four pieces, there are four different modes of operation, as shown in Table 2.

	P7	P6	P5	P4	P3	P2	P1	P0
Op1 (*default)*	Delay Bound						BE	
Op2	SP		Delay Bound				BE	
Op3	SP		WFQ					
Op4	WFQ							

Table 2 - Four QoS configurations per port

The default configuration is six delay-bounded queues and two best-effort queues. The delay bounds per class are 0.16 ms for P7 and P6, 0.32 ms for P5, 0.64 ms for P4, 1.28 ms for P3, and 2.56 ms for P2. Best effort traffic is only served when there is no delay-bounded traffic to be served. P1 has strict priority over P0.

There is a second configuration in which there are two strict priority queues, four delay bounded queues, and two best effort queues. The delay bounds per class are 0.32 ms for P5, 0.64 ms for P4, 1.28 ms for P3, and 2.56 ms for P2. If the user is to choose this configuration, it is important that P7-P6 (SP) traffic be either policed or implicitly bounded (e.g. if the incoming SP traffic is very light and predictably patterned). Strict priority traffic, if not admission-controlled at a prior stage to the MVTX2803AG, can have an adverse effect on all other classes' performance. P7 and P6 are both SP classes, and P7 has strict priority over P6.

The third configuration contains two strict priority queues and six queues receiving a bandwidth partition via WFQ. As in the second configuration, strict priority traffic needs to be carefully controlled.

In the fourth configuration, all queues are served using a WFQ service discipline

7.3 Delay Bound

In the absence of a sophisticated QoS server and signaling protocol, the MVTX2803AG may not be assured of the mix of incoming traffic ahead of time. To cope with this uncertainty, the delay assurance algorithm dynamically adjusts its scheduling and dropping criteria, guided by the queue occupancies and the due dates of their head-of-line (HOL) frames. As a result, latency bounds are assured for all admitted frames with high confidence, even in the presence of system-wide congestion. The algorithm identifies misbehaving classes and intelligently discards frames at no detriment to well-behaved classes. The algorithm also differentiates between high-drop and low-drop traffic with a weighted random early drop (WRED) approach. Random early dropping prevents congestion by randomly dropping a percentage of high-drop frames even before the chip's buffers are completely full, while still largely sparing low-drop frames. This allows high-drop frames to be discarded early, as a sacrifice for future low-drop frames. Finally, the delay bound algorithm also achieves bandwidth partitioning among classes.

7.4 Strict Priority and Best Effort

When strict priority is part of the scheduling algorithm, if a queue has even one frame to transmit, it goes first. Two of the four QoS configurations include strict priority queues. The goal is for strict priority classes to be used for IETF expedited forwarding (EF), where performance guarantees are required. As indicated, it is important that strict priority traffic be either policed or implicitly bounded, so as to keep from harming other traffic classes.

When best effort is part of the scheduling algorithm, a queue only receives bandwidth when none of the other classes have any traffic to offer. Two of the four QoS configurations include best effort queues. The goal is for best effort classes to be used for non-essential traffic, because there are no assurances about best effort performance. However, in a typical network setting, much best effort traffic will be transmitted, and with an adequate degree of expediency.

Because there is not any delay assurances for best effort traffic, enforcement of latency by dropping best effort traffic is not provided. Furthermore, because it is assumed that strict priority traffic is carefully controlled before entering the MVTX2803AG, a fair bandwidth partition by dropping strict priority traffic is not enforced. To summarize, dropping to enforce quality of service (i.e. bandwidth or delay) does not apply to strict priority or best effort queues. It only drops frames from best effort and strict priority queues when global buffer resources become scarce.

7.5 Weighted Fair Queuing

In some environments – for example, in an environment in which delay assurances are not required, but precise bandwidth partitioning on small time scales is essential - WFQ may be preferable to a delay-bounded scheduling discipline. The MVTX2803AG provides the user with a WFQ option with the understanding that delay assurances cannot be provided if the incoming traffic pattern is uncontrolled. The user sets eight WFQ "weights" such that all weights are whole numbers and sum to 64. This provides per-class bandwidth partitioning with error within 2%.

In WFQ mode, though frame latency is not assured, the MVTX2803AG still retains a set of dropping rules that helps to prevent congestion and trigger higher level protocol end-to-end flow control.

As before, when strict priority is combined with WFQ, there are no special dropping rules for the strict priority queues, because the input traffic pattern is assumed to be carefully controlled at a prior stage. However, there is indeed drop frames from SP queues for global buffer management purposes. In addition, queues P1 and P0 are treated as best effort from a dropping perspective, though they still are assured a percentage of bandwidth from a WFQ scheduling perspective. What this means is that these particular queues are only affected by dropping when the global buffer count becomes low.

7.6 Shaper

Although traffic shaping is not a primary function of the MVTX2803AG, the chip does implement a shaper for expedited forwarding (EF). The goal in shaping is to control the peak and average rate of traffic exiting the MVTX2803AG. Shaping is limited to class P6 (the second highest priority). This means that class P6 will be the class used for EF traffic. (By contrast, assume class P7 will be used for control packets only.) If shaping is enabled for P6, then P6 traffic must be scheduled using strict priority. With reference to Table 4, only the middle two QoS configurations may be used.

Peak rate is set using a programmable whole number, no greater than 64 (register QOS-CREDIT_C6_Gn). For example, if the setting is 32, then the peak rate for shaped traffic is 32/64 × 1000 Mbps = 500 Mbps. Average rate is also a programmable whole number, no greater than 64, and no greater than the peak rate. For example, if the setting is 16, then the average rate for shaped traffic is 16/64 × 1000 Mbps = 250 Mbps. As a consequence of the above settings in the example, shaped traffic will exit the MVTX2803AG at a rate always less than 500 Mbps, and averaging no greater than 250 Mbps.

Also, when shaping is enabled, it is possible for a P6 queue to explode in length if fed by a greedy source. The reason is that a shaper is by definition not work-conserving; that is, it may hold back from sending a packet even if the line is idle. Though there is global resource management, nothing is done to prevent this situation locally. This assumes SP traffic is policed at a prior stage to the MVTX2803AG.

7.7 WRED Drop Threshold Management Support

To avoid congestion, the Weighted Random Early Detection (WRED) logic drops packets according to specified parameters. The following table summarizes the behavior of the WRED logic.

	P7	P6	P5	P4	P3	P2	High Drop	Low Drop
Level 1 N ≥ 240	|P7| ≥ A KB	|P6| ≥ B KB	|P5| ≥ C KB	|P4| ≥ D KB	|P3| ≥ E KB	|P2| ≥ F KB	X%	0%
Level 2 N ≥ 280							Y%	Z%
Level 3 N ≥ 320							100%	100%

Table 3 - WRED Dropping Scheme

In the table, |Px| is the byte count in queue Px. The WRED logic has three drop levels, depending on the value of N, which is based on the number of bytes in the priority queues. If delay bound scheduling is used, N equals 16|P7| + 16|P6| + 8|P5| + 4|P4| + 2|P3| + |P2|. If WFQ scheduling is used, N equals |P7| + |P6| + |P5| + |P4| + |P3| + |P2|. Each drop level has defined high-drop and low-drop percentages, which indicate the percentage of high-drop and low-drop packets that will be dropped at that level. The X, Y, and Z percent parameters can be programmed using the registers RDRC0 and RDRC1. Parameters A-F are the byte count thresholds for each priority queue, and are also programmable. When using delay bound scheduling, the values selected for A-F also control the approximate bandwidth partition among the traffic classes; see application note.

7.8 Buffer Management

Because the number of frame data buffer (FDB) slots is a scarce resource, and because it is desirable to ensure that one misbehaving source port or class cannot harm the performance of a well-behaved source port or class, the concept of buffer management was produced into the MVTX2803AG. The buffer management scheme is designed to divide the total buffer space into numerous reserved regions and one shared pool, (see Figure 4).

As shown in the figure, the FDB pool is divided into several parts. A reserved region for temporary frames stores frames prior to receiving a switch response. Such a temporary region is necessary, because when the frame first enters the MVTX2803AG, its destination port and class are as yet unknown, and so the decision to drop or not needs to be temporarily postponed. This ensures that every frame can be received first before subjecting it to the frame drop discipline after classifying.

Six reserved sections, one for each of the highest six priority classes, ensure a programmable number of FDB slots per class. The lowest two classes do not receive any buffer reservation.

Another segment of the FDB reserves space for each of the 8 ports. These source port buffer reservations are programmable. These 8 reserved regions make sure that no well-behaved source port can be blocked by another misbehaving source port.

In addition, there is a shared pool, which can store any type of frame. The registers related to the Buffer Management logic are:

- PRG- Port Reservation for Gigabit Ports
- SFCB- Share FCB Size
- C2RS- Class 2 Reserved Size
- C3RS- Class 3 Reserved Size
- C4RS- Class 4 Reserved Size
- C5RS- Class 5 Reserved Size
- C6RS- Class 6 Reserved Size
- C7RS- Class 7 Reserved Size

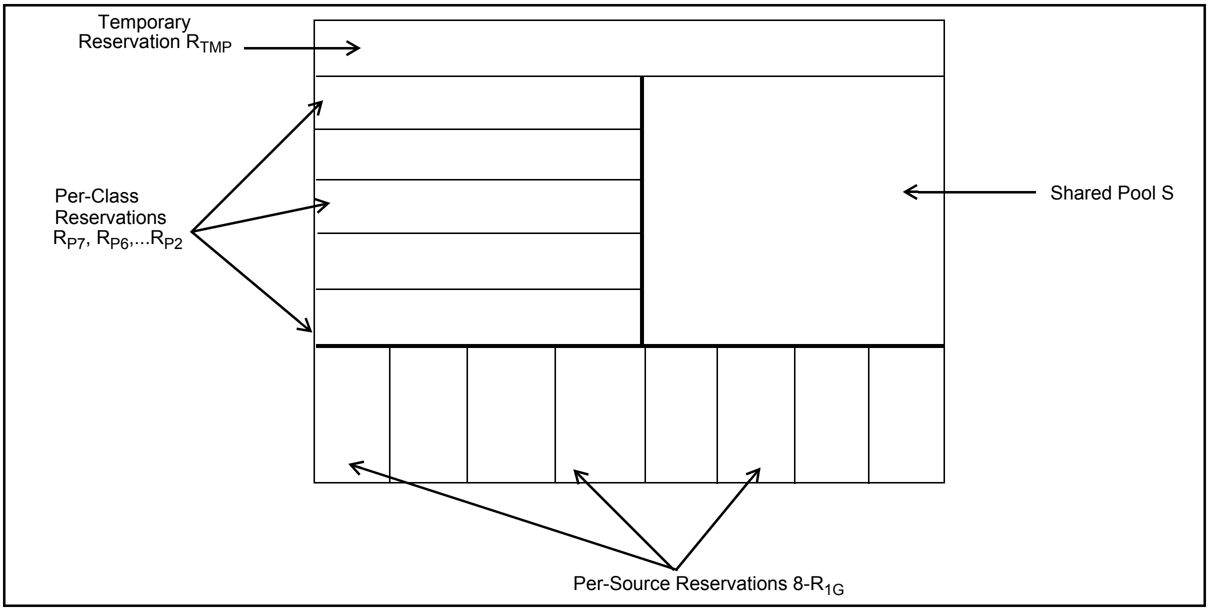


Figure 4 - Buffer Partition Scheme Used in the MVTX2803AG

7.8.1 Dropping When Buffers Are Scarce

Summarizing the two examples of local dropping discussed earlier in this chapter:

- If a queue is a delay-bounded queue, we have a multilevel WRED drop scheme, designed to control delay and partition bandwidth in case of congestion.
- If a queue is a WFQ-scheduled queue, we have a multilevel WRED drop scheme, designed to prevent congestion.

In addition to these reasons for dropping, the MVTX2803AG also drops frames when global buffer space becomes scarce. The function of buffer management is to ensure that such droppings cause as little blocking as possible.

7.9 MVTX2803AG Flow Control Basics

Because frame loss is unacceptable for some applications, the MVTX2803AG provides a flow control option. When flow control is enabled, scarcity of buffer space in the switch may trigger a flow control signal; this signal tells a source port, sending a packet to this switch, to temporarily hold off.

While flow control offers the clear benefit of no packet loss, it also introduces a problem for quality of service. When a source port receives an Ethernet flow control signal, all microflows originating at that port, well-behaved or not, are halted. A single packet destined for a congested output can block other packets destined for uncongested outputs. The resulting head-of-line blocking phenomenon means that quality of service cannot be assured with high confidence when flow control is enabled.

In the MVTX2803AG, each source port can independently have flow control enabled or disabled. For flow control enabled ports, by default all frames are treated as lowest priority during transmission scheduling. This is done so that those frames are not exposed to the WRED Dropping scheme. Frames from flow control enabled ports feed to only one queue at the destination, the queue of lowest priority. What this means is that if flow control is enabled for a given source port, then it can guarantee that no packets originating from that port will be lost, but at the possible expense of minimum bandwidth or maximum delay assurances. In addition, these "downgraded" frames may only use the shared pool or the per-source reserved pool in the FDB; frames from flow control enabled sources may not use reserved FDB slots for the highest six classes (P2-P7).

The MVTX2803AG does provide a system-wide option of permitting normal QoS scheduling (and buffer use) for frames originating from flow control enabled ports. When this programmable option is active, it is possible that some packets may be dropped, even though flow control is on. The reason is that intelligent packet dropping is a major component of the MVTX2803AG's approach to ensuring bounded delay and minimum bandwidth for high priority flows.

7.9.1 Unicast Flow Control

For unicast frames, flow control is triggered by source port resource availability. Recall that the MVTX2803AG's buffer management scheme allocates a reserved number of FDB slots for each source port. If a programmed number of a source port's reserved FDB slots have been used, then flow control Xoff is triggered. Xon is triggered when a port is currently being flow controlled, and all of that port's reserved FDB slots have been released.

Note that the MVTX2803AG's per-source-port FDB reservations assure that a source port that sends a single frame to a congested destination will not be flow controlled.

7.9.2 Multicast Flow Control

When port based Vlan is not used, a global buffer counter (64 packets) triggers flow control for multicast frames. When the system exceeds a programmable threshold of multicast packets, Xoff is triggered. Xon is triggered when the system returns below this threshold. MCC register programs the threshold. When port based Vlan is used, each Vlan has a global buffer counter.

In addition, each source port has an 8-bit port map recording which port or ports of the multicast frame's fanout were congested at the time Xoff was triggered. All ports are continuously monitored for congestion, and a port is identified as uncongested when its queue occupancy falls below a fixed threshold. When all those ports that were originally marked as congested in the port map have become uncongested, then Xon is triggered, and the 8-bit vector is reset to zero.

The MVTX2803AG also provides the option of disabling VLAN multicast flow control.

Note: If port flow control is on, QoS performance will be affected. To determine the most efficient way to program, please refer to the QoS Application Note.

7.10 Mapping to IETF Diffserv Classes

The mapping between priority classes discussed in this chapter and elsewhere is shown below.

MVTX2803AG	P7	P6	P5	P4	P3	P2	P1	P0
IETF	NM	EF	AF0	AF1	AF2	AF3	BE0	BE1

Table 4 - Mapping between MVTX2803AG and IETF Diffserv Classes for Gigabit Ports

As the table illustrates, P7 is used solely for network management (NM) frames. P6 is used for expedited forwarding service (EF). Classes P2 through P5 correspond to an assured forwarding (AF) group of size 4. Finally, P0 and P1 are two best effort (BE) classes.

Features of the MVTX2803AG that correspond to the requirements of their associated IETF classes are summarized in the following below.

Network Management (NM) and Expedited Forwarding (EF)	• Global buffer reservation for NM and EF • Shaper for EF traffic • Option of strict priority scheduling • No dropping if admission controlled
Assured Forwarding (AF)	• Four AF classes • Programmable bandwidth partition, with option of WFQ service • Option of delay-bounded service keeps delay under fixed levels even if not admission-controlled • Random early discard, with programmable levels • Global buffer reservation for each AF class
Best Effort (BE)	• Two BE classes • Service only when other queues are idle means that QoS not adversely affected • Random early discard, with programmable levels • Traffic from flow control enabled ports automatically classified as BE

Table 5 - MVTX2803AG Features Enabling IETF Diffserv Standards

8.0 Port Trunking

8.1 Features and Restrictions

A port group (i.e. trunk) can include up to 8 physical ports, but all of the ports in a group must be in the same MVTX2803AG.

The MVTX2803AG provides several pre-assigned trunk group options, containing as many as 4 ports per group, or alternatively, as many as 4 total groups.

Load distribution among the ports in a trunk for unicast is performed using hashing based on source MAC address and destination MAC address. The other options include source MAC address only, destination MAC address only. Load distribution for multicast is performed similarly.

If a VLAN includes any of the ports in a trunk group, all the ports in that trunk group should be in the same VLAN member map.

The MVTX2803AG also provides a safe fail-over mode for port trunking automatically. If one of the ports in the trunking group goes down, the MVTX2803AG will automatically redistribute the traffic over to the remaining ports in the trunk in unmanaged mode. In managed mode, the software can perform similar tasks.

8.2 Unicast Packet Forwarding

The search engine finds the destination MCT entry, and if the status field says that the destination address found belongs to a trunk, then the group number is retrieved instead of the port number. In addition, if the source address belongs to a trunk, then the source port’s trunk membership register is checked to determine if the address has moved.

A hash key is used to determine the appropriate forwarding port, based on some combination of the source and destination MAC addresses for the current packet.

The search engine retrieves the VLAN member ports from the VLAN index table, which consists of 4K entries.

The search engine retrieves the VLAN member ports from the ingress port’s VLAN map. Based on the destination MAC address, the search engine determines the egress port from the MCT database. If the egress port is a member of a trunk group, the packet can be distributed to the other members of that trunk group. The

VLAN map is used to check whether the egress port is a member of the VLAN, based on the ingress port. If it is a member, the packet is forwarded otherwise it is discarded.

8.3 Multicast Packet Forwarding

For multicast packet forwarding, the device must determine the proper set of ports from which to transmit the packet based on the VLAN index and hash key.

Two functions are required in order to distribute multicast packets to the appropriate destination ports in a port trunking environment.

- Determining one forwarding port per group.
- For multicast packets, all but one port per group, the forwarding port, must be excluded.

8.4 Preventing Multicast Packets from Looping Back to the Source Trunk

The search engine needs to prevent a multicast packet from sending to a port that is in the same trunk group with the source port. This is because, when selecting the primary forwarding port for each group, it does not take the source port into account. To prevent this, simply apply one additional filter, so as to block that forwarding port for this multicast packet.

9.0 LED Interface

9.1 Introduction

The MVTX2803AG LED block provides two interfaces: a serial output channel, and a parallel time-division interface. The serial output channel provides port status information from the MVTX2803AG chip in a continuous serial stream. This means that a low cost external device must be used to decode the serial data and to drive an LED array for display.

By contrast, the parallel time-division interface supports a glueless LED module. Indeed, the parallel interface can directly drive low-current LEDs without any extra logic. The pin LED_PM is used to select serial or parallel mode.

For some LED signals, the interface also provides a blinking option. Blinking may be enabled for LED signals TxD, RxD, COL, and FC (to be described later). The pin LED_BLINK is used to enable blinking, and the blinking frequency is around 160 ms.

9.2 Serial Mode

In serial mode, the following pins are utilized:

- LED_SYNCO – a sync pulse that defines the boundary between status frames
- LED_CLKO – the clock signal
- LED_DO – a continuous serial stream of data for all status LEDs that repeats once every frame time

In each cycle (one frame of status information, or one sync pulse), 16×8 bits of data are transmitted on the LED_DO signal. The sequence of transmission of data bits is as shown in the figure below:

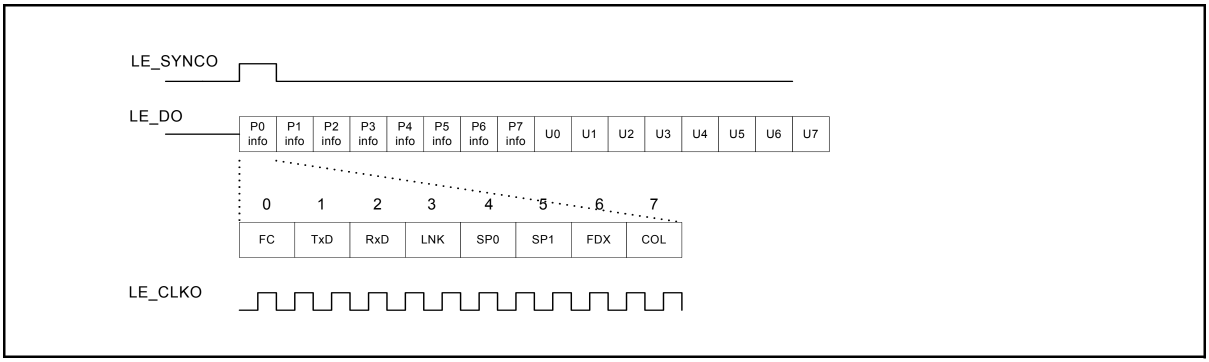


Figure 5 - Timing diagram for serial mode in LED interface

The status bits shown in here are flow control (FC), transmitting data (TxD), receiving data (RxD), link up (LNK), speed (SP0 and SP1), full duplex (FDX), and collision (COL). Note that SP[1:0] is defined as 10 for 1 Gbps, 01 for 100 Mbps, and 00 for 10 Mbps.

Also note that U0-U7 represent user-defined sub-frames in which additional status information may be embedded. We will see later that the MVTX2803AG provides registers that can be written by the CPU to indicate this additional status information as it becomes available.

9.3 Parallel Mode

In parallel mode, the following pins are utilized:

- LED_PORT_SEL[9:0] – indicates which of the 8 Gigabit port status bytes or 2 user-defined status bytes is being read out
- LED_BYTEOUT_[7:0] – provides 8 bits for 8 different port status indicators. Note that these bits are active low.

By default, the system is in parallel mode. In parallel mode, the 10 status bytes are scanned in a continuous loop, with one byte read out per clock cycle, and the appropriate port select bit asserted.

9.4 LED Control Registers

An LED Control Register can be used for programming the LED clock rate, sample hold time, and pattern in parallel mode.

In addition, the MVTX2803AG provides 8 registers called LEDUSER[7:0] for user-defined status bytes. During operation, the CPU can write values to these registers, which will be read out to the LED interface output (serial or parallel). Only LEDUSER[1:0] are used in parallel mode. The content of the LEDUSER registers will be sent out by the LED serial shift logic, or in parallel mode, a byte at a time.

Because in parallel mode there are only two user-defined registers, LEDUSER[7:2] is shared with LEDSIG[7:2].

For LEDSIG[j], where j = 2, 3, ..., 6, the corresponding register is used for programming the LED pin LED_BYTEOUT_[j]. The format is as follows:

7			4	3			0
COL	FDX	SP1	SP0	COL	FDX	SP1	SP0

Bits [3:0] Signal polarity: 0: do not invert polarity (high true)

1: invert polarity

Bits [7:4] Signal select: 0: do not select

1: select the corresponding bit

For j = 2, 3, 4, 5, the value of LED_BYTEOUT_[j] equals the logical AND of all selected bits. For j = 6, the value is equal to the logical OR. Therefore, the programmable LEDSIG[5:2] registers allow any conjunctive formula including any of the 4 status bits (COL, FDX, SP1, SP0) or their negations to be sent to the LED_BYTEOUT_[5:2] pins. Similarly, the programmable LEDSIG[6] register allows any disjunctive formula including any of the 4 status bits or their negations to be sent to pin LED_BYTEOUT_[6].

LEDSIG[7] is used for programming both LED_BYTEOUT_[1] and LED_BYTEOUT_[0]. As we will see, it has other functions as well. The format is as follows:

7			4	3			0
GP	RxD	TxD	FC	P6	RxD	TxD	FC

Bits [7] Global output polarity: this bit controls the output polarity of all LED_BYTEOUT_ and LED_PORT_SEL pins. **(Default 0)**
0: do not invert polarity (LED_BYTEOUT_[7:0] are high activated; LED_PORT_SEL[9:0] are low activated)
1: invert polarity (LED_BYTEOUT_[7:0] are low activated; LED_PORT_SEL[9:0] are high activated)

Bits [6:4] Signal select:
0: do not select
1: select the corresponding bit
The value of LED_BYTEOUT_[1] equals the logical OR of all selected bits. **(Default 110)**

Bit [3] Polarity control of LED_BYTEOUT_[6] **(Default 0)**
0: do not invert
1: invert

Bits [2:0] Signal select:
0: do not select
1: select the corresponding bit
The value of LED_BYTEOUT_[0] equals the logical OR of all selected bits. (**Default 001)**

10.0 Register Definition

10.1 MVTX2803AG Register Description

Register	Description	CPU Addr (Hex)	R/W	I^2C Addr (Hex)	Default	Notes
ETHERNET Port Control Registers – Substitute [N] with Port number (0..7)						
ECR1P"N"	Port Control Register 1 for Port N (N=0-7)	000 + 2N	R/W	000+2N	c0	
ECR2P"N"	Port Control Register 2 for Port N (N=0-7)	001 + 2N	R/W	001+2N	00	
GGCONTROL0	Extra Gigabit Port Control –port 0,1	012	R/W	N/A	00	

Register	Description	CPU Addr (Hex)	R/W	I^2C Addr (Hex)	Default	Notes
GGCONTROL1	Extra Gigabit Port Control –port 2,3	013	R/W	N/A	00	
GGCONTROL2	Extra Gigabit Port Control –port 4,5	014	R/W	N/A	00	
GGCONTROL3	Extra Gigabit Port Control –port 6,7	015	R/W	N/A	00	
ACTIVELINK	Active Link status port 7:0	016	R/W	N/A	00	
VLAN Control Registers – Substitute [N] with Port number (0..8)						
AVTCL	VLAN Type Code Register Low	100	R/W	012	00	
AVTCH	VLAN Type Code Register High	101	R/W	013	81	
PVMAP”N”_0	Port “N” Configuration Register 0 (N=0-8)	102 + 4N	R/W	014+4N	ff	
PVMAP”N”_3	Port “N” Configuration Register 3 (N=0-8)	105 + 4N	R/W	017+4N	00	
PVMODE	VLAN Operating Mode	126	R/W	038	00	
TRUNK Control Registers						
TRUNK0_MODE	Trunk Group 0 Mode	207	R/W	039	00	
TRUNK1_MODE	Trunk Group 1 Mode	20E	R/W	03A	00	
CPU Port Configuration						
TX_AGE	Transmission Queue Aging Time	312	R/W	03B	08	
Search Engine Configurations						
AGETIME_LOW	MAC Address Aging Time Low	400	R/W	03C	2c	
AGETIME_HIGH	MAC Address Aging Time High	401	R/W	03D	00	
SE_OPMODE	Search Engine operation mode	403	R/W	NA	00	
Buffer Control and QOS Control						
FCBAT	FCB Aging Timer	500	R/W	03E	ff	
QOSC	QOS Control	501	R/W	03F	00	
FCR	Flooding Control Register	502	R/W	040	08	
AVPML	VLAN Priority Map Low	503	R/W	041	88	
AVPMM	VLAN Priority Map Middle	504	R/W	042	c6	
AVPMH	VLAN Priority Map High	505	R/W	043	fa	

Register	Description	CPU Addr (Hex)	R/W	I^2C Addr (Hex)	Default	Notes
TOSPML	TOS Priority Map Low	506	R/W	044	88	
TOSPMM	TOS Priority Map Middle	507	R/W	045	c6	
TOSPMH	TOS Priority Map High	508	R/W	046	fa	
AVDM	VLAN Discard Map	509	R/W	047	00	
TOSDML	TOS Discard Map	50A	R/W	048	00	
BMRC	Broadcast/Multicast Rate Control	50B	R/W	049	00	
UCC	Unicast Congestion Control	50C	R/W	04A	07	
MCC	Multicast Congestion Control	50D	R/W	04B	48	
PR100	Port Reservation for 10/100 Ports	50E	R/W	04C	00	
PRG	Port Reservation for Giga Ports	50F	R/W	04D	26	
SFCB	Share FCB Size	510	R/W	04E	37	
C2RS	Class 2 Reserved Size	511	R/W	04F	00	
C3RS	Class 3 Reserved Size	512	R/W	050	00	
C4RS	Class 4 Reserved Size	513	R/W	051	00	
C5RS	Class 5 Reserved Size	514	R/W	052	00	
C6RS	Class 6 Reserved Size	515	R/W	053	00	
C7RS	Class 7 Reserved Size	516	R/W	054	00	
QOSC"N"	QOS Control (N=0 – 2F)	517–546	R/W	055-084		
QOSC"N"	QOS Control (N=30 – 82)	547-599	R/W	NA		
RDRC0	WRED Rate Control 0	59A	R/W	085	8e	
RDRC1	WRED Rate Control 1	59B	R/W	086	68	
MISC Configuration Registers						
MII_OP0	MII Register Option 0	600	R/W	0B1	00	
MII_OP1	MII Register Option 1	601	R/W	0B2	00	
FEN	Feature Registers	602	R/W	0B3	10	
MIIC0	MII Command Register 0	603	R/W	N/A	00	
MIIC1	MII Command Register 1	604	R/W	N/A	00	
MIIC2	MII Command Register 2	605	R/W	N/A	00	
MIIC3	MII Command Register 3	606	R/W	N/A	00	
MIID0	MII Data Register 0	607	RO	N/A	00	

Register	Description	CPU Addr (Hex)	R/W	I^2C Addr (Hex)	Default	Notes
MIID1	MII Data Register 1	608	RO	N/A	00	
LED	LED Control Register	609	R/W	0B4	38	
CHECKSUM	EEPROM Checksum Register	60B	R/W	0C5	00	
LEDUSER0	LED User Define Register 0	60C	R/W	0BB	00	
LEDUSER1	LED User Define Register 1	60D	R/W	0BC	00	
LEDUSER2	LED User Define Reg. 2/LED_byte pin 2	60E	R/W	0BD	80	
LEDUSER3	LED User Define Reg. 3/LED_byte pin 3	60F	R/W	0BE	33	
LEDUSER4	LED User Define Reg. 4/LED_byte pin 4	610	R/W	0BF	32	
LEDUSER5	LED User Define Reg. 5/LED_byte pin 5	611	R/W	0C0	20	
LEDUSER6	LED User Define Reg. 6/LED_byte pin 6	612	R/W	0C1	40	
LEDUSER7	LED User Define Reg. 7/LED_byte pin 1 & 0	613	R/W	0C2	61	
MIINP0	MII NEXT PAGE DATA REGISTER0	614	R/W	0C3	00	
MIINP1	MII NEXT PAGE DATA REGISTER1	615	R/W	0C4	00	
Test Group Control						
DTSRL	Test Register Low	E00	R/W	N/A	00	
DTSRM	Test Register Medium	E01	R/W	N/A	01	
DTSRH	Test Register High	E02	R/W	N/A	00	
TDRB0	TEST MUX read back register [7:0]	E03	RO	N/A		
TDRB1	TEST MUX read back register [15:8]	E04	RO	N/A		
DTCR	Test Counter Register	E05	R/W	N/A	00	
MASK0	MASK Timeout 0	E06	R/W	0B6	00	
MASK1	MASK Timeout 1	E07	R/W	0B7	00	
MASK2	MASK Timeout 2	E08	R/W	0B8	00	
MASK3	MASK Timeout 3	E09	R/W	0B9	00	
MASK4	MASK Timeout 4	E0A	R/W	0BA	00	

Register	Description	CPU Addr (Hex)	R/W	I^2C Addr (Hex)	Default	Notes
Device Configuration Register						
GCR	Global Control Register	F00	R/W	N/A	00	
DCR	Device Status and Signature Register	F01	RO	N/A		
DCR01	Gigabit Port0 Port1 Status Register	F02	RO	NA		
DCR23	Gigabit Port2 Port3 Status Register	F03	RO	NA		
DCR45	Gigabit Port4 Port5 Status Register	F04	RO	NA		
DCR67	Gigabit Port6 Port7 Status Register	F05	RO	NA		
DPST	Device Port Status Register	F06	R/W	N/A	00	
DTST	Data read back register	F07	RO	N/A		
PLLCR	PLL Control Register	F08	R/W	N/A	00	
LCLKCR	LCLK Control Register	F09	R/W	N/A	00	
BCLKCR	BCLK Control Register	F0A	R/W	N/A	00	
BSTRRB0	BOOT STRAP read back register 0	F0B	RO	N/A		
BSTRRB1	BOOT STRAP read back register 1	F0C	RO	N/A		
BSTRRB2	BOOT STRAP read back register 2	F0D	RO	N/A		
BSTRRB3	BOOT STRAP read back register 3	F0E	RO	N/A		
BSTRRB4	BOOT STRAP read back register 4	F0F	RO	N/A		
BSTRRB5	BOOT STRAP read back register 5	F10	RO	N/A		
DA	DA Register	FFF	RO	N/A	da	

Note: 1. se = Search Engine
Note: 2. fe = Frame Engine
Note: 3. pgs = Port Group01, 23, 45, and 67
Note: 4. mc = MAC Control
Note: 5. tm = time

10.2 Group 0 Address - MAC Ports Group

10.2.1 ECR1Pn: Port N Control Register

I^2C Address h00+2n; Serial Interface Address:h000+2n (n=0 to 7)

Accessed by serial interface and I^2C (R/W)

7	6	5	4	3	2	1	0
Sp State		A-FC	Port Mode				

Bit [4:0] Port Mode (Default 2'b00)

Bit [4:3] 00 - Automatic Enable Auto-Negotiation – This enables hardware state machine for auto-negotiation.
01 - Limited Disable auto-Negotiation – This disables hardware for speed auto-negotiation. Hardware Polls MII for link status.
10 - Link Down - Force link down (disable the port). Does not talk to PHY.
11 - Link Up – Does not talk to PHY. User ERC1 [2:0] for config.

Bit [2] 1 – 10Mbps (Default 1'b0)
0 – 100Mbps
Bit 2 is used only when the port is in MII (10/100) mode.

Bit [1] 1 – Half Duplex (Do not use) **(Default 1'b0)**
0 – Full Duplex

Bit [0] 1 – Flow Control Off **(Default 1'b0)**
0 – Flow Control On

When flow control is on:
In full duplex mode, the MAC transmitter sends Flow Control Frames when necessary. The MAC receiver interprets and processes incomming flow control frames. The Flow Control Frame Received counter is incremented whenever a flow control frame is received.

When flow control is off:
In full duplex mode, the MAC transmitter does not send flow control frames. The MAC receiver does not interpret or process the flow control frames. The Flow Control Frame Receiver counter is not incremented.

Bit [5] Asymmetric Flow Control Enable.
0 – Disable asymmetric flow control
1 – Enable asymmetric flow control
When this bit is set, and flow control is on (bit[0] = 0), don't send out a flow control frame. But MAC Receiver interprets and process flow control frames. **(Default is 0)**

Bit [7:6] SS - Spanning tree state (802.1D spanning tree protocol). **(Default 2'b11)**
00 – Blocking: Frame is dropped
01 - Listening: Frame is dropped
10 - Learning: Frame is dropped. Source MAC address is learned.
11 - Forwarding: Frame is forwarded. Source MAC address is learned.

10.2.2 ECR2Pn: Port N Control Register

I^{2}C Address: 01+2n; Serial Interface Address:h001+2n (n=0to7)

Accessed by serial interface (R/W)

7	5	3	2	1	0
Security En			DisL	Ftf	Futf

Bit[0]: Filter untagged frame **(Default 0)**
0: Disable
1: Enable – All untagged frames from this port are discarded or follow security option when security is enable

Bit[1]: Filter Tag frame **(Default 0)**
0: Disable
1: Enable - All tagged frames from this port are discarded or follow security option when security is enable

Bit[2]: Learning Disable **(Default 0)**
0: Learning is enabled on this port
1: Learning is disabled on this port

Bit [5:3:] Reserved

Bit[7:6] Security Enable (Default 00). The MVTX2804AG checks the incoming data for one of the following conditions:
If the source MAC address of the incoming packet is in the MAC table and is defined as secure address but the ingress port is not the same as the port associated with the MAC address in the MAC table.
A MAC address is defined as secure when its entry at MAC table has static status and bit 0 is set to 1. MAC address bit 0 (the first bit transmitted) indicates whether the address is unicast or multicast. As source addresses are always unicast bit 0 is not used (always 0). MVTX2804 uses this bit to define secure MAC addresses.
If the port is set as learning disable and the source MAC address of the incoming packet is not defined in the MAC address table.
If the port is configured to filter untagged frames and an untagged frame arrives or if the port is configured to filter tagged frames and a tagged frame arrives.

If one of these three conditions occurs, the packet will be handled according to one of the following specified options:
00 – Disable port security
01 – Enable port security. Port will be disabled when security violation is detected
10 – N/A
11 – N/A

10.2.3 GGControl 0– Extra GIGA Port Control

Serial Interface Address:h012

Accessed by and serial interface (R/W)

7	6	5	4	4	2	1	0
		MII1	Rst1			MII0	Rst0

Bit[0]: Reset GIGA port 0 (**Default is 0)**
0: Normal operation
1: Reset Gigabit port 0.

Bit[1]: GIGA port 0 use MII interface (10/100M) (**Default is 0)**
0: Gigabit port operation at 1000M mode
1: Gigabit port operation at 10/100M mode (MII)

Bit[3:2]: Reserved -Must be '0' **(Default 0)**

Bit[4]: Reset GIGA port 1 (**Default 0)**
0: Normal operation
1: Reset Gigabit port 1.

Bit[5]: GIGA port 1 use MII interface (10/100M) (**Default 0)**
0: Gigabit port operation at 1000M mode
1: Gigabit port operation at 10/100M mode (MII)

Bit[7:6]: Reserved - Must be '0' **(Default 0)**

10.2.4 GGControl 1– Extra GIGA Port Control

Serial Interface Address:h013

Accessed by CPU and serial interface (R/W)

7	6	5	4	3	2	1	0
		MII3	Rst3			MII2	Rst2

Bit[0]: Reset GIGA port 2 **Default is 0**
0: Normal operation
1: Reset Gigabit port 2

Bit[1]: GIGA port 2 use MII interface (10/100M) **Default is 0**
0: Gigabit port operation at 1000M mode
1: Gigabit port operation at 10/100M mode (MII)

Bit[3:2]: Reserved - Must be '0' **(Default '0')**

Bit[4]: Reset GIGA port 3 **Default is 0**
0: Normal operation
1: Reset Gigabit port 3.

Bit[5]: GIGA port 3 use MII interface (10/100M) **Default is 0**
0: Gigabit port operation at 1000M mode
1: Gigabit port operation at 10/100M mode (MII)

Bit[7:6]: Reserved - Must be '0' **(Default '0')**

10.2.5 GGControl 2– Extra GIGA Port Control

Serial Interface Address:h014

Accessed by CPU and serial interface (R/W)

7	6	5	4	3	2	1	0
		MII5	Rst5			MII4	Rst4

Bit[0]: Reset GIGA port 4 **Default is 0**
0: Normal operation
1: Reset Gigabit port 4.

Bit[1]: GIGA port 4 use MII interface (10/100M) **Default is 0**
0: Gigabit port operation at 1000M mode
1: Gigabit port operation at 10/100M mode (MII)

Bit[3:2]: Reserved - Must be '0' **(Default 0)**

Bit[4]: Reset GIGA port 5 **Default is 0**
0: Normal operation
1: Reset Gigabit port 5.

Bit[5]: GIGA port 5 use MII interface (10/100M) **Default is 0**
0: Gigabit port operation at 1000M mode
1: Gigabit port operation at 10/100M mode (MII)

Bit[7:6]: Reserved - Must be '0' **(Default 0)**

10.2.6 GGControl 3– Extra GIGA Port Control

Serial Interface Address:h015

Accessed by CPU and serial interface (R/W)

7	6	5	4	3	2	1	0
		MII7	Rst7			MII6	Rst6

Bit[0]: Reset GIGA port 6 **Default is 0**
0: Normal operation
1: Reset Gigabit port 6.

Bit[1]: GIGA port 6 use MII interface (10/100M) **Default is 0**
0: Gigabit port operation at 1000M mode
1: Gigabit port operation at 10/100M mode (MII)

Bit[3:2]: Reserved - Must be '0' **(Default 0)**

Bit[4]: Reset GIGA port 7 **Default is 0**
0: Normal operation
1: Reset Gigabit port 7.

Bit[5]: GIGA port 7 use MII interface (10/100M) **Default is 0**
0: Gigabit port operation at 1000M mode
1: Gigabit port operation at 10/100M mode (MII)

Bit[7:6]: Reserved - Must be '0' **(Default 0)**

10.3 Group 1 Address - VLAN Group

10.3.1 AVTCL – VLAN Type Code Register Low

I^2C Address h12; Serial Interface Address:h100

Accessed by serial interface and I^2C (R/W)

Bit[7:0]: VLANType_LOW: Lower 8 bits of the VLAN type code (Default 00)

10.3.2 AVTCH – VLAN Type Code Register High

I^2C Address h13; Serial Interface Address:h101

Accessed by serial interface and I^2C (R/W)

Bit [7:0] VLANType_HIGH: Upper 8 bits of the VLAN type code (Default is 81)

10.3.3 PVMAP00_0 – Port 00 Configuration Register 0

I^2C Address h14, Serial Interface Address:h102

Accessed by serial interface and I^2C (R/W)

Port Based VLAN Mode

This register indicates the legal egress ports. Example: A “1” on bit 7 means that packets arriving on port 0 can be sent to port 7. A “0” on bit 7 means that any packet destined to port 7 will be discarded.

Bit[7:0]: VLAN Mask for ports 7 to 0 (Default FF)
0 – Disable
1 - Enable

10.3.4 PVMAP00_3 – Port 00 Configuration Register 3

I^2C Address h17, Serial Interface Address:h105)

Accessed by serial interface and I^2C (R/W)

Port Based Mode

7	6	5 3	2	1	0
FP en	Drop	Default TX priority	FNT	IF	Reserved

Bit [1:0]: Reserved (Default 0)

Bit [2]: Force untagout (Default 0)
0 Disable
1 Force untag output
All packets transmitted from this port are untagged. This register is used when this port is connected to legacy equipment that does not support VLAN tagging.

Bit [5:3]: Fixed Transmit priority. Used when bit[7] = 1 **(Default 0)**
000 Transmit Priority Level 0 (Lowest)
001 Transmit Priority Level 1
010 Transmit Priority Level 2
011 Transmit Priority Level 3
100 Transmit Priority Level 4
101 Transmit Priority Level 5
110 Transmit Priority Level 6
111 Transmit Priority Level 7 (Highest)

Bit [6]: Fixed Discard priority **(Default 0)**
0 – Discard Priority Level 0 (Lowest)
1 – Discard Priority Level 7(Highest)

Bit [7]: Enable Fix Priority **(Default 0)**
0 Disable fix priority. All frames are analyzed. Transmit Priority and Drop Priority are based on VLAN Tag, TOS or Logical Port.
1 Transmit Priority and Discard Priority are based on values programmed in bit [6:3]

Port VLAN Map

PVMAP00_0,3 I^2C Address h14,17; Serial Interface Address:h102,105)

PVMAP01_0,3 I^2C Address h18,1B; Serial Interface Address:h106,109)

PVMAP02_0,3 I^2C Address h1C,1F; Serial Interface Address:h10A, 0D)

PVMAP03_0,3 I^2C Address h20,23; Serial Interface Address:h10E, 111)

PVMAP04_0,3 I^2C Address h24,27; Serial Interface Address:h112, 115)

PVMAP05_0,3 I^2C Address h28,2B; Serial Interface Address:h116, 119)

PVMAP06_0,3 I^2C Address h2C,2F; Serial Interface Address:h11A,11D)

PVMAP07_0,3 I^2C Address h30,33; Serial Interface Address:h11E, 121)

10.3.5 PVMODE

I^2C Address: h038, Serial Interface Address:h126

Accessed by serial interface (R/W)

7	6	5	4	3 ... 0
RO	MP	BPDU	DM	Reserved

Bit [0]: Reserved
Must be '0'

Bit [4]: Disable MAC address 0
0: MAC address 0 is not leaned.
1: MAC address 0 is leaned.

Bit [5]: Force BPDU as multicast frame (**Default 0**)
1: Enable. BPDU frames (frames with destination MAC address in the range of 01-80-C2 00-00-00 through 01-80-C2-00-00-0F) are forwarded as multicast frames.
0: Disable. Drop frames in this range.

Bit [6]: MAC/PORT
0: Single MAC address per system
1: Single MAC address per port

Bit [7]: Reserved

10.4 Group 2 Address - Port Trunking Group

10.4.1 TRUNK0_MODE – Trunk group 0 and 1 mode

I^2C Address: h039, Serial Interface Address:h207

Accessed by serial interface and I^2C (R/W)

Port Selection in unmanaged mode. Trunk group 0 and trunk group 1 are enable accordingly to bit [1:0] when input pin P_D[9] = 0 (external pull down).

7 ... 2	1 ... 0
	Port sel

Bit [1:0]: Port member selection for Trunk 0 and 1 in unmanaged mode (Default 2'b00)
00 – Only trunk group 0 is enable. Port 0 and 1 are used for trunk group0
01 – Only trunk group 0 is enable. Port 0,1 and 2 are used for trunk group0
10 – Only trunk group 0 is enable. Port 0,1,2 and 3 are used for trunk group0
11 – Trunk group 0 and 1 are enable. Port 0, 1 used for trunk group0, and port 2 and 3 are used for trunk group1

10.4.2 TRUNK1_MODE – Trunk group 1 mode (Unmanaged Mode)

I^2C Address h03A; Serial Interface Address:h20E

Accessed by serial interface and I^2C (R/W)

Port Selection in unmanaged mode. Trunk group 2 and Trunk group 3 are enable accordingly to bits [1:0] when input pin P_D[10] = 0 (External pull down).

7 … 2	1 … 0
	Port Select

Bit [1:0]: Port member selection for Trunk 2 and 3 in unmanaged mode
00 – Only trunk group 2 is enable. Port 4 and 5 are used for trunk group2
01 – Only trunk group 2 is enable. Port 4, 5 and 6 are used for trunk group2
10 – Only trunk group 2 is enable. Port 4, 5, 6 and 7 are used for trunk group2
11 – Trunk group 2 and trunk group 3 are enable. Port 4 and used for trunk group2, and port 6 5 are and 7 are used for trunk group3

10.4.3 TX_AGE – Tx Queue Aging timer

I^2C Address: h03B;Serial Interface Address:h312

Accessed by serial interface and I^2C (R/W)

7 … 5	4 … 0
	Tx Queue Agent

Bit[4:0]: Unit of 100ms (Default 8). Disable transmission queue aging if value is zero.

Bit[7:5]: Reserved. (Must be '0')

10.5 Group 4 Address - Search Engine Group

10.5.1 AGETIME_LOW – MAC address aging time Low

I^2C Address: h03C; Serial Interface Address:h400

Accessed by serial interface and I^2C (R/W)

Bit [7:0] Low byte of the MAC address aging timer. (Default 2c)

Mac address aging is enable/disable by boot strap T_D[9].

10.5.2 AGETIME_HIGH –MAC address aging time High

I^2C Address h03D; Serial Interface Address h401

Accessed by serial interface and I^2C (R/W)

Bit [7:0]: High byte of the MAC address aging timer. (Default 00)

Aging time is based on the following equation:

{AGETIME_HIGH,AGETIME_LOW} X (# of MAC entries X100µsec)

Note: the numer of entries= 66K when T_D[5] is pull down (SRAM memory size = 512K) and 34K when T_D[5] is pull up (SRAM memory size = 256K).

10.5.3 SE_OPMODE – Search Engine Operation Mode

Serial Interface Address:h403

Accessed by CPU (R/W)

7	6	5 ... 0
SL	DMS	

Bit [5:0]: Reserved

Bit [6]: Disable MCT speedup aging **(Default 0)**
1 – Disable speedup aging when MCT resource is low.
0 – Enable speedup aging when MCT resource is low.

Bit [7]: Slow Learning **(Default 0)**
1– Enable slow learning. Learning is temporary disabled when search demand is high
0 – Learning is performed independent of search demand

10.6 Group 5 Address - Buffer Control/QOS Group

10.6.1 FCBAT – FCB Aging Timer

I²C Address: h03E; Serial Interface Address:h500

7 ... 0
FCBAT

Bit [7:0]: FCB Aging time. Unit of 1ms. (**Default FF**)
FCBAT define the aging time out interval of FCB handle

10.6.2 QOSC – QOS Control

I²C Address: h03F; Serial Interface Address:h501

Accessed by serial interface and I²C (R/W)

7	6	5	4	3 ... 1	0
Tos-d	Tos-p		VF1c		fb

Bit [0]: QoS frame lost is OK. Priority will be available for flow control enabled source only when this bit is set **(Default 0)**

Bit [4]: Per VLAN (Port based) Multicast Flow Control **(Default 0)**
0 – Disable
1 - Enable

Bit [5]: Reserved

Bit [6]: Select TOS bits for Priority **(Default 0)**
0 – Use TOS [4:2] bits to map the transmit priority
1 – Use TOS [5:3] bits to map the transmit priority

Bit [7]: select TOS bits for Drop **(Default 0)**
0 – Use TOS [4:2] bits to map the drop priority
1 – Use TOS [5:3] bits to map the drop priority

10.6.3 FCR – Flooding Control Register

I^2C Address: h040; Serial Interface Address:h502

Accessed by serial interface and I^2C (R/W)

7	6 – 4	3 – 0
Tos	TimeBase	U2MR

Bit [3:0]: U2MR: Unicast to Multicast Rate. Units in terms of time base defined in bits [6:4]. This is used to limit the amount of flooding traffic. The value in U2MR specifies how many packets are allowed to flood within the time specified by bit [6:4]. To disable this function, program U2MR to 0. (**Default = 4'h8**)

Bit [6:4]: TimeBase**: (Default = 000)**
000 = 10us
001 = 20us
010 = 40us
011 = 80us
100 = 160us
101 = 320us
110 = 640us
111 = 10us, same as 000.

Bit [7]: Select VLAN tag or TOS field (IP packets) to be preferentially picked to map transmit priority and drop priority (**Default = 0**).
0 – Select VLAN tag priority field over TOS field
1 – Select TOS field over VLAN tag priority field

10.6.4 AVPML – VLAN Priority Map

I^2C Address: h041; Serial Interface Address:h503

Accessed by serial interface and I^2C (R/W)

7 – 6	5 – 3	2 – 0
VP2	VP1	VP0

Registers AVPML, AVPMM, and AVPMH allow the eight VLAN priorities to map into eight internal level transmit priorities. Under the internal transmit priority, ìsevenî is the highest priority where as ìzeroî is the lowest. This feature allows the user the flexibility of redefining the VLAN priority field. For example, programming a value of 7 into bit 2:0 of the AVPML register would map packet VLAN priority) into internal transmit priority 7. The new priority is used only inside the 2804. When the packet goes out it carries the original priority.

Bit [2:0]: Mapped priority of 0 **(Default 000)**

Bit [5:3]: Mapped priority of 1 **(Default 001)**

Bit [7:6]: Mapped priority of 2 **(Default 10)**

10.6.5 AVPMM – VLAN Priority Map

I^2C Address: h042, Serial Interface Address:h504

Accessed by serial interface and I^2C (R/W)

7	6 4	3 1	0
VP5	VP4	VP3	VP2

Map VLAN priority into eight level transmit priorities:

Bit [0]: Mapped priority of 2 **(Default 0)**

Bit [3:1]: Mapped priority of 3 **(Default 011)**

Bit [6:4]: Mapped priority of 4 **(Default 100)**

Bit [7]: Mapped priority of 5 **(Default 1)**

10.6.6 AVPMH – VLAN Priority Map

I^2C Address: h043, Serial Interface Address:h505

Accessed by serial interface and I^2C (R/W)

7 5	4 2	1 0
VP7	VP6	VP5

Map VLAN priority into eight level transmit priorities:

Bit [1:0]: Mapped priority of 5 **(Default 10)**

Bit [4:2]: Mapped priority of 6 **(Default 110)**

Bit [7:5]: Mapped priority of 7 **(Default 111)**

10.6.7 OSPML – TOS Priority Map

I^2C Address: h044, Serial Interface Address:h506

Accessed by serial interface and I^2C (R/W)

7 6	5 3	2 0
TP2	TP1	TP0

Map TOS field in IP packet into four level transmit priorities

Bit [2:0]: Mapped priority when TOS is 0 **(Default 000)**

Bit [5:3]: Mapped priority when TOS is 1 **(Default 001)**

Bit [7:6]: Mapped priority when TOS is 2 **(Default 10)**

10.6.8 TOSPMM – TOS Priority Map

I^2C Address: h045, Serial Interface Address:h507

Accessed by serial interface and I^2C (R/W)

7	6 4	3 1	0
TP5	TP4	TP3	TP2

Map TOS field in IP packet into four level transmit priorities

Bit [0]: Mapped priority when TOS is 2 **(Default 0)**

Bit [3:1]: Mapped priority when TOS is 3 **(Default 011)**

Bit [6:4]: Mapped priority when TOS is 4 **(Default 100)**

Bit [7]: Mapped priority when TOS is 5 **(Default 1)**

10.6.9 TOSPMH – TOS Priority Map

I^2C Address: h046, Serial Interface Address:h508

Accessed by serial interface and I^2C (R/W)

7 5	4 2	1 0
TP7	TP6	TP5

Map TOS field in IP packet into four level transmit priorities:

Bit [1:0]: Mapped priority when TOS is 5 **(Default 01)**

Bit [4:2]: Mapped priority when TOS is 6 **(Default 110)**

Bit [7:5]: Mapped priority when TOS is 7 **(Default 111)**

10.6.10 AVDM – VLAN Discard Map

I^2C Address: h047, Serial Interface Address:h509

Accessed by serial interface and I^2C (R/W)

7	6	5	4	3	2	1	0
FDV7	FDV6	FDV5	FDV4	FDV3	FDV2	FDV1	FDV0

Map VLAN priority into frame discard when low priority buffer usage is above threshold. Frames with high discard (drop) priority will be discarded (dropped) before frames with low drop priority.

- 0 – Low discard priority
- 1 – High discard priority

Bit [0]: Frame discard priority for frames with VLAN transmit priority 0 **(Default 0)**

Bit [1]: Frame discard priority for frames with VLAN transmit priority 1 **(Default 0)**

Bit [2]: Frame discard priority for frames with VLAN transmit priority 2 **(Default 0)**

Bit [3]: Frame discard priority for frames with VLAN transmit priority 3 **(Default 0)**

Bit [4]: Frame discard priority for frames with VLAN transmit priority 4 **(Default 0)**

Bit [5]: Frame discard priority for frames with VLAN transmit priority 5 **(Default 0)**

Bit [6]: Frame discard priority for frames with VLAN transmit priority 6 **(Default 0)**

Bit [7]: Frame discard priority for frames with VLAN transmit priority 7 **(Default 0)**

10.6.11 TOSDML – TOS Discard Map

I^2C Address: h048, Serial Interface Address:h50A

Accessed by serial interface and I^2C (R/W)

7	6	5	4	3	2	1	0
FDT7	FDT6	FDT5	FDT4	FDT3	FDT2	FDT1	FDT0

Map TOS into frame discard when low priority buffer usage is above threshold

Bit [0]: Frame discard priority for frames with TOS transmit priority 0 **(Default 0)**

Bit [1]: Frame discard priority for frames with TOS transmit priority 1 **(Default 0)**

Bit [2]: Frame discard priority for frames with TOS transmit priority 2 **(Default 0)**

Bit [3]: Frame discard priority for frames with TOS transmit priority 3 **(Default 0)**

Bit [4]: Frame discard priority for frames with TOS transmit priority 4 **(Default 0)**

Bit [5]: Frame discard priority for frames with TOS transmit priority 5 **(Default 0)**

Bit [6]: Frame discard priority for frames with TOS transmit priority 6 **(Default 0)**

Bit [7]: Frame discard priority for frames with TOS transmit priority 7 **(Default 0)**

10.6.12 BMRC - Broadcast/Multicast Rate Control

I^2C Address: h049, Serial Interface Address:h50B

Accessed by serial interface and I^2C (R/W)

7 4	3 0
Broadcast Rate	Multicast Rate

This broadcast and multicast rate defines for each port the number of incoming packet allowed to be forwarded within a specified time. Once the packet rate is reached, packets will be dropped. To turn off the rate limit, program the field to 0.

Bit [3:0] : Multicast Rate Control Number of multicast packets allowed within the time defined in bits 6 to 4 of the Flooding Control Register (FCR). **(Default 0)**.

Bit [7:4] : Broadcast Rate Control Number of broadcast packets allowed within the time defined in bits 6 to 4 of the Flooding Control Register (FCR). **(Default 0)**

10.6.13 UCC – Unicast Congestion Control

I^2C Address: h04A, Serial Interface Address: h50C

Accessed by serial interface and I^2C (R/W)

7 0
Unicast congest threshold

Bit [7:0] : Number of frame count. Used for best effort dropping at B% when destination port's best effort queue reaches UCC threshold and shared pool is all in use. Granularity 16 frame. (Default: h07)

10.6.14 MCC – Multicast Congestion Control

I^2C Address: h0B7, Serial Interface Address: h50D

Accessed by serial interface and I^2C (R/W)

7 5	4	3 0
FC reaction prd		Multicast congest threshold

Bit [3:0]: In multiples of two. Used for triggering MC flow control when destination port's best effort queue reaches MCC threshold. (Default 5'h08)

Bit [4]: Must be 0

Bit [7:5]: Flow control reaction period. ([7:5] *4)+3 usec (Default 3'h2).

10.6.15 PRG – Port Reservation for Giga ports

I^{2}C Address: h0B9, Serial Interface Address h50F

Accessed by serial interface and I^{2}C (R/W)

7 — 4	3 — 0
Buffer low thd	Per source buffer Reservation

Bit [3:0]: Per source buffer reservation. Define the space in the FDB reserved for each port. Expressed in multiples of 16 packets. For each packet 1536 bytes are reserved in the memory.
Default: 4'hA for 4MB memory
4'h6 for 2MB memory
4'h3 for 1MB memory

Bits [7:4]: Expressed in multiples of 16 packets. Threshold for dropping all best effort frames when destination port best effort queues reach UCC threshold and shared pool is all used and source port reservation is at or below the PRG[7:4] level. Also the threshold for initiating UC flow control.
Default: 4'h6 for 4MB memory
4'h2 for 2MB memory
4'h1 for 1MB memory

FCB Reservation

10.6.16 SFCB – Share FCB Size

I^{2}C Address: h04E, Serial Interface Address h510

Accessed by serial interface and I^{2}C (R/W)

7 — 0
Shared buffer size

Bits [7:0]: Expressed in multiples of 8. Buffer reservation for shared pool.
(Default 4G & 4M = 8'd62)
(Default 4G & 2M = 8'd20)
(Default 4G & 1M = 8'd08)
(Default 8G & 4M = 8'd150)
(Default 8G & 2M = 8'd55)
(Default 8G & 1M = 8'd25)

10.6.17 C2RS – Class 2 Reserved Size

I^2C Address: h04F, Serial Interface Address h511

Accessed by serial interface and I^2C (R/W)

7	0
Class 2 FCB Reservation	

Bits [7:0]: Buffer reservation for class 2 (third lowest priority). Granularity 2. **(Default 8'h00)**

10.6.18 C3RS – Class 3 Reserved Size

I^2C Address: h050, Serial Interface Address h512

Accessed by serial interface and I^2C (R/W)

7	0
Class 3 FCB Reservation	

Bits [7:0]: Buffer reservation for class 3. Granularity 2. **(Default 8'h00)**

10.6.19 C4RS – Class 4 Reserved Size

I^2C Address: h051, Serial Interface Address h513

Accessed by serial interface and I^2C (R/W)

7	0
Class 4 FCB Reservation	

Bits [7:0]: Buffer reservation for class 4. Granularity 2. **(Default 8'h00)**

10.6.20 C5RS – Class 5 Reserved Size

I^2C Address: h052; Serial Interface Address: h514

Accessed by serial interface and I^2C (R/W)

7	0
Class 5 FCB Reservation	

Bits [7:0]: Buffer reservation for class 5. Granularity 2. **(Default 8'h00)**

10.6.21 C6RS – Class 6 Reserved Size

I^{2}C Address: h053; Serial Interface Address: h515

Accessed by serial interface and I^{2}C (R/W)

7	0
Class 6 FCB Reservation	

Bits [7:0]: Buffer reservation for class 6 (second highest priority). Granularity 2. **(Default 8'h00)**

10.6.22 C7RS – Class 7 Reserved Size

I^{2}C Address: h054; Serial Interface Address: h516

Accessed by serial interface and I^{2}C (R/W)

7	0
Class 7 FCB Reservation	

Bits [7:0]: Buffer reservation for class 7 (highest priority). Granularity 2. **(Default 8'h00)**

Classes Byte Gigabit Port 0

10.6.23 QOSC00 – BYTE_C2_G0

I^{2}C Address: h055, Serial Interface Address: h517

Bits [7:0]: Byte count threshold for C2 queue WRED **(Default 8'h28)**
(1024byte/unit when Delay Bound is used)
(1024byte/unit when WFQ is used)

10.6.24 QOSC01 – BYTE_C3_G0

I^{2}C Address: h056, Serial Interface Address: h518

Bits [7:0]: Byte count threshold for C3 queue WRED **(Default 8'h28)**
512byte/unit when Delay Bound is used)
(1024byte/unit when WFQ is used)

10.6.25 QOSC02 – BYTE_C4_G0

I^{2}C Address: h057, Serial Interface Address: h519

Bits [7:0]: Byte count threshold for C4 queue WRED **(Default 8'h28)**
(256byte/unit when Delay Bound is used)
(1024byte/unit when WFQ is used)

10.6.26 QOSC03 – BYTE_C5_G0

I^{2}C Address: h058, Serial Interface Address: h51A

Bits [7:0]: Byte count threshold for C5 queue WRED **(Default 8'h28)**
(128byte/unit when Delay Bound is used)
(1024byte/unit when WFQ is used)

10.6.27 QOSC04 – BYTE_C6_G0

I^{2}C Address: h059, Serial Interface Address: h51B

Bits [7:0]: Byte count threshold for C6 queue WRED **(Default 8'h50)**
(64byte/unit when Delay Bound is used)
(1024byte/unit when WFQ is used)

10.6.28 QOSC05 – BYTE_C7_G0

I^{2}C Address: h05A, Serial Interface Address: h51C

Bits [7:0]: Byte count threshold for C6 queue WRED **(Default 8'h50)**
(64byte/unit when Delay Bound is used)
(1024byte/unit when WFQ is used)

QOSC00 through QOSC05 represent the values F-A in Table 3 for Gigabit port 0. They are per-queue byte thresholds for weighted random early drop (WRED). QOSC05 represents A, and QOSC00 represents F.

Classes Byte Gigabit Port 1

10.6.29 QOSC06 – BYTE_C2_G1

I^{2}C Address: h05B, Serial Interface Address: h51D

Bits [7:0]: Byte count threshold for C2 queue WRED **(Default 8'h28)**
(1024byte/unit when Delay Bound is used)
(1024byte/unit when WFQ is used)

10.6.30 QOSC07 – BYTE_C3_G1

I^{2}C Address: h05C, Serial Interface Address: h51E

Bits [7:0] Byte count threshold for C3 queue WRED **(Default 8'h28)**
(512 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.31 QOSC08 – BYTE_C4_G1

I^2C Address: h05D, Serial Interface Address: h51F

Bits [7:0]: Byte count threshold for C4 queue WRED **(Default 8'h28)**
(256 byte/unit when Delay Bound is used)
(1024byte/unit when WFQ is used)

10.6.32 QOSC09 – BYTE_C5_G1

I^2C Address: h05E, Serial Interface Address: h520

Bits [7:0]: Byte count threshold for C5 queue WRED **(Default 8'h28)**
(128 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.33 QOSC0A – BYTE_C6_G1

I^2C Address: h05F, Serial Interface Address: h521

Bits [7:0]: Byte count threshold for C6 queue WRED **(Default 8'h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.34 QOSC0B – BYTE_C7_G1

I^2C Address: h060, Serial Interface Address: h522

Bits [7:0]: Byte count threshold for C7 queue WRED **(Default 8'h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

QOSC06 through QOSC0B represent the values F-A in Table 3. They are per-queue byte thresholds for random early drop. QOSC0B represents A, and QOSC06 represents F.

Classes Byte Gigabit Port 2

10.6.35 QOSC0C – BYTE_C2_G2

I^2C Address: h061, Serial Interface Address: h523

Bits [7:0]: Byte count threshold for C2 queue WRED **(Default 8'h28)**
(1024 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.36 QOSC0D – BYTE_C3_G2

I^2C Address: h062, Serial Interface Address: h524

Bits [7:0]: Byte count threshold for C3 queue WRED **(Default 8’h28)**
(512 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.37 QOSC0E – BYTE_C4_G2

I^2C Address: h063, Serial Interface Address: h525

Bits [7:0]: Byte count threshold for C4 queue WRED **(Default 8’h28)**
(256 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.38 OSC0F – BYTE_C5_G2

I^2C Address: h064, Serial Interface Address: h526

Bits [7:0]: Byte count threshold for C5 queue WRED **(Default 8’h28)**
(128 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.39 QOSC10 – BYTE_C6_G2

I^2C Address: h065, Serial Interface Address: h27

Bits [7:0]: Byte count threshold for C6 queue WRED **(Default 8’h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.40 QOSC11 – BYTE_C7_G2

I^2C Address: h066, Serial Interface Address: h528

Bits [7:0]: Byte count threshold for C7 queue WRED **(Default 8’h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

QOSC0C through QOSC11 represent the values F-A in Table 3 for Gigabit port 2. They are per-queue byte thresholds for random early drop. QOSC11 represents A, and QOSC0C represents F.

Classes Byte Gigabit Port 3

10.6.41 QOSC12 – BYTE_C2_G3

I^2C Address: h067, Serial Interface Address: h529

Bits [7:0]: Byte count threshold for C2 queue WRED **(Default 8’h28)**
(1024 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.42 QOSC13 – BYTE_C3_G3

I^2C Address: h068, Serial Interface Address: h52A

Bits [7:0]: Byte count threshold for C3 queue WRED **(Default 8’h28)**
(512 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.43 QOSC14 – BYTE_C4_G3

I^2C Address: h069, Serial Interface Address: h52B

Bits [7:0]: Byte count threshold for C4 queue WRED **(Default 8’h28)**
(256 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.44 QOSC15 – BYTE_C5_G3

I^2C Address: h06A, Serial Interface Address: h52C

Bits [7:0]: Byte count threshold for C5 queue WRED **(Default 8’h28)**
(128 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.45 QOSC16 – BYTE_C6_G3

I^2C Address: h06B, Serial Interface Address: h52D

Bits [7:0]: Byte count threshold for C6 queue WRED **(Default 8’h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.46 QOSC17 – BYTE_C7_G3

I^2C Address: h06C, Serial Interface Address: h52E

Bits [7:0]: Byte count threshold for C7 queue WRED **(Default 8'h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

QOSC12 through QOSC17 represent the values F-A in Table 3 for Gigabit port 3. They are per-queue byte thresholds for random early drop. QOSC17 represents A, and QOSC12 represents F.

Classes Byte Gigabit Port 4

10.6.47 QOSC18 – BYTE_C2_G4

I^2C Address: h06D, Serial Interface Address:h 52F

Bits [7:0]: Byte count threshold for C2 queue WRED **(Default 8'h28)**
(1024 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.48 QOSC019 – BYTE_C3_G4

I^2C Address: h06E, Serial Interface Address: h530

Bits [7:0]: Byte count threshold for C3 queue WRED **(Default 8'h28)**
(512 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.49 QOSC1A – BYTE_C4_G4

I^2C Address: h06F, Serial Interface Address: h531

Bits [7:0]: Byte count threshold for C4 queue WRED **(Default 8'h28)**
(256 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.50 QOSC1B – BYTE_C5_G4

I^2C Address: h070, Serial Interface Address: h532

Bits [7:0]: Byte count threshold for C5 queue WRED **(Default 8'h28)**
(128 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.51 QOSC1C – BYTE_C6_G4

I2C Address: h071, Serial Interface Address: h533

Bits [7:0]: Byte count threshold for C6 queue WRED **(Default 8'h28)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.52 QOSC1D– BYTE_C7_G4

I2C Address: h072, Serial Interface Address: h534

Bits [7:0]: Byte count threshold for C7 queue WRED **(Default 8'h28)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

QOSC18 through QOSC1D represent the values F-A in Table 3 for Gigabit port 4. They are per-queue byte thresholds for random early drop. QOSC1D represents A, and QOSC18 represents F.

Classes Byte Gigabit Port 5

10.6.53 QOSC1E– BYTE_C2_G5

I2C Address: h073, Serial Interface Address: h535

Bits [7:0]: Byte count threshold for C2 queue WRED **(Default 8'h28)**
(1024 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.54 QOSC1F – BYTE_C3_G5

I2C Address: h074, Serial Interface Address: h536

Bits [7:0]: Byte count threshold for C3 queue WRED **(Default 8'h28)**
(512 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.55 QOSC20 – BYTE_C4_G5

I2C Address: h075, Serial Interface Address: h537

Bits [7:0]: Byte count threshold for C4 queue WRED **(Default 8'h28)**
(256 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.56 QOSC21 – BYTE_C5_G5

I^{2}C Address: h076, Serial Interface Address: h538

Bits [7:0]: Byte count threshold for C5 queue WRED **(Default 8'h28)**
(128 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.57 QOSC22 – BYTE_C6_G5

I^{2}C Address: h077, Serial Interface Address: h539

Bits [7:0]: Byte count threshold for C6 queue WRED **(Default 8'h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.58 QOSC23 – BYTE_C7_G5

I^{2}C Address: h078, Serial Interface Address: h53A

Bits [7:0]: Byte count threshold for C4 queue WRED **(Default 8'h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

QOSC1E through QOSC23 represent the values F-A in Table 3 for Gigabit port 5. They are per-queue byte thresholds for random early drop. QOSC23 represents A, and QOSC1E represents F.

Classes Byte Gigabit Port 6

10.6.59 QOSC24 – BYTE_C2_G6

I^{2}C Address: h079, Serial Interface Address: h53B

Bits [7:0]: Byte count threshold for C2 queue WRED **(Default 8'h28)**
(1024 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.60 QOSC25 – BYTE_C3_G6

I^{2}C Address: h07A, Serial Interface Address: h53C

Bits [7:0]: Byte count threshold for C3 queue WRED **(Default 8'h28)**
(512 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.61 QOSC26 – BYTE_C4_G6

I^2C Address: h07B, Serial Interface Address: h53D

Bits [7:0]: Byte count threshold for C4 queue WRED **(Default 8'h28)**
(256 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.62 QOSC27 – BYTE_C5_G6

I^2C Address: h07C, Serial Interface Address: h53E

Bits [7:0]: Byte count threshold for C5 queue WRED **(Default 8'h28)**
(128 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.63 QOSC28 – BYTE_C6_G6

I^2C Address: h07D, Serial Interface Address: h53F

Bits [7:0]: Byte count threshold for C6 queue WRED **(Default 8'h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.64 QOSC29 – BYTE_C7_G6

I^2C Address: h07E, Serial Interface Address:h 540

Bits [7:0]: Byte count threshold for C7 queue WRED **(Default 8'h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

QOSC24 through QOSC29 represent the values F-A in Table 3 for Gigabit port 6. They are per-queue byte thresholds for random early drop. QOSC29 represents A, and QOSC24 represents F.

Classes Byte Gigabit Port 7

10.6.65 QOSC2A – BYTE_C2_G7

I^2C Address: h07F, Serial Interface Address: h541

Bits [7:0]: Byte count threshold for C2 queue WRED **(Default 8'h28)**
(1024 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.66 QOSC2B – BYTE_C3_G7

I^{2}C Address: h080, Serial Interface Address: h542

Bits [7:0]: Byte count threshold for C3 queue WRED **(Default 8'h28)**
(512 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.67 QOSC2C – BYTE_C4_G7

I^{2}C Address: h081, Serial Interface Address: h543

Bits [7:0]: Byte count threshold for C4 queue WRED **(Default 8'h28)**
(256 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.68 QOSC2D – BYTE_C5_G7

I^{2}C Address: h082, Serial Interface Address: h544

Bits [7:0]: Byte count threshold for C5 queue WRED **(Default 8'h28)**
(128 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.69 QOSC2E – BYTE_C6_G7

I^{2}C Address: h083, Serial Interface Address: h545

Bits [7:0]: Byte count threshold for C6 queue WRED **(Default 8'h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

10.6.70 QOSC2F – BYTE_C7_G7

I^{2}C Address: h084, Serial Interface Address: h546

Bits [7:0]: Byte count threshold for C5 queue WRED **(Default 8'h50)**
(64 byte/unit when Delay Bound is used)
(1024 byte/unit when WFQ is used)

QOSC00 through QOSC05 represent the values F-A in Table 3 for Gigabit port 7. They are per-queue byte thresholds for random early drop. QOSC05 represents A, and QOSC00 represents F.

Classes Byte Limit CPU

Classes WFQ Credit Set 0

10.6.71 QOSC33 – CREDIT_C0_G0

Serial Interface Address: h54A

Bits [5:0]: W0 - Credit register for WFQ. (Default 6’h04)

Bits [7:6]: Priority type. Define one of the four QoS mode of operation for port 0 (Default 2’00)
00 : Option 1
01: Option 2
10: Option 3
11: Option 4

See table below

Queue	P7	P6	P5	P4	P3	P2	P1	P0
Option 1 Bit [7:6] = 2’B00	DELAY BOUND						BE	
Option 2 Bit [7:6] = 2’B01	SP		DELAY BOUND				BE	
Option 3 Bit [7:6] = 2’B10	SP		WFQ					
Opition 4 Bit [7:6] = 2’B11	WFQ							
Credit for WFQ – Bit [5:0]	W 7	W 6	W 5	W 4	W 3	W 2	W 1	W 0

10.6.72 QOSC34 – CREDIT_C1_G0

Serial Interface Address: h54B

Bits [7]: Flow control allow during WFQ scheme. **(Default 1’b1)**
0 = Not support QoS when the Source port Flow control status is on.
1= Always support QoS)

Bits [6]: Flow control BE Queue only. **(Default 1’b1)**
0= DO NOT send any frames if the XOFF is on.
1= the P7-P2 frames can be sent even the XOFF is ON

Bits [5:0] W1 - Credit register. **(Default 4’h04)**

Fc_allow	Fc_be_only	Lost_ok	
Egress- for dest fc_status		Ingress- for src fc status	
0	0	0	Go to BE Queue if (Src FC or Des FC on) otherwise Normal
0	0	1	Go to BE Queue if (Dest FC on) otherwise Normal
1	0	0	(WFQ only) Go to BE Queue if (Src FC on) otherwise BAD
1	0	1	(WFQ only) Always Normal
X	1	0	Go to BE Queue if (Src FC on)
X	1	1	Always Normal

10.6.73 QOSC35 – CREDIT_C2_G0

Serial Interface Address: h54C

Bits [5:0] W2 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.74 QOSC36 – CREDIT_C3_G0

Serial Interface Address: h54D

Bits [5:0] W3 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.75 QOSC37 – CREDIT_C4_G0

Serial Interface Address: h54E

Bits [5:0] W4 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.76 QOSC38 – CREDIT_C5_G0

Serial Interface Address: h54F

Bits [5:0] W5 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.77 QOSC39– CREDIT_C6_G0

Serial Interface Address: h550

Bits [5:0] W6 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.78 QOSC3A– CREDIT_C7_G0

Serial Interface Address: h551

Bits [5:0] W7 - Credit register. **(Default 5’h10)**

Bits [7:6]: Reserved

QOSC33 through QOSC3Arepresents the set of WFQ parameters (see section 7.5) for Gigabit port 0. The granularity of the numbers (bits [5:0]) is 1, and their sum must be 64. QOSC33 corresponds to W0, and QOSC3A corresponds to W7.

Classes WFQ Credit Port G1

10.6.79 QOSC3B – CREDIT_C0_G1

Serial Interface Address: h552

Bits [5:0]: W0 - Credit register for WFQ. (Default 6’h04)

Bits [7:6]: Priority type. Define one of the four QoS mode of operation for port 1 (Default 2’00)
00 : Option 1
01: Option 2
10: Option 3
11: Option 4

See table below:

Queue	P7	P6	P5	P4	P3	P2	P1	P0
Option 1 Bit [7:6] = 2’B00	DELAY BOUND						BE	
Option 2 Bit [7:6] = 2’B01	SP		DELAY BOUND				BE	
Option 3 Bit [7:6] = 2’B10	SP		WFQ					
Opition 4 Bit [7:6] = 2’B11	WFQ							
Credit for WFQ – Bit [5:0]	W 7	W 6	W 5	W 4	W 3	W 2	W 1	W 0

10.6.80 QOSC3C – CREDIT_C1_G1

Serial Interface Address: h54B

Bits [7]: Flow control allow during WFQ scheme. **(Default 1’b1)**
0 = Not support QoS when the Source port Flow control status is on.
1= Always support QoS)

Bits [6]: Flow control BE Queue only. **(Default 1’b1)**
0= DO NOT send any frames if the XOFF is on.
1= the P7-P2 frames can be sent even the XOFF is ON

Bits [5:0] W1 - Credit register. **(Default 4’h04)**

Fc_allow	Fc_be_only	Lost_ok	
Egress- for dest fc_status		Ingress- for src fc status	
0	0	0	Go to BE Queue if (Src FC or Des FC on) otherwise Normal
0	0	1	Go to BE Queue if (Dest FC on) otherwise Normal
1	0	0	(WFQ only) Go to BE Queue if (Src FC on) otherwise BAD
1	0	1	(WFQ only) Always Normal
X	1	0	Go to BE Queue if (Src FC on)
X	1	1	Always Normal

10.6.81 QOSC3D – CREDIT_C2_G1

Serial Interface Address: h553

Bits [5:0] W2 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.82 QOSC3E – CREDIT_C3_G1

Serial Interface Address: h554

Bits [5:0] W3 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.83 QOSC3F – CREDIT_C4_G1

Serial Interface Address: h555

Bits [5:0] W4 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.84 QOSC40 – CREDIT_C5_G1

Serial Interface Address: h556

Bits [5:0] W5 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.85 QOSC41– CREDIT_C6_G1

Serial Interface Address: h557

Bits [5:0] W6 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.86 QOSC42– CREDIT_C7_G1

Serial Interface Address: h558

Bits [5:0] W7 - Credit register. **(Default 5’h10)**

Bits [7:6]: Reserved

QOSC3B through QOSC42 represents the set of WFQ parameters (see section 7.5) for Gigabit port 1. The granularity of the numbers (bits [5:0]) is 1, and their sum must be 64. QOSC3B corresponds to W0, and QOSC42 corresponds to W7.

Classes WFQ Credit Port G2

10.6.87 QOSC43 – CREDIT_C0_G2

Serial Interface Address: h55A

Bits [5:0]: W0 - Credit register for WFQ. (Default 6’h04)

Bits [7:6]: Priority type. Define one of the four QoS mode of operation for port 2 (Default 2’00)
00 : Option 1
01: Option 2
10: Option 3
11: Option 4

See table below:

Queue	P7	P6	P5	P4	P3	P2	P1	P0
Option 1 Bit [7:6] = 2'B00	DELAY BOUND						BE	
Option 2 Bit [7:6] = 2'B01	SP		DELAY BOUND				BE	
Option 3 Bit [7:6] = 2'B10	SP		WFQ					
Opition 4 Bit [7:6] = 2'B11	WFQ							
Credit for WFQ – Bit [5:0]	W 7	W 6	W 5	W 4	W 3	W 2	W 1	W 0

10.6.88 QOSC44 – CREDIT_C1_G2

Serial Interface Address: h55B

Bits [7]: Flow control allow during WFQ scheme. **(Default 1'b1)**
0 = Not support QoS when the Source port Flow control status is on.
1= Always support QoS)

Bits [6]: Flow control BE Queue only. (Default 1'b1)
0= DO NOT send any frames if the XOFF is on.
1= the P7-P2 frames can be sent even the XOFF is ON

Bits [5:0] W1 - Credit register. (Default 4'h04)

Fc_allow	Fc_be_only	Lost_ok	
Egress- for dest fc_status		Ingress- for src fc status	
0	0	0	Go to BE Queue if (Src FC or Des FC on) otherwise Normal
0	0	1	Go to BE Queue if (Dest FC on) otherwise Normal
1	0	0	(WFQ only) Go to BE Queue if (Src FC on) otherwise BAD
1	0	1	(WFQ only) Always Normal
X	1	0	Go to BE Queue if (Src FC on)
X	1	1	Always Normal

10.6.89 QOSC45 – CREDIT_C2_G2

Serial Interface Address: h55C

Bits [5:0] W2 - Credit register. **(Default 4'h04)**

Bits [7:6]: Reserved

10.6.90 QOSC46 – CREDIT_C3_G2

Serial Interface Address: h55D

Bits [5:0] W3 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.91 QOSC47 – CREDIT_C4_G2

Serial Interface Address: h55E

Bits [5:0] W4 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.92 QOSC48 – CREDIT_C5_G2

Serial Interface Address: h55F

Bits [5:0] W5 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.93 QOSC49– CREDIT_C6_G2

Serial Interface Address: h560

Bits [5:0] W6 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.94 QOSC4A– CREDIT_C7_G2

Serial Interface Address: h561

Bits [5:0] W7 - Credit register. **(Default 5’h10)**

Bits [7:6]: Reserved

QOSC43 through QOSC4Arepresents the set of WFQ parameters (see section 7.5) for Gigabit port 2. The granularity of the numbers (bits [5:0]) is 1, and their sum must be 64. QOSC43 corresponds to W0, and QOSC4A corresponds to W7.

Classes WFQ Credit Port G3

10.6.95 QOSC4B – CREDIT_C0_G3

Serial Interface Address: h562

Bits [5:0]: W0 - Credit register for WFQ. (Default 6’h04)

Bits [7:6]: Priority type. Define one of the four QoS mode of operation for port 3 (Default 2’00)
00 : Option 1
01: Option 2
10: Option 3
11: Option 4

See table below:

Queue	P7	P6	P5	P4	P3	P2	P1	P0
Option 1 Bit [7:6] = 2’B00	DELAY BOUND						BE	
Option 2 Bit [7:6] = 2’B01	SP		DELAY BOUND				BE	
Option 3 Bit [7:6] = 2’B10	SP		WFQ					
Opition 4 Bit [7:6] = 2’B11	WFQ							
Credit for WFQ – Bit [5:0]	W7	W6	W5	W4	W3	W2	W1	W0

10.6.96 QOSC4 – CREDIT_C1_G3

Serial Interface Address: h563

Bits [7]: Flow control allow during WFQ scheme. **(Default 1’b1)**
0 = Not support QoS when the Source port Flow control status is on.
1= Always support QoS)

Bits [6]: Flow control BE Queue only. **(Default 1’b1)**
(0= DO NOT send any frames if the XOFF is on.
(1= the P7-P2 frames can be sent even the XOFF is ON)

Bits [5:0] W1 - Credit register. **(Default 4’h04)**

Fc_allow	Fc_be_only	Lost_ok	
Egress- for dest fc_status		Ingress- for src fc status	
0	0	0	Go to BE Queue if (Src FC or Des FC on) otherwise Normal
0	0	1	Go to BE Queue if (Dest FC on) otherwise Normal
1	0	0	(WFQ only) Go to BE Queue if (Src FC on) otherwise BAD
1	0	1	(WFQ only) Always Normal
X	1	0	Go to BE Queue if (Src FC on)
X	1	1	Always Normal

10.6.97 QOSC4D – CREDIT_C2_G3

Serial Interface Address: h564

Bits [5:0] W2 - Credit register. **(Default 4'h04)**

Bits [7:6]: Reserved

10.6.98 QOSC4E – CREDIT_C3_G3

Serial Interface Address: h565

Bits [5:0] W3 - Credit register. **(Default 4'h04)**

Bits [7:6]: Reserved

10.6.99 QOSC4F – CREDIT_C4_G3

Serial Interface Address: h566

Bits [5:0] W4 - Credit register. **(Default 4'h04)**

Bits [7:6]: Reserved

10.6.100 QOSC50 – CREDIT_C5_G3

Serial Interface Address: h567

Bits [5:0] W5 - Credit register. **(Default 5'h8)**

Bits [7:6]: Reserved

10.6.101 QOSC51– CREDIT_C6_G3

Serial Interface Address: h568

Bits [5:0] W6 - Credit register. **(Default 5'h8)**

Bits [7:6]: Reserved

10.6.102 QOSC52– CREDIT_C7_G3

Serial Interface Address: h569

Bits [5:0] W7 - Credit register. **(Default 5'h10)**

Bits [7:6]: Reserved

QOSC4B through QOSC52 represents the set of WFQ parameters (see section 7.5) for Gigabit port 3. The granularity of the numbers (bits [5:0]) is 1, and their sum must be 64. QOSC4B corresponds to W0, and QOSC52 corresponds to W7.

Classes WFQ Credit Port G4

10.6.103 QOSC53 – CREDIT_C0_G4

Serial Interface Address: h56A

Bits [5:0]: W0 - Credit register for WFQ. (Default 6'h04)

Bits [7:6]: Priority type. Define one of the four QoS mode of operation for port 4 (Default 2'00)
00 : Option 1
01: Option 2
10: Option 3
11: Option 4

See table below:

Queue	P7	P6	P5	P4	P3	P2	P1	P0
Option 1 Bit [7:6] = 2'B00	DELAY BOUND						BE	
Option 2 Bit [7:6] = 2'B01	SP		DELAY BOUND				BE	
Option 3 Bit [7:6] = 2'B10	SP		WFQ					
Opition 4 Bit [7:6] = 2'B11	WFQ							
Credit for WFQ – Bit [5:0]	W 7	W 6	W 5	W 4	W 3	W 2	W 1	W 0

10.6.104 QOSC54 – CREDIT_C1_G4

Serial Interface Address: h56B

Bits [7]: Flow control allow during WFQ scheme. **(Default 1'b1)**
0 = Not support QoS when the Source port Flow control status is on.
1= Always support QoS)

Bits [6]: Flow control BE Queue only. **(Default 1'b1)**
(0= DO NOT send any frames if the XOFF is on.
(1= the P7-P2 frames can be sent even the XOFF is ON)

Bits [5:0] W1 -Credit register. **(Default 4'h04)**

Fc_allow	Fc_be_only	Lost_ok	
Egress- for dest fc_status		Ingress- for src fc status	
0	0	0	Go to BE Queue if (Src FC or Des FC on) otherwise Normal
0	0	1	Go to BE Queue if (Dest FC on) otherwise Normal
1	0	0	(WFQ only) Go to BE Queue if (Src FC on) otherwise BAD
1	0	1	(WFQ only) Always Normal
X	1	0	Go to BE Queue if (Src FC on)
X	1	1	Always Normal

10.6.105 QOSC55 – CREDIT_C2_G4

Serial Interface Address: h56C

Bits [5:0] W2 - Credit register. **(Default 4'h04)**

Bits [7:6]: Reserved

10.6.106 QOSC56 – CREDIT_C3_G4

Serial Interface Address: h56D

Bits [5:0] W3 - Credit register. **(Default 4'h04)**

Bits [7:6]: Reserved

10.6.107 QOSC57 – CREDIT_C4_G4

Serial Interface Address: h56E

Bits [5:0] W4 - Credit register. **(Default 4'h04)**

Bits [7:6]: Reserved

10.6.108 QOSC58 – CREDIT_C5_G4

Serial Interface Address: h56F

Bits [5:0] W5 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.109 QOSC59– CREDIT_C6_G4

Serial Interface Address: h570

Bits [5:0] W6 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.110 QOSC5A– CREDIT_C7_G4

Serial Interface Address: h571

Bits [5:0] W7 - Credit register. **(Default 5’h10)**

Bits [7:6]: Reserved

QOSC53 through QOSC5A represents the set of WFQ parameters (see section 7.5) for Gigabit port 4. The granularity of the numbers (bits [5:0]) is 1, and their sum must be 64. QOSC53 corresponds to W0, and QOSC5A corresponds to W7.

Classes WFQ Credit Port G5

10.6.111 QOSC5B – CREDIT_C0_G5

Serial Interface Address: h572

Bits [5:0]: W0 - Credit register for WFQ. (Default 6’h04)

Bits [7:6]: Priority type. Define one of the four QoS mode of operation for port 5 (Default 2’00)
00 : Option 1
01: Option 2
10: Option 3
11: Option 4

See table below:

Queue	P7	P6	P5	P4	P3	P2	P1	P0
Option 1 Bit [7:6] = 2’B00	DELAY BOUND						BE	
Option 2 Bit [7:6] = 2’B01	SP		DELAY BOUND				BE	
Option 3 Bit [7:6] = 2’B10	SP		WFQ					
Opition 4 Bit [7:6] = 2’B11	WFQ							
Credit for WFQ – Bit [5:0]	W 7	W 6	W 5	W 4	W 3	W 2	W 1	W 0

10.6.112 QOSC5C – CREDIT_C1_G5

Serial Interface Address: h573

Bits [7]: Flow control allow during WFQ scheme. **(Default 1’b1)**
0 = Not support QoS when the Source port Flow control status is on.
1= Always support QoS)

Bits [6]: Flow control BE Queue only. **(Default 1’b1)**
(0= DO NOT send any frames if the XOFF is on.
(1= the P7-P2 frames can be sent even the XOFF is ON)

Bits [5:0] W1 - Credit register. **(Default 4’h04)**

Fc_allow	Fc_be_only	Lost_ok	
Egress- for dest fc_status		Ingress- for src fc status	
0	0	0	Go to BE Queue if (Src FC or Des FC on) otherwise Normal
0	0	1	Go to BE Queue if (Dest FC on) otherwise Normal
1	0	0	(WFQ only) Go to BE Queue if (Src FC on) otherwise BAD
1	0	1	(WFQ only) Always Normal
X	1	0	Go to BE Queue if (Src FC on)
X	1	1	Always Normal

10.6.113 QOSC5D – CREDIT_C2_G5

Serial Interface Address: h574

Bits [5:0] W2 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.114 QOSC5E – CREDIT_C3_G5

Serial Interface Address: h575

Bits [5:0] W3 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.115 QOSC5F – CREDIT_C4_G5

Serial Interface Address: h576

Bits [5:0] W4 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.116 QOSC60 – CREDIT_C5_G5

Serial Interface Address: h577

Bits [5:0] W5 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.117 QOSC61– CREDIT_C6_G5

Serial Interface Address: h578

Bits [5:0] W6 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.118 QOSC62– CREDIT_C7_G5

Serial Interface Address: h579

Bits [5:0] W7 - Credit register. **(Default 5’h10)**

Bits [7:6]: Reserved

QOSC5B through QOSC62 represents the set of WFQ parameters (see section 7.5) for Gigabit port 5. The granularity of the numbers (bits [5:0]) is 1, and their sum must be 64. QOSC5B corresponds to W0, and QOSC62 corresponds to W7.

Classes WFQ Credit Port G6

10.6.119 QOSC63 – CREDIT_C0_G6

Serial Interface Address: h57A

Bits [5:0]: W0 - Credit register for WFQ. (Default 6’h04)

Bits [7:6]: Priority type. Define one of the four QoS mode of operation for port 6 (Default 2’00)
00 : Option 1
01: Option 2
10: Option 3
11: Option 4

See table below:

Queue	P7	P6	P5	P4	P3	P2	P1	P0
Option 1 Bit [7:6] = 2’B00	DELAY BOUND						BE	
Option 2 Bit [7:6] = 2’B01	SP		DELAY BOUND				BE	
Option 3 Bit [7:6] = 2’B10	SP		WFQ					
Opition 4 Bit [7:6] = 2’B11	WFQ							
Credit for WFQ – Bit [5:0]	W 7	W 6	W 5	W 4	W 3	W 2	W 1	W 0

10.6.120 QOSC64 – CREDIT_C1_G6

Serial Interface Address: h57B

Bits [7]: Flow control allow during WFQ scheme. **(Default 1’b1)**
0 = Not support QoS when the Source port Flow control status is on.
1= Always support QoS)

Bits [6]: Flow control BE Queue only. **(Default 1’b1)**
(0= DO NOT send any frames if the XOFF is on.
(1= the P7-P2 frames can be sent even the XOFF is ON)

Bits [5:0] W1 - Credit register. **(Default 4’h04)**

Fc_allow	Fc_be_only	Lost_ok	
Egress- for dest fc_status		Ingress- for src fc status	
0	0	0	Go to BE Queue if (Src FC or Des FC on) otherwise Normal
0	0	1	Go to BE Queue if (Dest FC on) otherwise Normal
1	0	0	(WFQ only) Go to BE Queue if (Src FC on) otherwise BAD
1	0	1	(WFQ only) Always Normal
X	1	0	Go to BE Queue if (Src FC on)
X	1	1	Always Normal

10.6.121 QOSC65 – CREDIT_C2_G6

Serial Interface Address: h57C

Bits [5:0] W2 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.122 QOSC66 – CREDIT_C3_G6

Serial Interface Address: h57D

Bits [5:0] W3 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.123 QOSC67 – CREDIT_C4_G6

Serial Interface Address: h57E

Bits [5:0] W4 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.124 QOSC68 – CREDIT_C5_G6

Serial Interface Address: h57F

Bits [5:0] W5 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.125 QOSC69– CREDIT_C6_G6

Serial Interface Address: h580

Bits [5:0] W6 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.126 QOSC6A– CREDIT_C7_G6

Serial Interface Address: h581

Bits [5:0] W7 - Credit register. **(Default 5’h10)**

Bits [7:6]: Reserved

QOSC63 through QOSC6A represents the set of WFQ parameters (see section 7.5) for Gigabit port 6. The granularity of the numbers (bits [5:0]) is 1, and their sum must be 64. QOSC63 corresponds to W0, and QOSC6A corresponds to W7.

Classes WFQ Credit Port G7

10.6.127 QOSC6B – CREDIT_C0_G7

Serial Interface Address: h582

Bits [5:0]: W0 - Credit register for WFQ. (Default 6’h04)

Bits [7:6]: Priority type. Define one of the four QoS mode of operation for port 7 (Default 2’00)
00 : Option 1
01: Option 2
10: Option 3
11: Option 4

Queue	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
Option 1 Bit [7:6] = 2'B00	DELAY BOUND						BE	
Option 2 Bit [7:6] = 2'B01	SP		DELAY BOUND				BE	
Option 3 Bit [7:6] = 2'B10	SP		WFQ					
Opition 4 Bit [7:6] = 2'B11	WFQ							
Credit for WFQ – Bit [5:0]	W 7	W 6	W 5	W 4	W 3	W 2	W 1	W 0

10.6.128 QOSC6C – CREDIT_C1_G7

Serial Interface Address: h583

Bits [7]: Flow control allow during WFQ scheme. **(Default 1'b1)**
0 = Not support QoS when the Source port Flow control status is on.
1= Always support QoS)

Bits [6]: Flow control BE Queue only. **(Default 1'b1)**
(0= DO NOT send any frames if the XOFF is on.
(1= the P7-P2 frames can be sent even the XOFF is ON)

Bits [5:0] W1 - Credit register. **(Default 4'h04)**

Fc_allow	Fc_be_only	Lost_ok	
Egress- for dest fc_status		Ingress- for src fc status	
0	0	0	Go to BE Queue if (Src FC or Des FC on) otherwise Normal
0	0	1	Go to BE Queue if (Dest FC on) otherwise Normal
1	0	0	(WFQ only) Go to BE Queue if (Src FC on) otherwise BAD
1	0	1	(WFQ only) Always Normal
X	1	0	Go to BE Queue if (Src FC on)
X	1	1	Always Normal

10.6.129 QOSC6D – CREDIT_C2_G7

Serial Interface Address: h584

Bits [5:0] W2 - Credit register. **(Default 4'h04)**

Bits [7:6]: Reserved

10.6.130 QOSC6E – CREDIT_C3_G7

Serial Interface Address: h585

Bits [5:0] W3 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.131 QOSC6F – CREDIT_C4_G7

Serial Interface Address: h586

Bits [5:0] W4 - Credit register. **(Default 4’h04)**

Bits [7:6]: Reserved

10.6.132 QOSC70 – CREDIT_C5_G7

Serial Interface Address: h587

Bits [5:0] W5 - Credit register. **(Default 5’h8)**

Bits [7:6]: Reserved

10.6.133 QOSC71– CREDIT_C6_G7

Serial Interface Address: h588

Bits [5:0] W6 - Credit register. **(Default 5’h8)**

10.6.134 QOSC72– CREDIT_C7_G7

Serial Interface Address: h589

Bits [5:0] W7 - Credit register. **(Default 5’h10)**

Bits [7:6]: Reserved

QOSC6B through QOSC72 represents the set of WFQ parameters (see section 7.5) for Gigabit port 7. The granularity of the numbers (bits [5:0]) is 1, and their sum must be 64. QOSC6B corresponds to W0, and QOSC72 corresponds to W7.

Class 6 Shaper Control Port G0

10.6.135 QOSC73 – TOKEN_RATE_G0

Serial Interface Address: h58A

Bits [7:0] Bytes allow to transmit every frame time (0.512usec) when regulated by Shaper logic. **(Default: 8’h08)**

10.6.136 QOSC74 – TOKEN_LIMIT_G0

Serial Interface Address: h58B

Bits [7:0] Bytes allow to continue transmit out when regulated by Shaper logic. (16byte/unit) **(Default: 8'hC0)**

QOSC73 and QOSC74 correspond to parameters from section 7.6 on the shaper for EF traffic. QOSC73 is an integer less than 64, with granularity 1. QOSC74 is the programmed maximum value of the counter (maximum burst size). This value is expressed in multiples of 16. QOSC73 and QOSC74 apply to Gigabit port 0. Register QOSC39-CREDIT_C6_G0 programs the peak rate. See QoS application note for more information.

Class 6 Shaper Control Port G1

10.6.137 QOSC75 – TOKEN_RATE_G1

Serial Interface Address: h58C

Bits [7:0] Bytes allow to transmit every frame time (0.512usec) when regulated by Shaper logic. **(Default: 8'h08)**

10.6.138 QOSC76 – TOKEN_LIMIT_G1

Serial Interface Address: h58D

Bits [7:0] Bytes allow to continue transmit out when regulated by Shaper logic. (16byte/unit) **(Default: 8'hC0)**

QOSC75 and QOSC76 correspond to parameters from section 7.6 on the shaper for EF traffic. QOSC75 is an integer less than 64, with granularity 1. QOSC76 is the programmed maximum value of the counter (maximum burst size). This value is expressed in multiples of 16. QOSC75 and QOSC76 apply to Gigabit port 1. Register QOSC41-CREDIT_C6_G1 programs the peak rate. See QoS application note for more information.

Class 6 Shaper Control Port G2

10.6.139 QOSC77 – TOKEN_RATE_G2

Serial Interface Address: h58E

Bits [7:0] Bytes allow to transmit every frame time (0.512usec) when regulated by Shaper logic. **(Default: 8'h08)**

10.6.140 QOSC78 – TOKEN_LIMIT_G2

Serial Interface Address: h58F

Bits [7:0] Bytes allow to continue transmit out when regulated by Shaper logic. (16byte/unit) **(Default: 8’hC0)**

QOSC77 and QOSC78 correspond to parameters from section 7.6 on the shaper for EF traffic. QOSC77 is an integer less than 64, with granularity 1. QOSC78 is the programmed maximum value of the counter (maximum burst size). This value is expressed in multiples of 16. QOSC77 and QOSC78 apply to Gigabit port 2. Register QOSC49-CREDIT_C6_G2 programs the peak rate. See QoS application note for more information.

Class 6 Shaper Control Port G3

10.6.141 QOSC79 – TOKEN_RATE_G3

Serial Interface Address: h590

Bits [7:0] Bytes allow to transmit every frame time (0.512usec) when regulated by Shaper logic. **(Default: 8’h08)**

10.6.142 QOSC7A – TOKEN_LIMIT_G3

Serial Interface Address: h591

Bits [7:0] Bytes allow to continue transmit out when regulated by Shaper logic. (16byte/unit) **(Default: 8’hC0)**

QOSC79 and QOSC7A correspond to parameters from section 7.6 on the shaper for EF traffic. QOSC79 is an integer less than 64, with granularity 1. QOSC7A is the programmed maximum value of the counter (maximum burst size). This value is expressed in multiples of 16. QOSC79 and QOSC7A apply to Gigabit port 3. Register QOSC51-CREDIT_C6_G3 programs the peak rate. See QoS application note for more information.

Class 6 Shaper Control Port G4

10.6.143 QOSC7B – TOKEN_RATE_G4

Serial Interface Address: h592

Bits [7:0] Bytes allow to transmit every frame time (0.512usec) when regulated by Shaper logic. **(Default: 8’h08)**

10.6.144 QOSC7C – TOKEN_LIMIT_G4

Serial Interface Address: h593

Bits [7:0] Bytes allow to continue transmit out when regulated by Shaper logic. (16byte/unit) **(Default: 8’hC0)**

QOSC7B and QOSC7C correspond to parameters from section 7.6 on the shaper for EF traffic. QOSC7B is an integer less than 64, with granularity 1. QOSC7C is the programmed maximum value of the counter (maximum burst size). This value is expressed in multiples of 16. QOSC7B and QOSC7C apply to Gigabit port 4. Register QOSC59-CREDIT_C6_G4 programs the peak rate. See QoS application note for more information.

Class 6 Shaper Control Port G5

10.6.145 QOSC7D – TOKEN_RATE_G5

Serial Interface Address: h594

Bits [7:0] Bytes allow to transmit every frame time (0.512usec) when regulated by Shaper logic. **(Default: 8’h08)**

10.6.146 QOSC7E – TOKEN_LIMIT_G5

Serial Interface Address: h595

Bits [7:0] Bytes allow to continue transmit out when regulated by Shaper logic. (16byte/unit) **(Default: 8’hC0)**

QOSC7D and QOSC7E correspond to parameters from section 7.6 on the shaper for EF traffic. QOSC7D is an integer less than 64, with granularity 1. QOSC7E is the programmed maximum value of the counter (maximum burst size). This value is expressed in multiples of 16. QOSC7D and QOSC7E apply to Gigabit port 5. Register QOSC60-CREDIT_C6_G5 programs the peak rate. See QoS application note for more information.

Class 6 Shaper Control Port G6

10.6.147 QOSC7F – TOKEN_RATE_G6

Serial Interface Address: h596

Bits [7:0] Bytes allow to transmit every frame time (0.512usec) when regulated by Shaper logic. **(Default: 8’h08)**

10.6.148 QOSC80 – TOKEN_LIMIT_G6

Serial Interface Address: h597

Bits [7:0] Bytes allow to continue transmit out when regulated by Shaper logic. (16byte/unit) **(Default: 8’hC0)**

QOSC7F and QOSC80 correspond to parameters from section 7.6 on the shaper for EF traffic. QOSC7F is an integer less than 64, with granularity 1. QOSC80 is the programmed maximum value of the counter (maximum burst size). This value is expressed in multiples of 16. QOSC7F and QOSC80 apply to Gigabit port 6. Register QOSC69-CREDIT_C6_G6 programs the peak rate. See QoS application note for more information.

Class 6 Shaper Control Port G7

10.6.149 QOSC81 – TOKEN_RATE_G7

Serial Interface Address: h598

Bits [7:0] Bytes allow to transmit every frame time (0.512usec) when regulated by Shaper logic. **(Default: 8'h08)**

10.6.150 QOSC82 – TOKEN_LIMIT_G7

Serial Interface Address: h599

Bits [7:0] Bytes allow to continue transmit out when regulated by Shaper logic. (16byte/unit) **(Default: 8'hC0)**

QOSC81 and QOSC82 correspond to parameters from section 7.6 on the shaper for EF traffic. QOSC81 is an integer less than 64, with granularity 1. QOSC82 is the programmed maximum value of the counter (maximum burst size). This value is expressed in multiples of 16. QOSC81 and QOSC82 apply to Gigabit port 7. Register QOSC6F-CREDIT_C6_G7 programs the peak rate. See QoS application note for more information

10.6.151 RDRC0 – WRED Rate Control 0

I^2C Address: h085, Serial Interface Address: h59A

Accessed by Serial Interface and I^2C (R/W)

7 … 4	3 … 0
X Rate	Y Rate

Bits [7:4]: Corresponds to the percentage X% in Chapter 7. Used for random early drop. Granularity 6.25%. **(Default: 4'h8)**

Bits[3:0]: Corresponds to the percentage Y% in Chapter 7. Used for random early drop. Granularity 6.25%.**(Default: 4'hE)**

10.6.152 RDRC1 – WRED Rate Control 1

I^2C Address: h086, Serial Interface Address: h59B

Accessed by Serial Interface and I^2C (R/W)

7 … 4	3 … 0
Z Rate	B Rate

Bits [7:4]: Corresponds to the percentage Z% in Chapter 7. Used for random early drop. Granularity 6.25%.%. **(Default: 4'h6)**

Bits[3:0]: Corresponds to the best effort frame drop percentage B%, when shared pool is all in use and destination port best effort queue reaches UCC. Used for random early drop. Granularity 6.25%.%. **(Default: 4'h8)**

10.7 Group 6 Address - MISC Group

10.7.1 MII_OP0 – MII Register Option 0

I^2C Address: h0B1, Serial Interface Address: h600

Accessed by serial interface and I^2C (R/W)

7	6	5	4 0
Hfc	1prst	NP	Vendor Spc. Reg Addr

Bit [7]: Half duplex flow control no default enable (Do not use half duplex mode)
0 = Half duplex flow control always enable
1 = Half duplex flow control by negotiation

Bit[6]: Link partner reset auto-negotiate disable

Bit [5] Next page enable
1: enable
0: disable

Bit[4:0]: Vendor specified link status register address (null value means don't use it) **(Default 00)**

10.7.2 MII_OP1 – MII Register Option 1

I^2C Address: h0B2, Serial Interface Address: h601

Accessed by serial interface and I^2C (R/W)

7 4	3 0
Speed bit location	Duplex bit location

Bits[3:0]: Duplex bit location in vendor specified register

Bits [7:4]: Speed bit location in vendor specified register **(Default 00)**

10.7.3 FEN – Feature Register

I^2C Address: h0B3, Serial Interface Address: h602

Accessed by serial interface and I^2C (R/W)

7	6	5 3	2	1 0
DML	MII		DS	

Bits [1:0]: Reserved

Bit [2]: Support DS EF Code. **(Default 0)**
0 – Disable
1 – Enable (all ports)
When 101110 is detected in DS field (TOS[7:2]), the frame priority is set for 110 and drop is set for 0.

Bit [5:3]: Reserved

Bit [6]: 0: Enable MII Management State Machine **(Default 0)**
1: Disable MII Management State Machine

Bit [7]: 0: Enable using MCT Link List structure
1: Disable using MCT Link List structure

10.7.4 MIIC0 – MII Command Register 0

Serial Interface Address:h603

Accessed by serial interface (R/W)

Bit [7:0] MII Data [7:0]

Note: Before programming MII command: set FEN[6], check MIIC3, making sure no RDY, and no VALID; then program MII command.

10.7.5 MIIC1 – MII Command Register 1

Serial Interface Address:h604

Accessed by serial interface (R/W)

Bit [7:0] MII Data [15:8]

Note: Before programming MII command: set FEN[6], check MIIC3, making sure no RDY and no VALID; then program MII command.

10.7.6 MIIC2 – MII Command Register 2

Serial Interface Address:h605

Accessed by serial interface (R/W)

7	6 5	4 0
	Mii OP	Register address

Bits [4:0]: REG_AD – Register PHY Address

Bit [6:5] OP – Operation code “10” for read command and “01” for write command

Note: Before programming MII command: set FEN[6], check MIIC3, making sure no RDY and no VALID; then program MII command.

10.7.7 MIIC3 – MII Command Register 3

Serial Interface Address:h606

Accessed by serial interface (R/W)

7	6	5	4 0
Rdy	Valid		PHY address

Bits [4:0]: PHY_AD – 5 Bit PHY Address

Bit [6] VALID – Data Valid from PHY (Read Only)

Bit [7] RDY – Data is returned from PHY (Ready Only)

Note: Before programming MII command: set FEN[6], check MIIC3, making sure no RDY and no VALID; then program MII command.

10.7.8 MIID0 – MII Data Register 0

Serial Interface Address:h607

Accessed by serial interface (RO)

Bit [7:0] MII Data [7:0]

10.7.9 MIID1 – MII Data Register 0

Serial Interface Address:h608

Accessed by serial interface (RO)

Bit [7:0] MII Data [15:8]

10.7.10 LED Mode – LED Control

I^2C Address:h0B4; Serial Interface Address:h609

Accessed by serial interface and I^2C (R/W)

7	6	5 4	3 2	1 0
lpbk		Out Pattern	Clock rate	Hold Time

Bit[1:0] Sample hold time **(Default 2’b00)**
2’b00- 8 msec
2’b01- 16 msec
2’b10- 32 msec
2’b11- 64 msec

Bit[3:2] LED clock speed (serial mode) **(Default 2'b10)**
2'b00- sclk/128 2'b01- sclk/256
2'b10- sclk/1024 2'b11- sclk/2048
LED clock speed (parallel mode) **(Default 2'b10)**
2'b00- sclk/1024 2'b01- sclk/4096
2'b10- sclk/2048 2'b11- sclk/8192

Bit[5:4] LED indicator out pattern (Default 2'b11)
2'b00- Normal output, LED signals go straight out, no logical combination
2'b01- 4 bi-color LED mode
2'b10- 3 bi-color LED mode
2'b11- programmable mode
1. Normal mode:
LED_BYTEOUT_[7]:Collision (COL)
LED_BYTEOUT_[6]:Full duplex (FDX)
LED_BYTEOUT_[5]:Speed[1] (SP1)
LED_BYTEOUT_[4]:Speed[0] (SP0)
LED_BYTEOUT_[3]:Link (LNK)
LED_BYTEOUT_[2]:Rx (RXD)
LED_BYTEOUT_[1]:Tx (TXD)
LED_BYTEOUT_[0]:Flow Control (FC)

2. 4 bi-color LED mode
LED_BYTEOUT_[7]:COL
LED_BYTEOUT_[6]:1000FDX
LED_BYTEOUT_[5]:1000HDX
LED_BYTEOUT_[4]:100FDX
LED_BYTEOUT_[3]:100HDX
LED_BYTEOUT_[2]:10FDX
LED_BYTEOUT_[1]:10HDX
LED_BYTEOUT_[0]:ACT
Note: All output qualified by Link signal

3. 3 bi-color LED mode:
LED_BYTEOUT_[7]:COL
LED_BYTEOUT_[6]:LNK
LED_BYTEOUT_[5]:FC
LED_BYTEOUT_[4]:SPD1000
LED_BYTEOUT_[3]:SPD100
LED_BYTEOUT_[2]:FDX
LED_BYTEOUT_[1]:HDX
LED_BYTEOUT_[0]:ACT
Note: All output qualified by Link signal
4. Programmable mode:
LED_BYTEOUT_[7]:Link
LED_BYTEOUT_[6:0]:Defined by the LEDSIG6 ~ LEDSIG0 programmable registers.
Note: All output qualified by Link signal

Bit[6]: Reserved. Must be '0'

Bit[7]: Enable internal loop back. When this bit is set to '1' all ports work in internal loop back mode. For normal operation must be '0'.

10.7.11 CHECKSUM - EEPROM Checksum

I^2C Address h0C5, Serial Interface Address:h60B

Accessed by serial interface and I^2C (R/W)

Bit [7:0]: (Default 00)

Before requesting that the MVTX2603AG updates the EEPROM device, the correct checksum needs to be calculated and written into this checksum register. The checksum formula is:

$$\sum_{i=0}^{FF} i^2C \text{ register} = 0$$

After booting cicle the MVTX2603AG calculates the checksum. If the checksum is not zeroed the MVTX2803AG does not start.

10.7.12 LED User

10.7.13 LEDUSER0

I^2C Address h0BB, Serial Interface Address:h60C

Accessed by serial interface and I^2C (R/W)

7 ... 0
LED USER0

Bit [7:0]: (Default 00)
Content will send out by LED serial logic

10.7.14 LEDUSER1

I^2C Address h0BC, Serial Interface Address:h60D

Accessed by serial interface and I^2C (R/W)

7 ... 0
LED USER1

Bit [7:0]: (Default 00)
Content will send out by LED serial logic

10.7.15 LEDUSER2/LEDSIG2

I^{2}C Address h0BD, Serial Interface Address:h60E

Accessed by serial interface and I^{2}C (R/W)

In serial mode:

7 … 0
LED USER2

Bit [7:0]: (Default 00)
Content will be sent out by LED serial shift logic

In parallel mode: this register is used for programming the LED pin – led_byteout_[2]

7			4	3			0
COL	FDX	SP1	SP0	COL	FDX	SP1	SP0

Bit [3:0]: (Default 4’H0)
Signal polarity:
0: not invert polarity (high true)
1: invert polarity

Bit [7:4] (Default 4’H8)
Signal Select:
0: not select
1: select the corresponding bit
When bits get selected, the led_byteout_[2] = AND (all selected bits)

10.7.16 EDUSER3/LEDSIG3

I^{2}C Address:h0BE, Serial Interface Address:h60F

Access by CPU, serial interface (R/W)

In serial mode:

7 … 0
LED USER3

Bit [7:0]: (Default 8’H33)
Content will be sent out by LED serial shift logic.

In parallel mode: this register is used for programming the LED pin - led_byteout_[3]

7			4	3			0
COL	FDX	SP1	SP0	COL	FDX	SP1	SP0

Bit [3:0]: (Default 4'H3)
Signal polarity:
0: not invert polarity (high true)
1: invert polarity

Bit [7:4] (Default 4'H3)
Signal Select:
0: not select
1: select the corresponding bit
When bits get selected, the led_byteout_[3] = AND (all selected bits)

10.7.17 LEDUSER4/LEDSIG4

I^{2}C Address:h0BF, Serial Interface Address:h610

Access by CPU, serial interface (R/W)

7 ... 0
LED USER4

Bit [7:0] (Default 8'H32)
Content will be sent out by LED serial shift logic.

In parallel mode: this register is used for programming the LED pin - led_byteout_[4]

7			4	3			0
COL	FDX	SP1	SP0	COL	FDX	SP1	SP0

Bit [3:0] (Default 4'H2)
Signal polarity:
0: not invert polarity (high true)
1: invert polarity

Bit [7:4] (Default 4'H3)
Signal Select:
0: not select
1: select the corresponding bit
When bits get selected, the led_byteout_[4] = AND (all selected bits)

10.7.18 LEDUSER5/LEDSIG5

I^{2}C Address:h0C0, Serial Interface Address:h611
Access by CPU, serial interface (R/W)

7 ... 0
LED USER5

Bit [7:0] (Default 8'H20)
Content will be sent out by LED serial shift logic.

In parallel mode: this register is used for programming the LED pin - led_byteout_[5]

7			4	3			0
COL	FDX	SP1	SP0	COL	FDX	SP1	SP0

Bit [3:0] (Default 4'H0)
Signal polarity:
0: not invert polarity (high true
1: invert polarity

Bit [7:4] (Default 4'H2)
Signal Select:
0: not select
1: select the corresponding bit
When bits get selected, the led_byteout_[5] = AND (all selected bits)

10.7.19 LEDUSER6/LEDSIG6

I^2C Address:h0C1, Serial Interface Address:h612

Access by CPU, serial interface (R/W)

7 … 0
LED USER6

Bit [7:0] (Default 8'H40)
Content will be sent out by LED serial shift logic.

In parallel mode: this register is used for programming the LED pin - led_byteout_[6]

7			4	3			0
COL	FDX	SP1	SP0	COL	FDX	SP1	SP0

Bit [3:0] (Default 4'B0000)
Signal polarity:
0: not invert polarity (high true)
1: invert polarity

Bit [7:4] (Default 4'b0100)
Signal Select:
0: not select
1: select the corresponding bit
When bits get selected, the led_byteout_[6] = AND (all selected bits), or the polarity of led_byteout_[6] is controlled by LEDSIG1_0[3]

10.7.20 LEDUSER7/LEDSIG1_0

I²C Address:h0C2, Serial Interface Address:h613

Access by CPU, serial interface (R/W)

7	0
LED USER7	

Bit [7:0] (Default 8'H61)
Content will be sent out by LED serial shift logic.

In parallel mode: this register is used for programming the LED pin - led_byteout_[2]

7			4	3			0
GP	RX	TX	FC	P6	RX	TX	FC

Bit [7] (Default 1'B0)
Global output polarity: this bit controls the output polarity of all led_byteout_ and led_port_sel pins.
0: no invert polarity - (led_byteout_[7:0] are high activated, led_port_sel[9:0] are low activated)
1: invert polarity - (led_byteout_[7:0] are low activated, led_port_sel[9:0] are high activated)

Bit [6:4] (Default 3'B110)
Signal Select:
0: not select
1: select the corresponding bit
When bits get selected, the led_byteout_[6] = OR (all selected bits)

Bit[3] (Default 1'B0)
Polarity control of led_byteout_[6]
0: not invert
1: invert

Bit [2:0] (Default 3'b001)
Signal Select:
0: not select
1: select the corresponding bit
When bits get selected, the led_byteout_[0] = OR (all selected bits)

10.7.21 MIINP0 – MII Next Page Data Register 0

I²C Address:h0C3, Serial Interface Address:h614

Access by CPU and serial interface only (R/W)

Bit [7:0] MII next page Data [7:0]

10.7.22 MIINP1 – MII Next Page Data Register 1

I^2C Address:h0C4, Serial Interface Address:h615

Access by CPU and serial interface only (R/W)

Bit [7:0] MII next page Data [15:8]

10.8 Group F Address - CPU Access Group

10.8.1 GCR-Global Control Register

Serial Interface Address: hF00

Accessed by serial interface. (R/W)

7 – 4	3	2	1	0
	Reset	Bist	SR	SC

Bit [0]: Store configuration **(Default = 0)**
Write ‘1’ followed by ‘0’ to store configuration into external EEPROM

Bit[1]: Store configuration and reset **(Default = 0)**
Write ‘1’ to store configuration into external EEPROM and reset chip

Bit[2]: Start BIST **(Default = 0)**
Write ‘1’ followed by ‘0’ to start the device’s built-in self-test. The result is found in the DCR register.

Bit[3]: Soft Reset **(Default = 0)**
Write ‘1’ to reset the chip

Bit[7:4]: Reserved

10.8.2 DCR-Device Status and Signature Register

Serial Interface Address: hF01

Accessed by serial interface. (RO)

7 – 6	5 – 4	3	2	1	0
Revision	Signature	RE	BinP	BR	BW

Bit [0]: 1 - Busy writing configuration to I^2C
0 – Not Busy writing configuration to I^2C

Bit[1]: 1 - Busy reading configuration from I^2C
0 – Not Busy reading configuration from I^2C

Bit[2]: 1 - BIST in progress
0 - BIST not running

Bit[3]: 1 - RAM Error
0 – RAM OK

Bit[5:4]: Device Signature
00 – 4 Ports Device, non-management mode
01 – 8 Ports Device, non-management mode
10 – 4 Ports Device, management mode possible (need to install CPU)
11 - 8 Ports Device, management mode possible (need to install CPU)

Bit [7:6]: Revision

10.8.3 DCR01-Giga port status

Serial Interface Address: hF02

Accessed by serial interface. (RO)

7	6 - 4	3 - 2	1 - 0
CIC		GIGA1	GIGA0

Bit [1:0]: Giga port 0 strap option
00 – 100Mb MII mode
01 – Reserved
10 – GMII
11 – PCS

Bit[3:2] Giga port 1 strap option
00 – 100Mb MII mode
01 – Reserved
10 – GMII
11 – PCS

Bit [7] Chip initialization completed
Note: DCR01[7], DCR23[7], DCR45[7] and DCR67[7] have the same function.

10.8.4 DCR23-Giga port status

Serial Interface Address: hF03

Accessed by CPU and serial interface. (RO)

7	6 - 4	3 - 2	1 - 0
CIC		GIGA3	GIGA2

Bit [1:0]: Giga port 2 strap option
00 – 100Mb MII mode
01 – Reserved
10 – GMII
11 – PCS

Bit[3:2] Giga port 3 strap option
00 – 100Mb MII mode
01 – Reserved
10 – GMII
11 – PCS

Bit [7] Chip initialization completed

10.8.5 DCR45-Giga port status

Serial Interface Address: hF04

Accessed by CPU and serial interface. (RO)

7	6	4	3	2	1	0
CIC			GIGA5		GIGA4	

Bit [1:0]: Giga port 4 strap option
00 – 100Mb MII mode
01 – Reserved
10 – GMII
11 – PCS

Bit[3:2] Giga port 5 strap option
00 – 100Mb MII mode
01 – Reserved
10 – GMII
11 – PCS

Bit [7] Chip initialization completed

10.8.6 DCR67-Giga port status

Serial Interface Address: hF05

Accessed by CPU and serial interface. (RO)

7	6	4	3	2	1	0
CIC			GIGA7		GIGA6	

Bit [1:0]: Giga port 6 strap option
00 – 100Mb MII mode
01 – Reserved
10 – GMII
11 – PCS

Bit[3:2] Giga port 7 strap option
00 – 100Mb MII mode
01 – Reserved
10 – GMII
11 – PCS

Bit [7] Chip initialization completed

10.8.7 DPST – Device Port Status Register

Serial Interface Address:hF06

Accessed by CPU and serial interface (R/W)

Bit[2:0]: Read back index register. This is used for selecting what to read back from DTST. **(Default 00)**
3'B000 - Port 0 Operating mode and Negotiation status
3'B001 - Port 1 Operating mode and Negotiation status
3'B010 - Port 2 Operating mode and Negotiation status
3'B011 - Port 3 Operating mode and Negotiation status
3'B100 - Port 4 Operating mode and Negotiation status
3'B101 - Port 5 Operating mode and Negotiation status
3'B110 - Port 6 Operating mode and Negotiation status
3'B111 - Port 7 Operating mode and Negotiation status

10.8.8 DTST – Data Read Back Register

Serial Interface Address: hF07

Accessed by CPU and serial interface (RO)

7	6	5	4	3	2	1	0
MD	InfoDet	SigDet	Giga	Inkdn	FE	Fdpx	Fc_en

This register provides various internal information as selected in DPST bit[2:0]

Bit[0]: Flow control enabled

Bit[1]: Full duplex port

Bit[2]: Fast ethernet port (if not giga)

Bit[3]: Link is down

Bit[4]: GIGA port

Bit[5]: Signal detect (when PCS interface mode)

Bit[6]: Pipe signal detected (pipe mode only)

Bit[7]: Module detected (for hot swap purpose)

11.0 BGA and Ball Signal Description

11.1 BGA Views (Top-View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
	AVDD	NC9	SCAN_EN	LB_D[0]	LB_D[4]	LB_D[5]	LB_D[10]	LB_D[16]	LB_D[19]	LB_D[26]	LB_D[31]	LB_D[32]	LB_D[36]	LB_D[40]	LB_D[45]	S_CLK	LB_D[60]	LB_A[3]	LB_A[7]	LB_A[11]	LB_A[15]	B_A[16]	B_A[12]	B_A[7]	B_A[2]	B_OE#	B_D[27]	B_D[26]	NC4	NC3
	DEV_CFG[0]	LA_D[0]	NC7	LB_D[1]	LB_D[3]	LB_D[6]	LB_D[12]	LB_D[17]	LB_D[20]	LB_D[28]	LB_CS0#	LB_D[33]	LB_D[37]	LB_D[41]	LB_D[47]	LB_D[54]	LB_D[58]	LB_D[62]	LB_A[6]	LB_A[10]	LB_A[13]	B_A[17]	B_A[13]	B_A[8]	B_A[3]	B_WE#	B_D[30]	DEV_CFG[1]	NC5	B_D[25]
	LA_D[1]	LA_CLK	LA_D[3]	NC6	LB_D[2]	LB_D[8]	LB_D[15]	LB_D[18]	LB_D[21]	LB_D[29]	LB_RW#	LB_D[34]	LB_D[39]	LB_D[43]	LB_D[48]	LB_D[52]	LB_D[57]	LB_D[61]	LB_A[4]	LB_A[8]	LB_A[12]	B_A[18]	B_A[14]	B_A[11]	B_A[5]	B_A[4]	B_D[28]	AVDD	B_CLK	B_D[22]
	LA_D[2]	LA_D[5]	LA_D[9]	NC8	LB_CLK	LB_D[9]	LB_D[13]	LB_D[23]	LB_D[22]	LB_D[24]	LB_D[25]	LB_D[35]	LB_D[42]	LB_D[44]	LB_D[50]	LB_D[51]	LB_D[55]	LB_D[63]	LB_A[14]	LB_A[18]	LB_A[16]	LB_A[19]	B_A[9]	B_A[10]	B_ADSC#	NC2	B_D[29]	B_D[24]	B_D[18]	B_D[21]
	LA_D[8]	LA_D[7]	LA_D[6]	LA_D[4]	AGND	LB_D[7]	LB_D[14]	LB_D[11]	LB_D[27]	LB_D[30]	LB_CS1#	LB_D[38]	LB_D[46]	LB_D[49]	LB_D[53]	LB_D[56]	LB_D[59]	LB_A[5]	LB_A[9]	LB_A[17]	LB_A[20]	B_A[15]	B_A[6]	B_D[31]	AGND	B_D[17]	B_D[23]	B_D[19]	B_D[16]	B_D[14]
	LA_D[10]	LA_D[11]	LA_D[12]	LA_D[13]	LA_D[14]	VSS	VSS		VDD	VDD		VCC	VCC	VCC	VSS	VSS	VCC	VCC	VCC		VDD	VDD		VSS	VSS	NC1	B_D[9]	B_D[10]	B_D[11]	B_D[12]
	LA_D[15]	LA_D[16]	LA_D[19]	LA_D[18]	LA_D[17]	VDD																			VDD	B_D[20]	B_D[4]	B_D[3]	B_D[6]	B_D[7]
	LA_D[20]	LA_D[21]	LA_D[22]	LA_D[29]	LA_D[24]																					B_D[15]	B_D[8]	P_INT#	B_D[1]	B_D[2]
	LA_D[23]	LA_D[25]	LA_D[26]	LA_D[27]	LA_D[31]	VDD																			VDD	B_D[13]	P_A[1]	P_A[2]	P_WE#	P_RD#
	LA_D[28]	LA_D[30]	LA_CS0#	LA_D[37]	LA_D[33]	VDD																			VDD	B_D[5]	P_D[15]	P_D[11]	P_D[12]	P_D[13]
L	LA_CS1#	LA_RW#	LA_D[32]	LA_D[46]	LA_D[41]																					P_CS#	P_D[14]	P_D[7]	P_D[8]	P_D[10]
	LA_D[34]	LA_D[35]	LA_D[36]	LA_D[53]	LA_D[48]	VCC																			VCC	P_A[0]	B_D[0]	P_D[3]	P_D[4]	P_D[5]
	LA_D[38]	LA_D[40]	LA_D[42]	LA_D[61]	LA_D[56]	VCC							VSS	VSS	VSS	VSS	VSS	VSS							VCC	P_D[6]	P_D[9]	P_D[0]	P_D[1]	P_D[2]
	LA_D[43]	LA_D[44]	LA_D[45]	LA_A[4]	LA_D[39]	VCC							VSS	VSS	VSS	VSS	VSS	VSS							VCC	T_D[15]	T_D[11]	T_D[12]	T_D[13]	T_D[14]
	LA_D[49]	LA_D[50]	LA_D[51]	LA_D[52]	LA_D[47]	VSS							VSS	VSS	VSS	VSS	VSS	VSS							VSS	T_D[10]	T_D[5]	T_D[7]	T_D[8]	T_D[9]
	LA_D[58]	LA_D[57]	LA_D[55]	LA_D[54]	LA_A[7]	VSS							VSS	VSS	VSS	VSS	VSS	VSS							VSS	T_D[6]	T_D[4]	T_D[2]	T_D[1]	T_D[0]
	LA_D[63]	LA_D[62]	LA_D[60]	LA_D[59]	LA_A[11]	VCC							VSS	VSS	VSS	VSS	VSS	VSS							VCC	S_RST#	T_D[3]	TMODE[1]	TMODE[0]	RESOUT#
	LA_A[6]	LA_A[5]	LA_A[3]	LA_A[14]	LA_A[18]	VCC							VSS	VSS	VSS	VSS	VSS	VSS							VCC	G7_RXD[7]	G7_RX_ER	LESYNO#	LE_CLK0	LE_DO
	LA_A[10]	LA_A[9]	LA_A[8]	LA_A[20]	G0_TXD[1]	VCC																			VCC	G7_RXD[3]	G7_RXD[1]	G7_RX_DV	G7_RXD[6]	G7_RXD[5]
	LA_A[15]	LA_A[13]	LA_A[12]	G0_CRS/L	G0_TXD[4]																					G7_TXD[6]	G7_TX_EN	G7_RXD[4]	G7_RXD[2]	G7_RXD[0]
	LA_A[19]	LA_A[17]	LA_A[16]	GREFC[0]	G0_TXD[7]	VDD																			VDD	G7_TXD[0]	G7_TXD[3]	G7_COL	G7_RXCLK	MIITXCK[7]
	MIITXCK[0]	G0_TXD[2]	G0_TXD[0]	G0_TXCLK	G0_TX_ER	VDD																			VDD	G6_RXD[7]	G7_TX_ER	G7_TXD[7]	G7_TXD[5]	G7_TXD[4]
	G0_RXCLK	G0_TXD[5]	G0_TXD[3]	G0_RXD[2]	G0_RXD[6]																					G6_RXD[2]	G6_RXD[4]	G7_TXD[2]	G7_TXD[1]	G7_CRS/L
	G0_RXD[0]	G0_TX_EN	G0_COL	G0_TXD[6]	G0_RX_DV	VSS																			VDD	G6_RXD[0]	G6_RX_ER	G7_TXCLK	GREFC[7]	G6_RX_DV
	G0_RXD[5]	G0_RXD[4]	G0_RXD[3]	G0_RXD[1]	G1_TXD[0]	VSS	VDD		VDD	VDD		VCC	VCC	VCC	VSS	VSS	VCC	VCC	VCC		VDD	VDD		VSS	VSS	G6_TXD[7]	G6_RXD[6]	G6_RXD[5]	G6_RXD[3]	G6_RXD[1]
	G0_RXD[7]	G0_RX_ER	GREFC[1]	G1_RXD[2]	G1_RXD[5]	G1_RXD[7]	G2_TXD[0]	G2_TXD[7]	G2_RXD[2]	G2_RXD[4]	G2_RXD[5]	G3_TXD[1]	G3_TXD[6]	G3_COL	G3_RXD[3]	G3_RXD[6]	IND_CM	G3_RXD[4]	G3_RX_ER	G4_TXD[3]	G4_RXD[1]	G4_RXD[4]	G5_TXD[2]	G5_TXD[4]	G5_TX_ER	G5_RXD[5]	G6_RXCLK	G6_TXD[6]	G6_COL	G6_TX_ER
	G1_TXD[1]	G1_TXCLK	G1CRS/L	G1_TXD[7]	G2_TXCLK	G1_RXD[4]	G2_TXD[4]	G2_TXD[3]	G2_RXD[3]	G2_RXCLK	G2_RXD[7]	G2_RX_ER	G3_TX_EN	G3_RXD[0]	G3_RXD[5]	G3_RXD[7]	GREFC[4]	M_MDIO	G4_TXD[1]	G4_RXD[5]	G4_RXD[6]	G4_RXD[7]	G5_CRS/L	G5_TXD[5]	MIITXCK[5]	G5_RXD[1]	G6_TXD[3]	G6_TXD[4]	G6_TX_EN	G6_TXD[5]
	G1_TXD[2]	G1_TXD[3]	MIITXCK[1]	G1_RXD[0]	G1_RXCLK	G2CRS/L	MIITXCK[2]	G2_TX_EN	G2_RXD[1]	G2_RX_DV	G3_TXCLK	G3_TXD[3]	G3_TXD[5]	G3_RXCLK	G3_RXD[2]	G3_RX_DV	G4_TXCLK	G4_TXD[4]	G4_TXD[6]	G4_TX_ER	G4_RXCLK	G4_RX_DV	G4_RX_ER	G5_TXD[3]	G5_TX_EN	G5_RXD[3]	G5_RXD[6]	G6_TXD[1]	G6_TXD[2]	G6_TXCLK
	G1_TXD[5]	G1_TXD[4]	G1_TX_ER	G1_COL	G1_RXD[6]	GREFC[2]	G2_TXD[2]	G2_TXD[6]	G2_RXD[0]	G2_RXD[6]	GREFC[3]	G3_TXD[2]	MIITXCK[3]	G3_TX_ER	G3_RXD[1]	M_MDC	G4_TXD[0]	G4_TXD[5]	G4_TXD[7]	G4_RXD[0]	G4_COL	GREFC[5]	G5_TXD[0]	G5_TXD[6]	G5_RXD[0]	G5_COL	G5_RXD[4]	G5_RX_ER	G6_CRS/L	G6_TXD[0]
AK	G1_TXD[6]	G1_TX_EN	G1_RXD[1]	G1_RXD[3]	G1_RX_DV	G1_RX_ER	G2_TXD[1]	G2_TXD[5]	G2_TX_ER	G2_COL	G3_CRS/L	G3_TXD[0]	G3_TXD[4]	G3_TXD[7]	CM_CLK	G4CRS/L	G4_TXD[2]	MIITXCK[4]	G4_TX_EN	G4_RXD[2]	G4_RXD[3]	G5_TXCLK	G5_TXD[1]	G5_TXD[7]	G5_RXD[2]	G5_RXCLK	G5_RXD[7]	G5_RX_DV	MIITXCK[6]	GREFC[6]

11.2 Ball- Signal Descriptions

All pins are CMOS type; all Input pins are 5 Volt tolerance, and all Output pins are 3.3 CMOS drive.

Ball No(s)	Symbol	I/O	Description
L30	TRUNK0_EN	I/O - TS with pull up	Trunk enable External pull up or unconnected-disable trunk group 0 and 1 External pull down - enable trunk group 0 and 1 See register TRUNK0_MODE for port selection and trunk enable.
N27	TRUNK1_EN	I/O - TS with pull up	Trunk enable External pull up or unconnected - disable trunk group 2 and 3 External pull down - enable trunk group 2 and 3 See register TRUNK1_MODE for port selection and trunk enable.
L29, L28, N26, M30, M29, M28, N30, N29, N28	P_D[8:0]	I/O - TS with pull up	Bootstrap function - See bootstrap section
K27, L27, K30, K29, K28, J28, H28	RESERVED		Not used - leave unconnected
I^2C Interface (0) Note: In unmanaged mode, Use I^2C and Serial control interface to configure the system			
J27	SCL	Output	I^2C Data Clock
M26	SDA	I/O-TS with pull up	I^2C Data I/O
Serial Control Interface			
J29	PS_STROBE	Input with weak internal pull up	Serial Strobe Pin
J30	PS_DI	Input with weak internal pull up	Serial Data Input
L26	PS_DO (AUTOFD)	Output with pull up	Serial Data Output (AutoFD)
Frame Buffer Interface			
U1, U2, N4, U3, U4, T1, T2, N5, T3, T4, M4, R4, R3, R2, R1, M5, R5, L4, P3, P2, P1, N3, L5, N2, P5, N1, K4, M3, M2, M1, K5, L3, J5, K2, H4, K1, J4, J3, J2, H5, J1, H3, H2, H1, G3, G4, G5, G2, G1, F5, F4, F3, F2, F1, D3, E1, E2, E3, D2., E4, C3, D1, C1, B2	LA_D[63:0]	I/O-TS with pull up	Frame Bank A– Data Bit [63:0]

Ball No(s)	Symbol	I/O	Description
AA1, V5, AA2, AA3, Y1, V4, Y2, Y3, U5, W1, W2, W3, T5, V1, V2, P4, V3	LA_A[19:3]	Output	Frame Bank A – Address Bit [19:3]
W4	LA_A[20]	Output with pull up	Frame Bank A – Address Bit [20]
C2	LA_CLK	Output	Frame Bank A Clock Input
K3	LA_CS0#	Output with pull up	Frame Bank A Low Portion Chip Selection
L1	LA_CS1#	Output with pull up	Frame Bank A High Portion Chip Selection
L2	LA_RW#	Output with pull up	Frame Bank A Read/Write
D18, B18, C18, A17, E17, B17, C17, E16, D17, B16, E15, C16, D16, D15, E14, C15, B15, E13, A15, D14, C14, D13, B14, A14, C13, E12, B13, A13, D12, C12, B12, A12, A11, E10, C10, B10, E9, A10, D11, D10, D8, D9, C9, B9, A9, C8, B8, A8, C7, E7, D7, B7, E8, A7, D6, C6, E6, B6, A6, A5, B5, C5, B4,A4	LB_D[63:0]	I/O-TS with pull up.	Frame Bank B– Data Bit [63:0]
D22, D20, E20, D21, A21, D19, B21, C21, A20, B20, E19, C20, A19, B19, E18, C19, A18	LB_A[19:3]	Output	Frame Bank B – Address Bit [19:3]
E21	LB_A[20]	Output with pull up	Frame Bank B – Address Bit [20]
D5	LB_CLK	Output	Frame Bank B Clock Input
B11	LB_CS0#	Output with pull up	Frame Bank B Low Portion Chip Selection
E11	LB_CS1#	Output with pull up	Frame Bank B High Portion Chip Selection
C11	LB_RW#	Output with pull up	Frame Bank B Read/Write
Switch Database Interface			
E24,B27, D27, C27, A27, A28, B30, D28, E27, C30, D30, G26, E28, D29, E26, E29, H26, E30, J26, F30, F29, F28, F27, H27, G30, G29, K26, G27, G28, H30, H29, M27	B_D[31:0]	I/O-TS with pull up	Switch Database Domain – Data Bit [31:0]

Ball No(s)	Symbol	I/O	Description
C22, B22, A22, E22, C23, B23, A23, C24, D24, D23, B24, A24, E23, C25, C26, B25, A25	B_A[18:2]	Output	Switch Database Address (512K) – Address Bit [18:2]
C29	B_CLK	Output	Switch Database Clock Input
D25	B_ADSC#	Output with pull up	Switch Database Address Status Control
B26	B_WE#	Output with pull up	Switch Database Write Chip Select
A26	B_OE#	Output with pull up	Switch Database Read Chip Select
MII Management Interface			
AJ16	M_MDC	Output	MII Management Data Clock – (common for all MII Ports [7:0])
AG18	M_MDIO	I/O-TS with pull up	MII Management Data I/O – (common for all MII Ports –[7:0])) 2.5Mhz
GMII / MII Interface (193) Gigabit Ethernet Access Port			
AD29, AK30, AJ22, AG17, AJ11, AJ6, AF3,AA4	GREF_CLK [7:0]	Input w/ pull up	Gigabit Reference Clock
AK15	CM_CLK	Input w/ pull up	Common Clock shared by port G[7:0]
AF17	IND/CM	Input w/ pull up	1: select GREF_CLK[7:0] as clock 0: select CM_CLK as clock for all ports
AA30, AK29, AG25, AK18, AJ13, AH7, AH3, AB1	MII TX CLK[7:0]	Input w/ pull up	
V26, W29, W30, Y28, W26, Y29, W27, Y30 AB26, AE27, AE28, AC27, AE29, AC26, AE30, AD26 AK27, AH27, AF26, AJ27, AH26, AK25, AG26, AJ25 AG22, AG21, AG20, AF22, AK21, AK20, AF21, AJ20 AG16, AF16, AG15, AF18, AF15, AH15, AJ15, AG14 AG11, AJ10, AF11, AF10, AG9, AF9, AH9, AJ9 AF6, AJ5, AF5, AG6, AK4, AF4, AK3, AH4 AF1, AC5, AE1, AE2, AE3, AC4, AE4, AD1	G7_RXD[7:0] G6_RXD[7:0] G5_RXD[7:0] G4_RXD[7:0] G3_RXD[7:0] G2_RXD[7:0] G1_RXD[7:0] G0_RXD[7:0]	Input w/ pull up	G[7:0] port – Receive Data Bit [7:0]
W28, AD30, AK28, AH22, AH16, AH10, AK5, AD5	G[7:0]_RX_DV	Input w/ pull down	G[7:0]port – Receive Data Valid

Ball No(s)	Symbol	I/O	Description
V27, AD27, AJ28, AH23, AF19, AG12, AK6, AF2	G[7:0]_RX_ER	Input w/ pull up	G[7:0]port – Receive Error
AC30, AJ29, AG23, AK16, AK11, AH6, AG3, Y4	G[7:0]_CRS/LINK	Input w/ pull down	G[7:0]port – Carrier Sense
AA28, AF29, AJ26, AJ21, AF14, AK10, AJ4, AD3	G[7:0]_COL	Input w/ pull up	G[7:0]port – Collision Detected
AA29, AF27, AK26, AH21, AH14, AG10, AH5, AC1	G[7:0]_RXCLK	Input w/ pull up	G[7:0]port – Receive Clock
AB28, Y26, AB29, AB30, AA27, AC28, AC29, AA26 AE26, AF28, AG30, AG28, AG27, AH29, AH28, AJ30 AK24, AJ24, AG24, AF24, AH24, AF23, AK23, AJ23 AJ19, AH19, AJ18, AH18, AF20, AK17, AG19, AJ17 AK14, AF13, AH13, AK13, AH12, AJ12, AF12, AK12 AF8, AJ8, AK8, AG7, AG8, AJ7, AK7, AF7 AG4, AK1, AJ1, AJ2, AH2, AH1, AG1, AE5 AA5, AD4, AC2, Y5, AC3, AB2, W5, AB3	G7_TXD[7:0] G6_TXD[7:0] G5_TXD[7:0] G4_TXD[7:0] G3_TXD[7:0] G2_TXD[7:0] G1_TXD[7:0] G0_TXD[7:0]	Output	G[7:0]port – Transmit Data Bit [7:0]
Y27, AG29, AH25, AK19, AG13, AH8, AK2, AD2	G[7:0]_TX_EN	Output w/ pull up	G[7:0]port – Transmit Data Enable
AB27, AF30, AF25, AH20, AJ14, AK9, AJ3, AB5	G[7:0]_TX_ER	Output w/ pull up	G[7:0]port – Transmit Error
AD28, AH30, AK22, AH17, AH11, AG5, AG2, AB4	G[7:0]_ TXCLK	Output	G[7:0]port – Gigabit Transmit Clock
PMA Interface (193) Gigabit Ethernet Access Port (PCS)			
AD29, AK30, AJ22, AG17, AJ11, AJ6, AF3,AA4	GREF_CLK [7:0]	Input w/ pull up	Gigabit Reference Clock
AK15	CM_CLK	Input w/ pull up	Common Clock shared by port G[7:0]
AF17	IND/CM	Input w/ pull up	1: select GREF_CLK[7:0] as clock 0: select CM_CLK as clock for all port

Ball No(s)	Symbol	I/O	Description
V26, W29, W30, Y28, W26, Y29, W27, Y30 AB26, AE27, AE28, AC27, AE29, AC26, AE30, AD26 AK27, AH27, AF26, AJ27, AH26, AK25, AG26, AJ25 AG22, AG21, AG20, AF22, AK21, AK20, AF21, AJ20 AG16, AF16, AG15, AF18, AF15, AH15, AJ15, AG14 AG11, AJ10, AF11, AF10, AG9, AF9, AH9, AJ9 AF6, AJ5, AF5, AG6, AK4, AF4, AK3, AH4 AF1, AC5, AE1, AE2, AE3, AC4, AE4, AD1	G7_RXD[7:0] G6_RXD[7:0] G5_RXD[7:0] G4_RXD[7:0] G3_RXD[7:0] G2_RXD[7:0] G1_RXD[7:0] G0_RXD[7:0]	Input w/ pull up	G[7:0]port – PMA Receive Data Bit [7:0]
W28, AD30, AK28, AH22, AH16, AH10, AK5, AD5	G[7:0]_RX_D[8]	Input w/ pull down	G[7:0]port – PMA Receive Data Bit [8]
V27, AD27, AJ28, AH23, AF19, AG12, AK6, AF2	G[7:0]_RX_D[9]	Input w/ pull up	G[7:0]port – PMA Receive Data Bit [9]
AA28, AF29, AJ26, AJ21, AF14, AK10, AJ4, AD3	G[7:0]_RXCLK1	Input w/ pull up	G[7:0]port – PMA Receive Clock 1
AA29, AF27, AK26, AH21, AH14, AG10, AH5, AC1	G[7:0]_RXCLK0	Input w/ pull up	G[7:0]port – PMA Receive Clock 0
AB28, Y26, AB29, AB30, AA27, AC28, AC29, AA26 AE26, AF28, AG30, AG28, AG27, AH29, AH28, AJ30 AK24, AJ24, AG24, AF24, AH24, AF23, AK23, AJ23 AJ19, AH19, AJ18, AH18, AF20, AK17, AG19, AJ17 AK14, AF13, AH13, AK13, AH12, AJ12, AF12, AK12 AF8, AJ8, AK8, AG7, AG8, AJ7, AK7, AF7 AG4, AK1, AJ1, AJ2, AH2, AH1, AG1, AE5 AA5, AD4, AC2, Y5, AC3, AB2, W5, AB3	G7_TXD[7:0] G6_TXD[7:0] G5_TXD[7:0] G4_TXD[7:0] G3_TXD[7:0] G2_TXD[7:0] G1_TXD[7:0] G0_TXD[7:0]	Output	G[7:0]port – PMA Transmit Data Bit [7:0]
1Y27, AG29, AH25, AK19, AG13, AH8, AK2, AD2	2G[7:0]_TXD[8]	3Output w/ pull up	4G[7:0]port – PMA Transmit Data Bit [8]
AB27, AF30, AF25, AH20, AJ14, AK9, AJ3, AB5	G[7:0]_TX_D[9]	Output w/ pull up	G[7:0]port – PMA Transmit Data Bit [9]
AD28, AH30, AK22, AH17, AH11, AG5, AG2, AB4	G[7:0]_ TXCLK	Output	G[7:0]port – PMA Gigabit Transmit Clock

Ball No(s)	Symbol	I/O	Description
Test Facility (3)			
U29	T_MODE0	I/O-TS with pull up	Test – Set upon Reset, and provides NAND Tree test output during test mode Use external Pull up for normal operation
U28	T_MODE1	I/O-TS with pull up	Test – Set upon Reset, and provides NAND Tree test output during test mode Use external Pull up for normal operation
A3	SCAN_EN	Input with pull down	Enable test mode For normal operation leave it unconnected
LED Interface (serial and parallel)			
R28, T26, R27, T27, U27, T28, T29, T30	T_D[7:0]/ LED_PD[7:0]	Output	While resetting, T_D[7,0] are in input mode and are used as strapping pins. Internal pull up LED_PD - Parallel Led data [7:0]
P26, P30, P29, P28, P27, R26, R30, R29	T_D[15:8]/ LED_PT[7:0]	Output	While resetting, T_D[15:8] are in input mode and are used as strapping pins. Internal pull up LED_PR[7:0] – Parallel Led port selection [7:0]
V29	LED_CLK0/ LED_PT[8]	Output	LED_CLK0 – LED Serial Interface Output Clock LED_PT[8] – Parallel Led port sel [8]
V30	LED_BLINK/ LED_DO/ LED_PT[9]	Output	While resetting, LED-BLINK is in input mode and is used as strapping pin. 1: No Blink, 0: Blink. Internal pull up. LED_DO - LED Serial Data Output Stream LED_PT[9] – Parallel Led port sel [9]
V28	LED_PM/ LED_SYNCO#	Output with pull up	While resetting, LED_PM is in input mode and is used as strapping pin. Internal pull up. 1: Enable parallel interface, 0: enable serial interface. LED_SYNCO# - LED Output Data Stream Envelop

Ball No(s)	Symbol	I/O	Description
System Clock, Power, and Ground Pins			
A16	S_CLK	Input	System Clock at 133 MHz
U26	S_RST#	Input – ST	Reset Input
U30	RESOUT#	Output	Reset PHY
B1	DEV_CFG[0]	Input w/ pull down	Not used
B28	DEV_CFG[1]	Input w/ pull down	Not used
AE7, AE9, F10, F21, F22, F9, G25, G6, J25, J6, K25, K6, AA25, AA6, AB25, AB6, AD25, AE10, AE21, AE22	VDD	Power core	+2.5 Volt DC Supply
V14, V15, V16, V17, V18, F16, F24, F25, F6, F7, N13, N14, N15, N16, N17, N18, P13, P14, P15, P16, P17, P18, R13, R14, R15, R16, R17, R18, R25, R6, T13, T14, T15, T16, T17, T18, T25, T6, U13, U14, U15, U16, U17, U18, V13, AD6, AE15, AE16, AE24, AE25, AE6, F15	VSS	Ground	Ground
A1, C28	AVDD	Power	Analog +2.5 Volt DC Supply
E5, E25	AVSS	Ground	Analog Ground
AE12, AE13, AE14, AE17, AE18, AE19, F12, F13, F14, F17, F18, F19, M25, M6, N25, N6, P25, P6, U25, U6, V25, V6, W25, W6	VCC	Power I/O	+3.3 Volt DC Supply
Bootstrap Pins (Default= pull up, 1= pull up 0= pull down)			
AD2, AB5	G0_TX_EN, G0_TX_ER	Default: PCS	Giga0 Mode: G0_TXEN G0_TXER 0 0 MII 0 1 RSVD 1 0 GMII 1 1 PCS
AK2, AJ3	G1_TX_EN, G1_TX_ER	Default: PCS	Giga1 Mode: G1_TXEN G1_TXER 0 0 MII 0 1 RSVD 1 0 GMII 1 1 PCS

Ball No(s)	Symbol	I/O	Description
AH8, AK9	G2_TX_EN, G2_TX_ER	Default: PCS	Giga2 Mode: G0_TXEN G0_TXER 0 0 MII 0 1 RSVD 1 0 GMII 1 1 PCS
AG13, AJ14	G3_TX_EN, G3_TX_ER	Default: PCS	Giga3 Mode: G0_TXEN G0_TXER 0 0 MII 0 1 RSVD 1 0 GMII 1 1 PCS
AK19, AH20	G4_TX_EN, G4_TX_ER	Default: PCS	Giga4 Mode: G0_TXEN G0_TXER 0 0 MII 0 1 RSVD 1 0 GMII 1 1 PCS
AH25, AF25	G5_TX_EN, G5_TX_ER	Default: PCS	Giga5 Mode: G0_TXEN G0_TXER 0 0 MII 0 1 RSVD 1 0 GMII 1 1 PCS
AG29, AF30	G6_TX_EN, G6_TX_ER	Default: PCS	Giga6 Mode: G0_TXEN G0_TXER 0 0 MII 0 1 RSVD 1 0 GMII 1 1 PCS
Y27, AB27	G7_TX_EN, G7_TX_ER	Default: PCS	Giga7 Mode: G0_TXEN G0_TXER 0 0 MII 0 1 RSVD 1 0 GMII 1 1 PCS
After reset T_D[15:0] are used by the LED interface			
T30	T_D[0]	1	Giga link active status 0 – active low 1 – active high
T29	T_D[1]	1	Power saving 0 – No power saving 1 – Power saving Stop MAC clock if no MAC activity.
T28	T_D[2]	Must be pulled-down	Reserved - Must be pulled-down

Ball No(s)	Symbol	I/O	Description
U27	T_D[3]	1	Hot plug port module detection enable 0 – module detection enable 1 – module detection disable
T27	T_D[4]	Must be pulled-down	Reserved - Must be pulled-down
R27	T_D[5]	1	SRAM memory size 0 – 512K SRAM 1 – 256K SRAM
T26	T_D[6]		Reserved
R28	T_D[7]	1	FDB memory depth 1– one memory layer 0 – two memory layers
	LA_A[20], LB_A[20]	11	FDB memory size 11 - 2M per bank = 4M total 10 - 1M per bank = 2M total 0x - 512K per bank = 1M total
R29	T_D[8]	1	EEPROM installed 0 – EEPROM is installed 1 – EEPROM is not installed
R30	T_D[9]	1	MCT Aging enable 0 – MCT aging disable 1 – MCT aging enable
R26	T_D[10]	1	FCB handle aging enable 0 – FCB handle aging disable 1 – FCB handle aging enable
P27	T_D[11]	1	Timeout reset enable 0 – timeout reset disable 1 – timeout reset enable Issue reset if any state machine did not go back to idle for 5sec.
P28, 29, 30	T_D[14:12]		Reserved
P26	T_D[15]	1	External RAM test 0 – Perform the infinite loop of ZBT RAM BIST. Debug test only 1 – Regular operation.

Ball No(s)	Symbol	I/O	Description
N30, N29, N28	P_D[2:0]	111	ZBT RAM la_clk turning 3’b000 - control by reg. **LCLKCR**[2:0] 3’b001 - delay by method # 0 3’b010 - delay by method # 1 3’b011 - delay by method # 2 3’b100 - delay by method # 3 3’b101 - delay by method # 4 3’b110 - delay by method # 5 3’b111 - delay by method # 6 – USE THIS METHOD
M30, M29, M28	P_D[5:3]	111	ZBT RAM lb_clk turning 3’b000 - control by reg. **LCLKCR**[6:4] 3’b001 - delay by method # 0 3’b010 - delay by method # 1 3’b011 - delay by method # 2 3’b100 - delay by method # 3 3’b101 - delay by method # 4 3’b110 - delay by method # 5 3’b111 - delay by method # 6– USE THIS METHOD
L29, L28, N26	P_D[8:6]	111	SBRAM b_clk turning 3’b000 - control by **BCLKCR**[2:0] 3’b001 - delay by method # 0 3’b010 - delay by method # 1 3’b011 - delay by method # 2 3’b100 - delay by method # 3 3’b101 - delay by method # 4 3’b110 - delay by method # 5 3’b111 - delay by method # 6– USE THIS METHOD

Notes:

- # = Active low signal
- Input = Input signal
- In-ST = Input signal with Schmitt-Trigger
- Output = Output signal (Tri-State driver)
- Out-OD= Output signal with Open-Drain driver
- I/O-TS = Input & Output signal with Tri-State driver
- I/O-OD = Input & Output signal with Open-Drain driver

11.3 Ball Signal Name

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	AVDD	M1	LA_D[34]	Y2	LA_A[13]
B1	DEV_CFG[0]	M2	LA_D[35]	V4	LA_A[14]
B2	LA_D[0]	M3	LA_D[36]	Y1	LA_A[15]
C2	LA_CLK	K4	LA_D[37]	AA3	LA_A[16]
C1	LA_D[1]	N1	LA_D[38]	AA2	LA_A[17]
D1	LA_D[2]	P5	LA_D[39]	V5	LA_A[18]
C3	LA_D[3]	N2	LA_D[40]	AA1	LA_A[19]
E4	LA_D[4]	L5	LA_D[41]	W4	LA_A[20]
D2	LA_D[5]	N3	LA_D[42]	Y4	G0_CRS/LINK
E3	LA_D[6]	P1	LA_D[43]	AA4	GREF_CLK[0]
E2	LA_D[7]	P2	LA_D[44]	AB4	G0_TXCLK
E1	LA_D[8]	P3	LA_D[45]	AB3	G0_TXD[0]
D3	LA_D[9]	L4	LA_D[46]	W5	G0_TXD[1]
F1	LA_D[10]	R5	LA_D[47]	AB2	G0_TXD[2]
F2	LA_D[11]	M5	LA_D[48]	AB1	MII_TX_CLK[0]
F3	LA_D[12]	R1	LA_D[49]	AC3	G0_TXD[3]
F4	LA_D[13]	R2	LA_D[50]	Y5	G0_TXD[4]
F5	LA_D[14]	R3	LA_D[51]	AC2	G0_TXD[5]
G1	LA_D[15]	R4	LA_D[52]	AC1	G0_RXCLK
G2	LA_D[16]	M4	LA_D[53]	AD3	G0_COL
G5	LA_D[17]	T4	LA_D[54]	AD4	G0_TXD[6]
G4	LA_D[18]	T3	LA_D[55]	AA5	G0_TXD[7]
G3	LA_D[19]	N5	LA_D[56]	AD2	G0_TX_EN
H1	LA_D[20]	T2	LA_D[57]	AB5	G0_TX_ER
H2	LA_D[21]	T1	LA_D[58]	AD1	G0_RXD[0]
H3	LA_D[22]	U4	LA_D[59]	AE4	G0_RXD[1]
J1	LA_D[23]	U3	LA_D[60]	AC4	G0_RXD[2]
H5	LA_D[24]	N4	LA_D[61]	AE3	G0_RXD[3]
J2	LA_D[25]	U2	LA_D[62]	AE2	G0_RXD[4]
J3	LA_D[26]	U1	LA_D[63]	AE1	G0_RXD[5]

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
J4	LA_D[27]	V3	LA_A[3]	AC5	G0_RXD[6]
K1	LA_D[28]	P4	LA_A[4]	AF1	G0_RXD[7]
H4	LA_D[29]	V2	LA_A[5]	AD5	G0_RX_DV
K2	LA_D[30]	V1	LA_A[6]	AF2	G0_RX_ER
J5	LA_D[31]	T5	LA_A[7]	AF3	GREF_CLK[1]
K3	LA_CS0#	W3	LA_A[8]	AG2	G1_TXCLK
L1	LA_CS1#	W2	LA_A[9]	AG3	G1_CRS/LINK
L2	LA_RW#	W1	LA_A[10]	AE5	G1_TXD[0]
L3	LA_D[32]	U5	LA_A[11]	AG1	G1_TXD[1]
K5	LA_D[33]	Y3	LA_A[12]	AH1	G1_TXD[2]
AH2	G1_TXD[3]	AG10	G2_RXCLK	AG19	G4_TXD[1]
AJ2	G1_TXD[4]	AK10	G2_COL	AK17	G4_TXD[2]
AJ1	G1_TXD[5]	AJ10	G2_RXD[6]	AF20	G4_TXD[3]
AK1	G1_TXD[6]	AG11	G2_RXD[7]	AH18	G4_TXD[4]
AG4	G1_TXD[7]	AH10	G2_RX_DV	AJ18	G4_TXD[5]
AK2	G1_TX_EN	AG12	G2_RX_ER	AK18	MII_TX_CLK[4]
AH3	MII_TX_CLK[1]	AK11	G3_CRS/LINK	AH19	G4_TXD[6]
AJ3	G1_TX_ER	AJ11	GREF_CLK[3]	AJ19	G4_TXD[7]
AH4	G1_RXD[0]	AH11	G3_TXCLK	AK19	G4_TX_EN
AK3	G1_RXD[1]	AK12	G3_TXD[0]	AH20	G4_TX_ER
AF4	G1_RXD[2]	AF12	G3_TXD[1]	AJ20	G4_RXD[0]
AK4	G1_RXD[3]	AJ12	G3_TXD[2]	AF21	G4_RXD[1]
AH5	G1_RXCLK	AH12	G3_TXD[3]	AK20	G4_RXD[2]
AJ4	G1_COL	AK13	G3_TXD[4]	AH21	G4_RXCLK
AG6	G1_RXD[4]	AJ13	MII_TX_CLK[3]	AJ21	G4_COL
AF5	G1_RXD[5]	AH13	G3_TXD[5]	AK21	G4_RXD[3]
AJ5	G1_RXD[6]	AF13	G3_TXD[6]	AF22	G4_RXD[4]
AF6	G1_RXD[7]	AK14	G3_TXD[7]	AG20	G4_RXD[5]
AK5	G1_RX_DV	AG13	G3_TX_EN	AG21	G4_RXD[6]
AK6	G1_RX_ER	AJ14	G3_TX_ER	AG22	G4_RXD[7]
AJ6	GREF_CLK[2]	AH14	G3_RXCLK	AH22	G4_RX_DV

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
AG5	G2_TXCLK	AF14	G3_COL	AJ22	GREF_CLK[5]
AH6	G2_CRS/LINK	AG14	G3_RXD[0]	AK22	G5_TXCLK
AF7	G2_TXD[0]	AK15	CM_CLK	AH23	G4_RX_ER
AK7	G2_TXD[1]	AF17	IND_CM	AG23	G5_CRS/LINK
AJ7	G2_TXD[2]	AJ15	G3_RXD[1]	AJ23	G5_TXD[0]
AG8	G2_TXD[3]	AH15	G3_RXD[2]	AK23	G5_TXD[1]
AG7	G2_TXD[4]	AF15	G3_RXD[3]	AF23	G5_TXD[2]
AH7	MII_TX_CLK[2]	AF18	G3_RXD[4]	AH24	G5_TXD[3]
AK8	G2_TXD[5]	AG15	G3_RXD[5]	AF24	G5_TXD[4]
AJ8	G2_TXD[6]	AF16	G3_RXD[6]	AG24	G5_TXD[5]
AF8	G2_TXD[7]	AG16	G3_RXD[7]	AJ24	G5_TXD[6]
AH8	G2_TX_EN	AH16	G3_RX_DV	AK24	G5_TXD[7]
AK9	G2_TX_ER	AF19	G3_RX_ER	AG25	MII_TX_CLK[5]
AJ9	G2_RXD[0]	AJ16	M_MDC	AH25	G5_TX_EN
AH9	G2_RXD[1]	AG18	M_MDIO	AF25	G5_TX_ER
AF9	G2_RXD[2]	AK16	G4_CRS/LINK	AJ25	G5_RXD[0]
AG9	G2_RXD[3]	AG17	GREF_CLK[4]	AG26	G5_RXD[1]
AF10	G2_RXD[4]	AH17	G4_TXCLK	AK25	G5_RXD[2]
AF11	G2_RXD[5]	AJ17	G4_TXD[0]	AK26	G5_RXCLK
AJ26	G5_COL	AA27	G7_TXD[3]	P29	T_D[13]
AH26	G5_RXD[3]	AB30	G7_TXD[4]	P30	T_D[14]
AJ27	G5_RXD[4]	AB29	G7_TXD[5]	P26	T_D[15]
AF26	G5_RXD[5]	Y26	G7_TXD[6]	N28	P_D[0]
AH27	G5_RXD[6]	AB28	G7_TXD[7]	N29	P_D[1]
AK27	G5_RXD[7]	Y27	G7_TX_EN	N30	P_D[2]
AK28	G5_RX_DV	AB27	G7_TX_ER	M28	P_D[3]
AJ28	G5_RX_ER	AA30	MII_TX_CLK[7]	M29	P_D[4]
AJ29	G6_CRS/LINK	AA29	G7_RXCLK	M30	P_D[5]
AK29	MII_TX_CLK[6]	AA28	G7_COL	N26	P_D[6]
AK30	GREF_CLK[6]	Y30	G7_RXD[0]	L28	P_D[7]
AJ30	G6_TXD[0]	W27	G7_RXD[1]	L29	P_D[8]

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
AH28	G6_TXD[1]	Y29	G7_RXD[2]	N27	TRUNK1_EN
AH29	G6_TXD[2]	W26	G7_RXD[3]	L30	TRUNK0_EN
AG27	G6_TXD[3]	Y28	G7_RXD[4]	K28	NC
AG28	G6_TXD[4]	W30	G7_RXD[5]	K29	NC
AH30	G6_TXCLK	W29	G7_RXD[6]	K30	NC
AG30	G6_TXD[5]	V26	G7_RXD[7]	L27	NC
AF28	G6_TXD[6]	W28	G7_RX_DV	K27	NC
AE26	G6_TXD[7]	V27	G7_RX_ER	M26	SDA
AG29	G6_TX_EN	V30	LED_DO	J27	SCL
AF27	G6_RXCLK	V29	LED_CLK0	J28	NC
AF29	G6_COL	V28	LED_SYNCO#	J29	PS_STROBE
AF30	G6_TX_ER	U26	S_RST#	J30	PS_DI
AD26	G6_RXD[0]	U30	RESOUT#	L26	PS_DO
AE30	G6_RXD[1]	U29	T_MODE[0]	H28	P_INT#
AC26	G6_RXD[2]	U28	T_MODE[1]	M27	B_D[0]
AE29	G6_RXD[3]	T30	T_D[0]	H29	B_D[1]
AC27	G6_RXD[4]	T29	T_D[1]	H30	B_D[2]
AE28	G6_RXD[5]	T28	T_D[2]	G28	B_D[3]
AE27	G6_RXD[6]	U27	T_D[3]	G27	B_D[4]
AB26	G6_RXD[7]	T27	T_D[4]	K26	B_D[5]
AD30	G6_RX_DV	R27	T_D[5]	G29	B_D[6]
AD29	GREF_CLK[7]	T26	T_D[6]	G30	B_D[7]
AD27	G6_RX_ER	R28	T_D[7]	H27	B_D[8]
AD28	G7_TXCLK	R29	T_D[8]	F27	B_D[9]
AC30	G7_CRS/LINK	R30	T_D[9]	F28	B_D[10]
AA26	G7_TXD[0]	R26	T_D[10]	F29	B_D[11]
AC29	G7_TXD[1]	P27	T_D[11]	F30	B_D[12]
AC28	G7_TXD[2]	P28	T_D[12]	J26	B_D[13]
E30	B_D[14]	A23	B_A[12]	E14	LB_D[49]
H26	B_D[15]	B23	B_A[13]	C15	LB_D[48]
E29	B_D[16]	C23	B_A[14]	B15	LB_D[47]

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
E26	B_D[17]	E22	B_A[15]	E13	LB_D[46]
D29	B_D[18]	A22	B_A[16]	A15	LB_D[45]
E28	B_D[19]	B22	B_A[17]	D14	LB_D[44]
G26	B_D[20]	C22	B_A[18]	C14	LB_D[43]
D30	B_D[21]	E21	LB_A[20]	D13	LB_D[42]
C30	B_D[22]	D22	LB_A[19]	B14	LB_D[41]
E27	B_D[23]	D20	LB_A[18]	A14	LB_D[40]
C29	B_CLK	E20	LB_A[17]	C13	LB_D[39]
D28	B_D[24]	D21	LB_A[16]	E12	LB_D[38]
B30	B_D[25]	A21	LB_A[15]	B13	LB_D[37]
F26	NC1	D19	LB_A[14]	A13	LB_D[36]
D26	NC2	B21	LB_A[13]	D12	LB_D[35]
A30	NC3	C21	LB_A[12]	C12	LB_D[34]
A29	NC4	A20	LB_A[11]	B12	LB_D[33]
B29	NC5	B20	LB_A[10]	A12	LB_D[32]
E25	AGND	E19	LB_A[9]	C11	LB_RW#
B28	DEV_CFG[1]	C20	LB_A[8]	E11	LB_CS1#
C28	AVDD	A19	LB_A[7]	B11	LB_CS0#
A28	B_D[26]	B19	LB_A[6]	A11	LB_D[31]
A27	B_D[27]	E18	LB_A[5]	E10	LB_D[30]
C27	B_D[28]	C19	LB_A[4]	C10	LB_D[29]
D27	B_D[29]	A18	LB_A[3]	B10	LB_D[28]
B27	B_D[30]	D18	LB_D[63]	E9	LB_D[27]
E24	B_D[31]	B18	LB_D[62]	A10	LB_D[26]
D25	B_ADSC#	C18	LB_D[61]	D11	LB_D[25]
B26	B_WE#	A17	LB_D[60]	D10	LB_D[24]
A26	B_OE#	E17	LB_D[59]	D8	LB_D[23]
A25	B_A[2]	B17	LB_D[58]	D9	LB_D[22]
B25	B_A[3]	C17	LB_D[57]	C9	LB_D[21]
C26	B_A[4]	E16	LB_D[56]	B9	LB_D[20]
C25	B_A[5]	D17	LB_D[55]	A9	LB_D[19]

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
E23	B_A[6]	A16	S_CLK	C8	LB_D[18]
A24	B_A[7]	B16	LB_D[54]	B8	LB_D[17]
B24	B_A[8]	E15	LB_D[53]	A8	LB_D[16]
D23	B_A[9]	C16	LB_D[52]	C7	LB_D[15]
D24	B_A[10]	D16	LB_D[51]	E7	LB_D[14]
C24	B_A[11]	D15	LB_D[50]	D7	LB_D[13]
B7	LB_D[12]	P15	VSS	AE7	VDD
E8	LB_D[11]	P16	VSS	AE9	VDD
A7	LB_D[10]	P17	VSS	F10	VDD
D6	LB_D[9]	P18	VSS	F21	VDD
C6	LB_D[8]	R13	VSS	F22	VDD
E6	LB_D[7]	R14	VSS	F9	VDD
B6	LB_D[6]	R15	VSS	G25	VDD
A6	LB_D[5]	R16	VSS	G6	VDD
A5	LB_D[4]	R17	VSS	J25	VDD
B5	LB_D[3]	R18	VSS	J6	VDD
C5	LB_D[2]	R25	VSS	K25	VDD
B4	LB_D[1]	R6	VSS	K6	VDD
D5	LB_CLK	T13	VSS	AE12	VCC
A4	LB_D[0]	T14	VSS	AE13	VCC
A3	SCAN_EN	T15	VSS	AE14	VCC
E5	AGND	T16	VSS	AE17	VCC
C4	NC6	T17	VSS	AE18	VCC
B3	NC7	T18	VSS	AE19	VCC
D4	NC8	T25	VSS	F12	VCC
A2	NC9	T6	VSS	F13	VCC
AD6	VSS	U13	VSS	F14	VCC
AE15	VSS	U14	VSS	F17	VCC
AE16	VSS	U15	VSS	F18	VCC
AE24	VSS	U16	VSS	F19	VCC
AE25	VSS	U17	VSS	M25	VCC

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
AE6	VSS	U18	VSS	M6	VCC
F15	VSS	V13	VSS	N25	VCC
F16	VSS	V14	VSS	N6	VCC
F24	VSS	V15	VSS	P25	VCC
F25	VSS	V16	VSS	P6	VCC
F6	VSS	V17	VSS	U25	VCC
F7	VSS	V18	VSS	U6	VCC
N13	VSS	AA25	VDD	V25	VCC
N14	VSS	AA6	VDD	V6	VCC
N15	VSS	AB25	VDD	W25	VCC
N16	VSS	AB6	VDD	W6	VCC
N17	VSS	AD25	VDD		
N18	VSS	AE10	VDD		
P13	VSS	AE21	VDD		
P14	VSS	AE22	VDD		

11.4 Characteristics and Timing

11.4.1 Absolute Maximum Ratings

Storage Temperature	-65C to +150C
Operating Temperature	-40°C to +85C
Maximum Junction Temperature-	+125C
Supply Voltage VCC with Respect to VSS	+3.0 V to +3.6 V
Supply Voltage VDD with Respect to VSS	+2.38 V to +2.75 V
Voltage on Input Pins	-0.5 V to (VCC + 3.3 V)

Caution: Stress above those listed may damage the device. Exposure to the Absolute Maximum Ratings for extended periods may affect device reliability. Functionality at or above these limits is not implied.

11.4.2 DC Electrical Characteristics

VCC = 3.0 V to 3.6 V (3.3v +/- 10%) $T_{AMBIENT}$ = -40°C to +85°C

VDD = 2.5V +10% - 5%

11.4.3 Recommended Operating Conditions

Symbol	Parameter Description	Min	Type	Max	Unit
f_{osc}	Frequency of Operation		133		MHz
I_{CC}	Supply Current – @ 133 MHz (3.3V Supply)	720		930	mA
I_{DD}	Supply Current – @ 133 MHz (2.5V Supply))	1400		1700	mA
V_{OH}	Output High Voltage (CMOS)	2.4			V
V_{OL}	Output Low Voltage (CMOS)			0.4	V
V_{IH-TTL}	Input High Voltage (TTL 5V tolerant)	2.0		VCC + 2.0	V
V_{IL-TTL}	Input Low Voltage (TTL 5V tolerant)			0.8	V
I_{IL}	Input Leakage Current (0.1 V < V_{IN} < VCC)			10	µA
I_{OL}	Output Leakage Current (0.1 V < VOUT < VCC)			10	µA
C_{IN}	Input Capacitance			5	pF
C_{OUT}	Output Capacitance			5	pF
$C_{I/O}$	I/O Capacitance			7	pF
θ_{ja}	Thermal resistance with 0 air flow			11.2	C/W
θ_{ja}	Thermal resistance with 1 m/s air flow			9.9	C/W
θ_{ja}	Thermal resistance with 2 m/s air flow			8.7	C/W
θ_{jc}	Thermal resistance between junction and case			3.3	C/W

11.5 AC Characteristics and Timing

11.5.1 Typical Reset & Bootstrap Timing Diagram

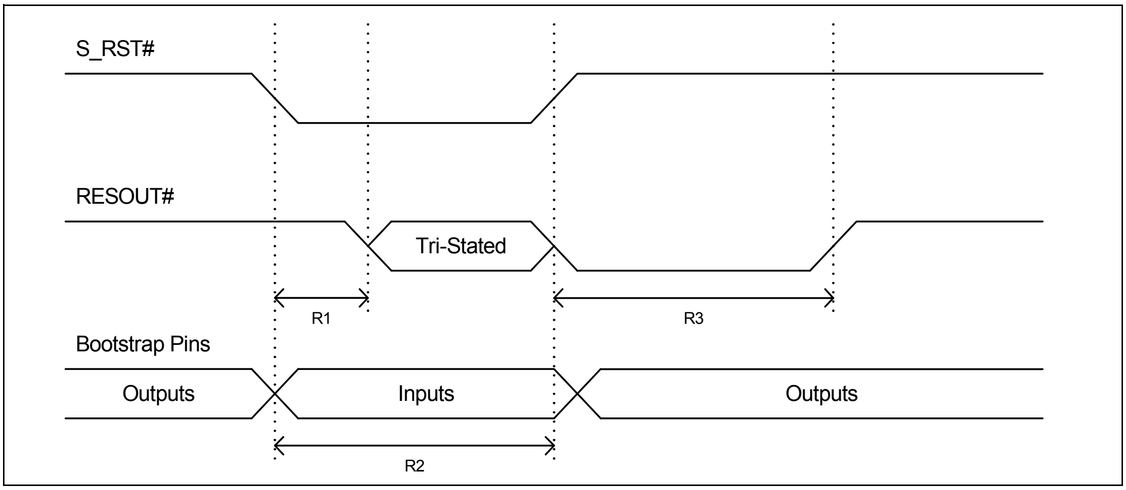


Figure 6 - Typical Reset & Bootstrap Timing Diagram

Symbol	Parameter	Min	Typ	Note:
R1	Delay until RESOUT# is tri-stated		10ns	RESOUT# state is then determined by the external pull-up/down resistor
R2	Bootstrap stabilization	1μs	10μs	Bootstrap pins sampled on rising edge of S_RST#[1]
R3	RESOUT# assertion		2ms	

Table 6 - Reset & Bootstrap Timing

1. The T_D[15:0] pins will switch over to the LED interface functionality in 3 SCLK cycles after S_RST# goes high

11.5.2 Local Frame Buffer ZBT SRAM Memory Interface

11.5.2.1 Local ZBT SRAM Memory Interface A

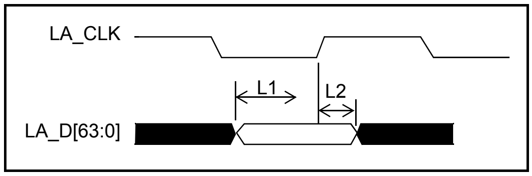


Figure 7 - Local Memory Interface – Input setup and hold timing

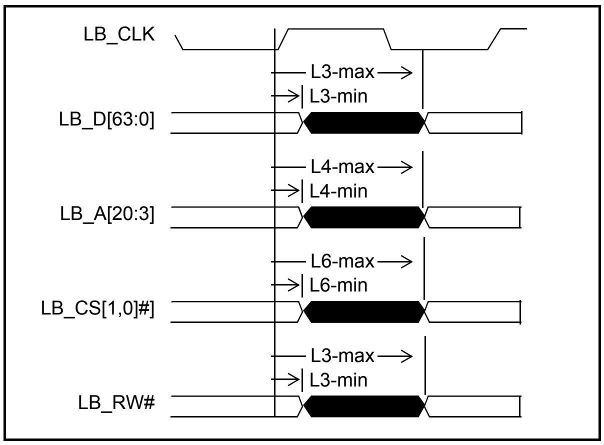


Figure 8 - Local Memory Interface - Output valid delay timing

AC Characteristics – Local frame buffer ZBT-SRAM Memory Interface A

Symbol	Parameter	(SCLK= 133MHz)		Note:
		Min (ns)	Max (ns)	
L1	LA_D[63:0] input set-up time	2.5		
L2	LA_D[63:0] input hold time	1		
L3	LA_D[63:0] output valid delay	3	5	C_L = 25pf
L4	LA_A[20:3] output valid delay	3	5	C_L = 30pf
L6	LA_CS[1:0]# output valid delay	3	5	C_L = 30pf
L9	LA_WE# output valid delay	3	5	C_L = 25pf

11.5.3 Local ZBT SRAM Memory Interface B

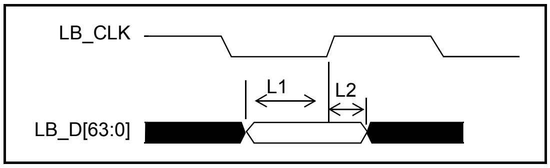


Figure 9 - Local Memory Interface – Input setup and hold timing

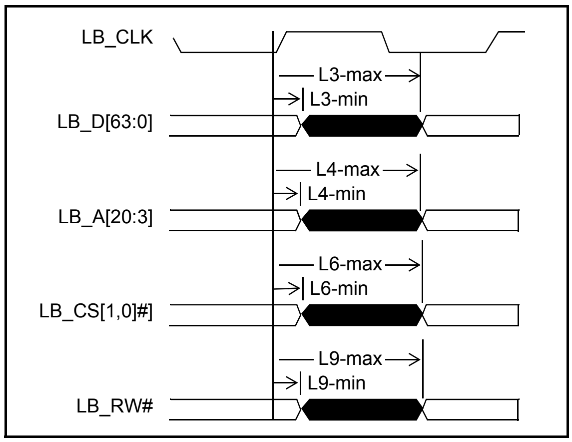


Figure 10 - Local Memory Interface - Output valid delay timing

Local frame buffer ZBT-SRAM Memory Interface B

Symbol	Parameter	(SCLK= 133MHz)		Note:
		Min (ns)	Max (ns)	
L1	LB_D[63:0] input set-up time	2.5		
L2	LB_D[63:0] input hold time	1		
L3	LB_D[63:0] output valid delay	3	5	C_L = 25pf
L4	LB_A[20:3] output valid delay	3	5	C_L = 30pf
L6	LB_CS[1:0]# output valid delay	3	5	C_L = 30pf
L9	LB_WE# output valid delay	3	5	C_L = 25pf

11.5.4 Local Switch Database SBRAM Memory Interface

11.5.4.1 Local SBRAM Memory Interface

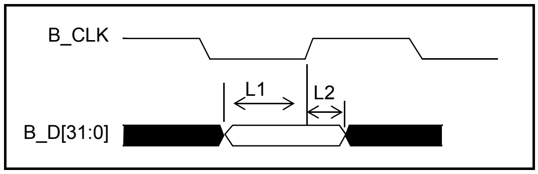


Figure 11 - Local Memory Interface – Input setup and hold timing

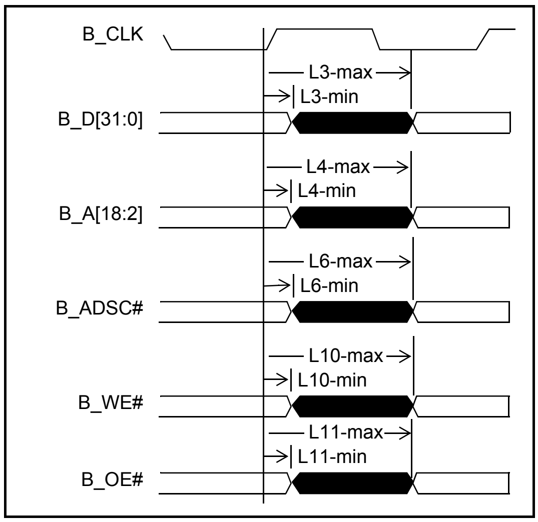


Figure 12 - Local Memory Interface - Output valid delay timing

AC Characteristics – Local Switch Database SBRAM Memory Interface

Symbol	Parameter	(SCLK= 133MHz)		Note:
		Min (ns)	Max (ns)	
L1	B_D[63:0] input set-up time	2.5		
L2	B_D[63:0] input hold time	1		
L3	B_D[63:0] output valid delay	3	5	C_L = 25pf
L4	B_A[20:3] output valid delay	3	5	C_L = 30pf
L6	B_ADSC# output valid delay	3	5	C_L = 30pf
L10	B_WE# output valid delay	3	5	C_L = 25pf
L11	B_OE# output valid delay	3	4	C_L = 25pf

11.5.5 Media Independent Interface

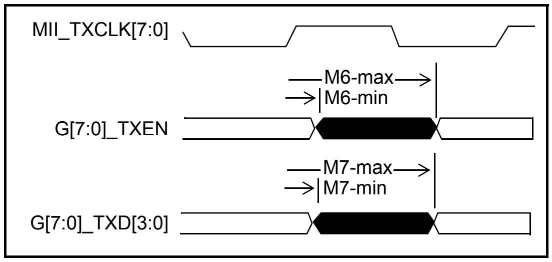


Figure 13 - AC Characteristics – Media Independent Interface

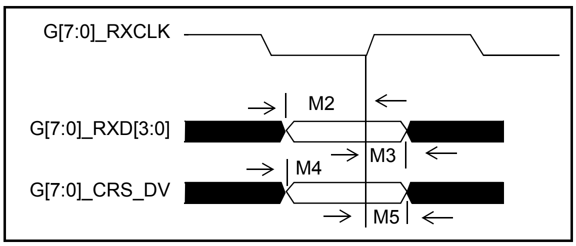


Figure 14 - AC Characteristics – Media Independent Interface

AC Characteristics – Media Independent Interface

Symbol	Parameter	(MII_TXCLK & G_RXCLK = 25MHz)		Note:
		Min (ns)	Max (ns)	
M2	G[7:0]_RXD[3:0] Input Setup Time	4		
M3	G[7:0]_RXD[3:0] Input Hold Time	1		
M4	G[7:0]_CRS_DV Input Setup Time	4		
M5	G[7:0]_CRS_DV Input Hold Time	1		
M6	G[7:0]_TXEN Output Delay Time	3	11	C_L = 20 pF
M7	G[7:0]_TXD[3:0] Output Delay Time	3	11	C_L = 20 pF

11.5.6 Gigabit Media Independent Interface

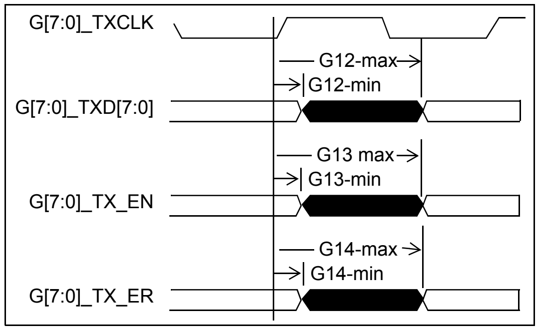


Figure 15 - AC Characteristics- GMII

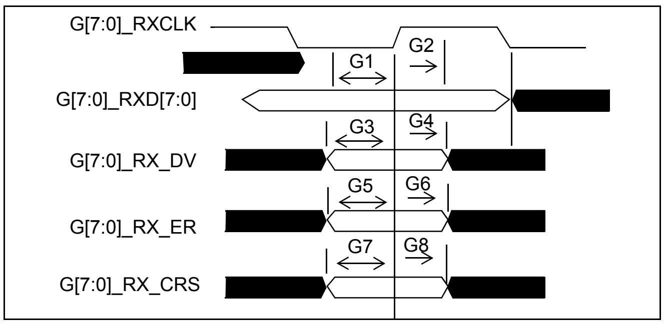


Figure 16 - AC Characteristics – Gigabit Media Independent Interface

AC Characteristics – Gigabit Media Independent Interface

Symbol	Parameter	(G_RCLK & G_REFCLK = 125MHz)		Note:
		Min (ns)	Max (ns)	
G1	**G[7:0]**_RXD[7:0] Input Setup Times	2		
G2	**G[7:0]**_RXD[7:0] Input Hold Times	1		
G3	**G[7:0]**_RX_DV Input Setup Times	2		
G4	**G[7:0]**_RX_DV Input Hold Times	1		
G5	**G[7:0]**_RX_ER Input Setup Times	2		
G6	**G[7:0]**_RX_ER Input Hold Times	1		
G7	**G[7:0]**_CRS Input Setup Times	2		
G8	**G[7:0]**_CRS Input Hold Times	1		
G12	**G[7:0]**_TXD[7:0] Output Delay Times	1	5	C_L = 20pf
G13	**G[7:0]**_TX_EN Output Delay Times	1	5	C_L = 20pf
G14	**G[7:0]**_TX_ER Output Delay Times	1	5	C_L = 20pf

11.5.7 PCS Interface

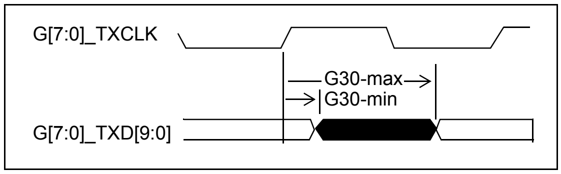


Figure 17 - AC Characteristics – PCS Interface

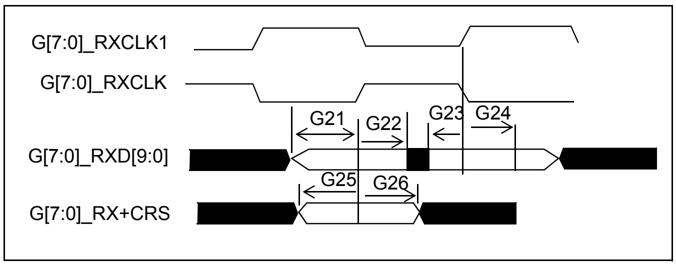


Figure 18 - AC Characteristics – PCS Interface

AC Characteristics – PCS Interface

Symbol	Parameter	(G_RCLK & G_REFCLK = 125MHz)		Note:
		Min (ns)	Max (ns)	
G21	**G[7:0]**_RXD[9:0] Input Setup Times ref to G_RXCLK	2		
G22	**G[7:0]**_RXD[9:0] Input Hold Times ref to G_RXCLK	1		
G23	**G[7:0]**_RXD[9:0] Input Setup Times ref to G_RXCLK1	2		
G24	**G[7:0]**_RXD[9:0] Input Hold Times ref to G_RXCLK1	1		
G25	**G[7:0]**_CRS Input Setup Times	2		
G26	**G[7:0]**_CRS Input Hold Times	1		
G30	**G[7:0]**_TXD[9:0] Output Delay Times	1	5	C_L = 20pf

11.5.8 LED Interface

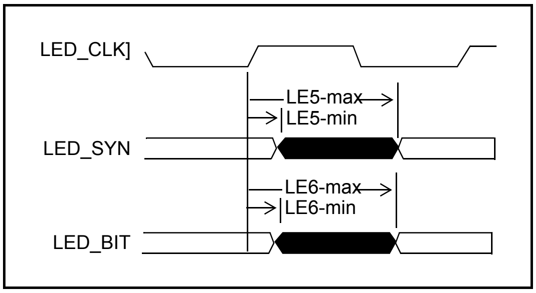


Figure 19 - AC Characteristics – LED Interface

AC Characteristics – LED Interface

Symbol	Parameter	Variable FREQ.		Note:
		Min(ns)	Max (ns)	
LE5	LED_SYN Output Valid Delay	1	7	C_L = 30pf
LE6	LED_BIT Output Valid Delay	1	7	C_L = 30pf

11.5.9 MDIO Input Setup and Hold Timing

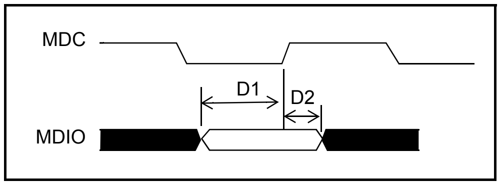


Figure 20 - MDIO Input Setup and Hold Timing

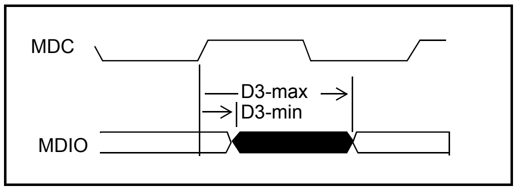


Figure 21 - MDIO Output Delay Timing

MDIO Timing

Symbol	Parameter	1MHz Min (ns)	Max (ns)	Note:
D1	MDIO input setup time	10		
D2	MDIO input hold time	2		
D3	MDIO output delay time	1	20	C_L = 50pf

11.5.10 I^{2}C Input Setup Timing

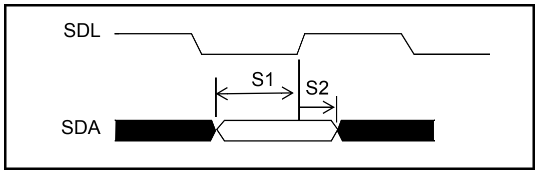


Figure 22 - I^{2}C Input Setup Timing

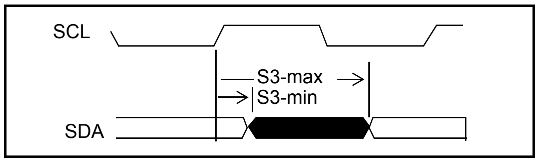


Figure 23 - I^{2}C Output Delay Timing

I^{2}C Timing

Symbol	Parameter	500KHz		
		Min (ns)	Max (ns)	Note:
S1	SDA input setup time	20		
S2	SDA input hold time	1		
S3*	SDA output delay time	1	20	C_L = 30pf

* Open Drain Output. Low to High transistor is controlled by external pullup resistor.

11.5.11 Serial Interface Setup Timing

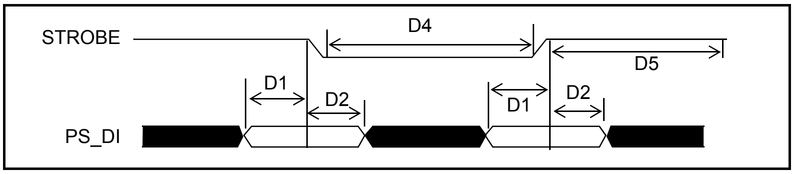


Figure 24 - Serial Interface Setup Timing

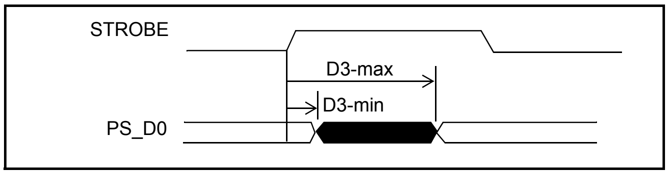
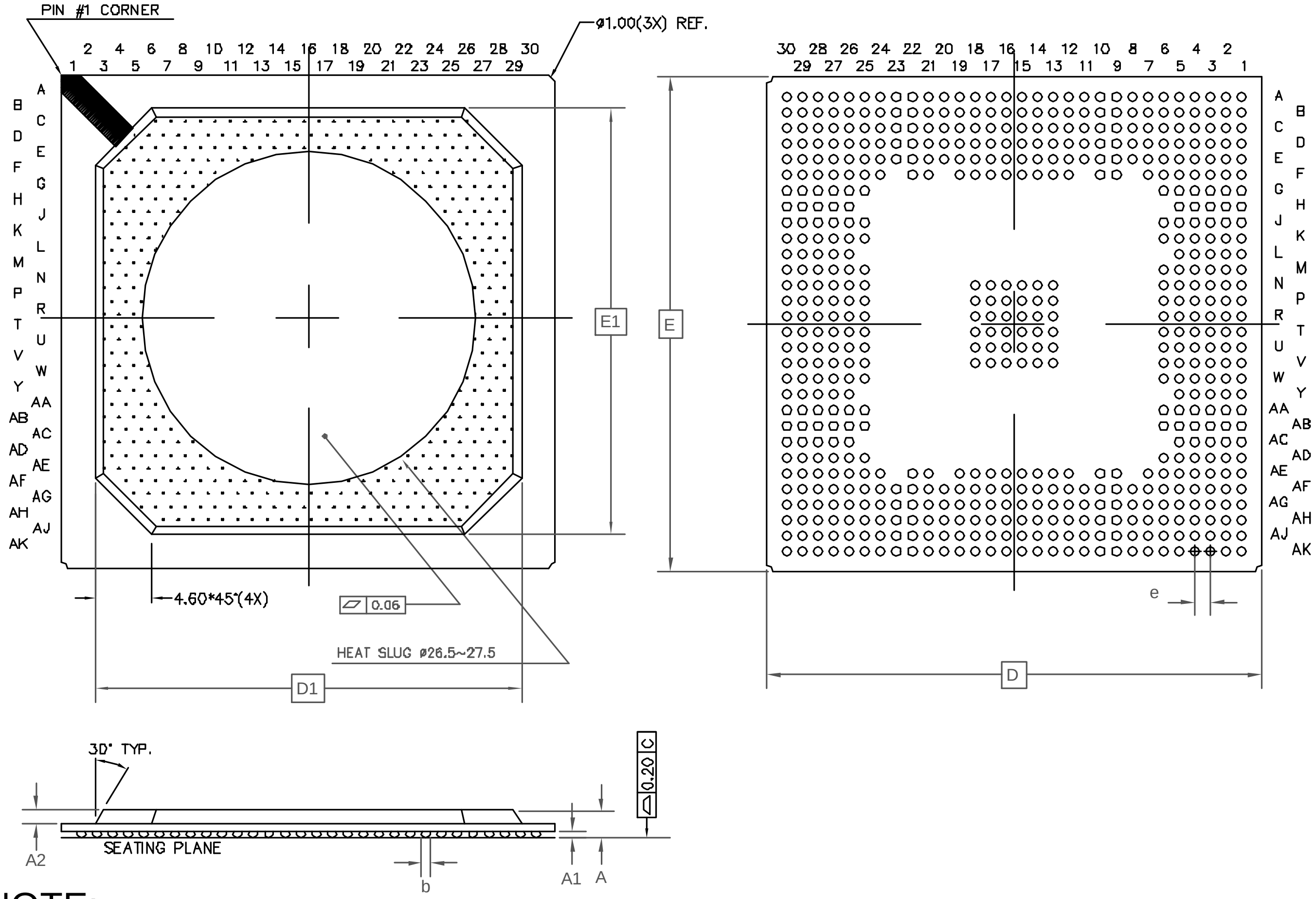


Figure 25 - Serial Interface Output Delay Timing

Serial Interface Timing

Symbol	Parameter	(SCLK =133 MHz) Min (ns)	Max (ns)	Note:
D1	PS_DI setup time	20		
D2	PS_DI hold time	10		
D3	PS_DO output delay time	1	50	C_L = 100pf
D4	Strobe low time	5µs		
D5	Strobe high time	5µs		



DIMENSION	MIN	MAX
A	2.20	2.46
A1	0.50	0.70
A2	1.17 REF	
D	39.80	40.20
D1	34.50 REF	
E	39.80	40.20
E1	34.50 REF	
b	0.60	0.90
e	1.27	
N	596	
Conforms to JEDEC MS - 034		

NOTE:

1. CONTROLLING DIMENSIONS ARE IN MM
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER
3. SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. N IS THE NUMBER OF SOLDER BALLS
5. NOT TO SCALE.
6. SUBSTRATE THICKNESS IS 0.56 MM

ISSUE	1			
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ZARLINK SEMICONDUCTOR

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Package Code GK

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