MVA60000 Series
1.4 Micron CMOS MEGACELL ASICs

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GENERAL DESCRIPTION

Very large scale integrated circuits, requiring large RAM and ROM blocks, often do not suit even high complexity gate arrays, such as Zarlink Semiconductors' CLA60000 series. MVA60000 Megacell ASICs provide RAM, ROM, and PLA macros, optimised for minimum area, which are compiled to match system requirements exactly. Based on an advanced CMOS process using stacked contacts and vias to produce cells virtually 'transparent' to interconnection routing, MVA60000 allows systems up to 80,000 gates to be integrated on a single silicon chip.

With ever-decreasing lifecycles many systems need a clear migration route to higher technology. MVA60000 designs are fully netlist compatible with 1.4 micron CLA60000 array designs, which provides a clear path for upgrading systems by integration of large RAM and ROM blocks, and analog elements. Compatibility extends to Zarlink Semiconductors' new sub-micron CMOS ASIC products, such as the CLA70000 gate array family. Operation over the full military temperature range is easily achieved, even for complex designs, since Zarlink Semiconductors' process allows a maximum junction temperature of 150 degrees C.

FEATURES

- High performance with typical gate delays of 700ps (NAND2 Fanout=2).
- Extensive cell libraries: 180 SSI microcells, 100 MSI and LSI macrocells, and Compiled paracells (ROM to 64K bits, RAM to 16K bits and PLAs) to minimise design timescales.
- Up to 80,000 used gates at <9µW/MHz per loaded gate (Fanout=2) allows integration of entire systems.
- 1.1 micron channel length (1.4 micron drawn) dual layer metal, silicon gate CMOS process, with double polysili con option for precision analog design.
- Slew controlled outputs with drivers up to 24mA for bus driving and other applications.
- Netlist compatible with CLA60000 1.4 micron gate array (and CLA70000 1.0 micron gate array) cell and macro libraries which provides an easy upgrade path for all designs.
- Fully supported by simulation and layout software for quick design and efficient project management.
- ESD protection up to 2kV.
- Easy implementation of JTAG/BIST test philosophies.
- Epitaxial silicon to eliminate Latch-Up.
- Maximum junction temperature of 150 degrees C permits operation over full military temperature range.

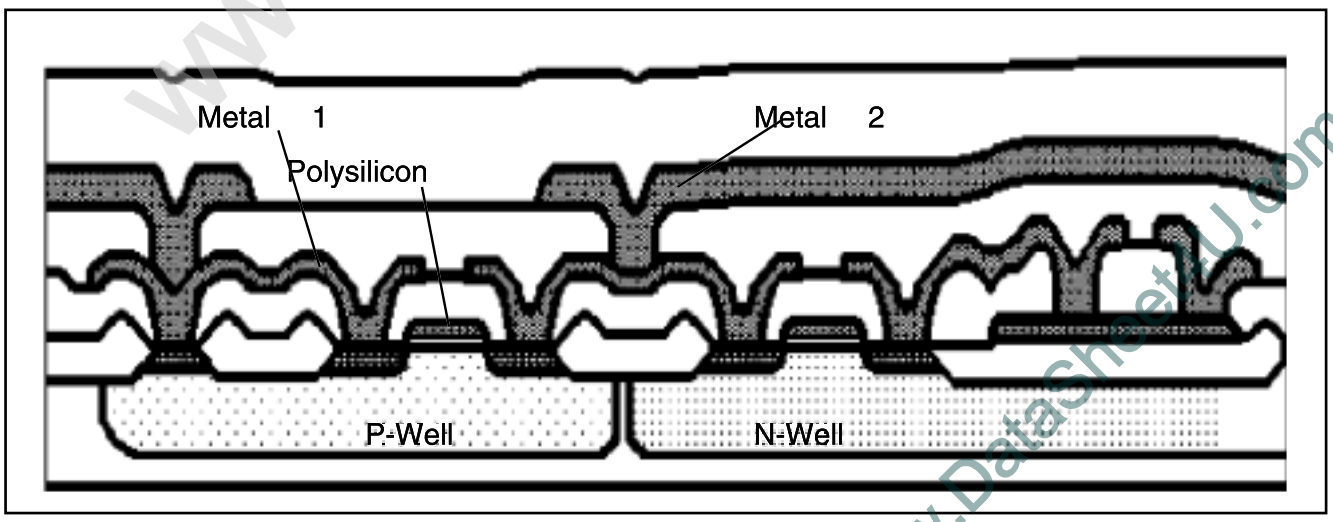


Figure 1: 'VK' Process Cross-Section

CMOS PROCESS TECHNOLOGY

Zarlink Semiconductors' in-house expertise in CMOS process development has produced a range of high density CMOS processes. The MVA60000 Megacell ASICs are totally process compatible with CLA60000 gate arrays designs using the 1.1 micron channel length (1.4 micron drawn) 'VJ' Single Polysilicon Double Level Metal process. Self-aligned, twin-well, oxide isolated devices are fabricated on an epitaxial substrate to eliminate Latch-Up. Manufacture at Zarlink Semiconductors' own Class 1, 6-inch fabrication facility in the UK using the latest equipment and techniques, ensures low defect densities and very high reliability. In addition, the 'VM' Double Polysilicon process variant provides 200 ohms/ square polysilicon resistors which allows precision analogue design for integration of mixed signal systems.

CORE CELL DESIGN

A four transistor group (2 NMOS and 2 PMOS) forms the basic core cell of all the digital logic devices used on MVA60000. Zarlink Semiconductors' processes allow STACKED contacts and vias which provide a higher packing density than conventional processes, by making cells almost 'transparent' to interconnection routing. Flip-flops, LSI macrocells, and other large hierarchical cells are thus interconnected easily, and with a minimum of silicon area. Such transparency also permits a chip layout scheme optimized for data flow, clock distribution, and control signal routing. In addition, symmetrical cell design allows microcell layouts to be easily inverted or reflected if required, which further contributes to efficient implementation of microcells and macrocells, giving very high utilisation of silicon.

INPUT/OUTPUT BUFFER DESIGN

The Input/Output Buffers are designed to offer several interfacing options, TTL and CMOS for example. The cells already contain input 'pull-up' and 'pull-down' resistors and Electro Static Discharge protection elements. Components for implementing Schmitt Triggers, TTL threshold detectors, tristate control, and flip-flops for signal re-timing are also included. A range of output buffers is available with various output drive currents to match system requirements.

Noise transients due to a large number of simultaneously switching outputs are an increasing problem as bus widths widen (The supply pad location, and the inductance of the bond wires and package leads are also factors). MVA60000 Megacells offer several I/O buffers with the capability to control the output slew (di/dt) which are invaluable in controlling these transients when driving large capacitive loads such as buses.

A further process variant, 'VL' is currently in development which will allow Electrically Erasable Programmable ROM to be implemented on MVA60000 devices in addition to the standard logic, RAM, ROM, and PLA cells.

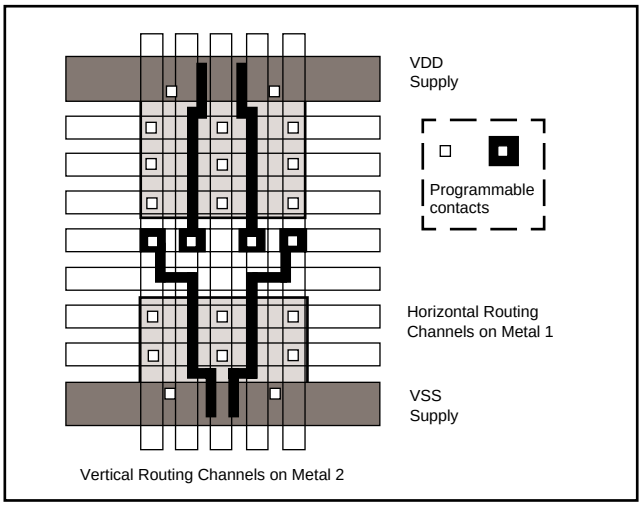
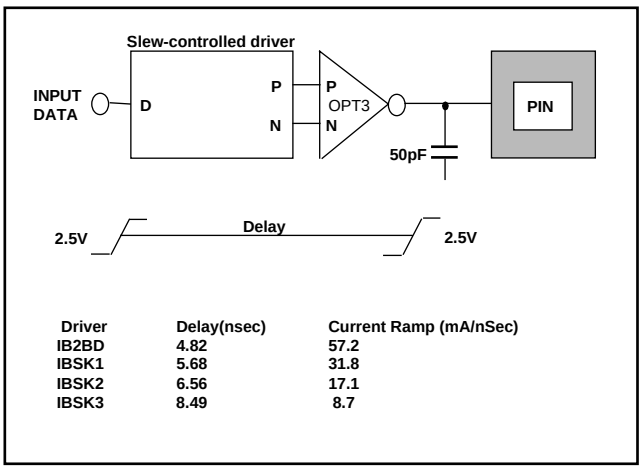


Figure 2: Core Cell Design showing Cell Transparency



Driver	Delay(nsec)	Current Ramp (mA/nSec)
IB2BD	4.82	57.2
IBSK1	5.68	31.8
IBSK2	6.56	17.1
IBSK3	8.49	8.7

Figure 3: Slew Rate Control

DC ELECTRICAL CHARACTERISTICS

All characteristics at Commercial Grade voltage and temperature (Note 1)

CHARACTERISTIC	SYM	VALUE Min	VALUE Typ	VALUE Max	UNIT	CONDITIONS
LOW LEVEL INPUT VOLTAGE	VIL				V	
TTL Inputs (IBTTL1/IBTTL2)				0.8		
CMOS Inputs (IBCMOS1/IBCMOS2)				1.0		
HIGH LEVEL INPUT VOLTAGE	VIH				V	
TTL Inputs (IBTTL1/IBTTL2)		2.0				
CMOS Inputs (IBCMOS1/IBCMOS2)		VDD - 1.0				
INPUT HYSTERESIS (IBST1) Rising	VT+		2.75		V	VIL to VIH
Falling VT-		1.92				VIH to VIL
(IBST2) Rising VT+		2.20				VIL to VIH
Falling VT-		1.35				VIH to VIL
INPUT CURRENT CMOS / TTL INPUTS	IIN		±5		µA	VIN = VDD or VSS
Inputs with 1Kohm Resistors		±5		mA		VIN = VDD or VSS
Inputs with 2Kohm Resistors		±2.5		mA		VIN = VDD or VSS
Inputs with 4Kohm Resistors		±1.25		mA		VIN = VDD or VSS
Inputs with 100Kohm Resistors			±50		µA	VIN = VDD or VSS
Resistor values nominal - See note 2						
HIGH LEVEL OUTPUT VOLTAGE	VOH				V	
All outputs		VDD - 0.05				IOH = - 1µA
Smallest drive cell OP1 / OPOS1		VDD - 1.0	VDD - 0.5			IOH = - 1mA
Low drive cell OP2 / OPOS2		VDD - 1.0	VDD - 0.5			IOH = - 2mA
Standard drive cell OP3 / OPOS3		VDD - 1.0	VDD - 0.5			IOH = - 3mA
Medium drive cell OP6 / OPOS6		VDD - 1.0	VDD - 0.5			IOH = - 6mA
Large drive cell OP12/OPOS12		VDD - 1.0	VDD - 0.5			IOH = - 12mA
LOW LEVEL OUTPUT VOLTAGE	VOL				V	
All Outputs				VSS + 0.05		IOL = 1µA
Smallest Drive Cell OP1 / OPOD1			0.2	0.4		IOL = 2mA
Low drive cell OP2 / OPOD2			0.2	0.4		IOL = 4mA
Standard drive cell OP3 / OPOD3			0.2	0.4		IOL = 6mA
Medium drive cell OP6 / OPOD6			0.2	0.4		IOL = 12mA
Large drive cell OP12/ OPOD12			0.2	0.4		IOL = 24mA
TRISTATE OUTPUT LEAKAGE CURRENT	IOZ				µA	
All open drain output cells		-10		10		VOH = VSS or VDD
OUTPUT SHORT CIRCUIT CURRENT	IOS				mA	
Standard outputs OP3 / OPT3		36	72	144		VDD = MAX VOUT = VDD
(See Note 3) OPOD3 / OPOS3		18	36	72		VDD = MAX VOUT = 0V
STANDBY SUPPLY CURRENT (per gate)	IDDSB		10		nA	
OPERATING SUPPLY CURRENT (per gate) (See Note 4)	IDDOP		1		µA/MHz	
INPUT CAPACITANCE		CI		5	pF	ANY INPUTS (See Note 5)
OUTPUT CAPACITANCE		COUT		5	pF	ANY OUTPUT (See Note 5)
BIDIRECTIONAL PIN CAPACITANCE	CI/O		7		pF	ANY I/O PIN (See Note 6)

Note 1: Commercial grade is 0 - 70 degree C, 5V ± 10% power supply voltage.

Note 2: Resistor value spreads (Min - Max):
LOW VALUE (Rtyp 1K) 0.5 - 2Kohm LOW VALUE (Rtyp 4K) 2K - 8Kohm
LOW VALUE (Rtyp 2K) 1.0 - 4Kohm HIGH VALUE (Rtyp 100K) 25K - 250Kohm

Note 3: Standard driver output OP3 etc. Short circuit current for other outputs will scale. Not more than one output may be shorted at a time for a maximum duration of one second.

Note 4: Excluding peripheral buffers.

Note 5: Excludes package leadframe capacitance or bidirectional pins.

Note 6: Excludes package.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MIN	MAX	UNITS
Supply Voltage	- 0.5	7.0	V
Input Voltage	- 0.5	VDD+0.5	V
Output Voltage	- 0.5	VDD+0.5	V
Storage Temperature:			
Ceramic	- 65	150	degree C
Plastic	- 40	125	degree C

Operation above these absolute maximum ratings may permanently damage device characteristics and may affect reliability.

RECOMMENDED OPERATING LIMITS

PARAMETER	MIN	MAX	UNITS
Supply Voltage	4.0	6.0	V
Input Voltage	VSS	VDD	V
Output Voltage	VSS	VDD	V
Current per pad		100	mA
Operating Temperature:			
Commercial Grade	0	70	degree C
Industrial Grade	-40	85	degree C
Military Grade	-55	125	degree C

AC CHARACTERISTICS FOR SELECTED CELLS

The performance of MVA60000 Megacell devices depends on numerous factors including:

Supply voltage (variation from the nominal 5V).
Ambient temperature, and temperature of the device's active junctions.
Gate fanout, i.e. the logic loading on the gate outputs.
Interconnection loading on the gates.
Processing tolerance, i.e. the manufacturing spreads.

The MVA60000 technology library contains all the performance information for each cell in the design libraries. The PDS design software suite accesses this data, and the simulation program automatically calculates the design's performance under the selected operating conditions. Prior to layout, estimates of the interconnection loadings are used in the simulations. After layout, track loadings are extracted from the physical design to allow re-simulation with actual values to confirm device performance.

The effect of these factors on the propagation delays of a range of selected cells is illustrated in the tables below.

Fanout is in gate load units

INTERNAL CORE CELLS				Typical Propagation Delay (ns)	Worst case Propagation Delay (ns)			
					Commercial		Industrial	
					Fanout		Fanout	
Name	Cells	Description	Symbol	Fanout=2	2	4	2	4
INV2	1	INVERTER DUAL DRIVE	t_{PLH}	0.64	1.20	1.39	1.25	1.44
			t_{PHL}	0.39	0.73	0.88	0.76	0.92
NAND2	1	2 - INPUT NAND GATE	t_{PLH}	0.82	1.54	1.91	1.60	1.99
			t_{PHL}	0.67	1.25	1.67	1.30	1.73
NOR 2	1	2 - INPUT NOR GATE	t_{PLH}	1.11	2.08	2.72	2.16	2.82
			t_{PHL}	0.58	1.09	1.39	1.13	1.44
DF	4	MASTER SLAVE	t_{PLH}	1.04	1.95	2.32	2.02	2.41
		D - TYPE FLIP FLOP	t_{PHL}	0.93	1.74	2.04	1.81	2.12
DFRS	6	MASTER SLAVE D - TYPE	t_{PLH}	1.19	2.23	2.60	2.32	2.71
		WITH SET AND RESET	t_{PHL}	1.12	2.10	2.51	2.18	2.61

INTERMEDIATE BUFFER CELLS				Typical Propagation Delay (ns)	Worst case Propagation Delay (ns)			
					Commercial		Industrial	
					Fanout		Fanout	
Name	Cells	Description	Symbol	Fanout=2	2	4	2	4
IBGATE	-	LARGE 2 INPUT NAND GATE	t_{PLH}	0.73	1.37	1.63	1.42	1.69
		+ 2 INPUT NOR	t_{PHL}	0.62	1.16	1.46	1.21	1.52
IBDF	-	MASTER SLAVE D-TYPE	t_{PLH}	1.04	1.95	2.32	2.02	2.41
		FLIP FLOP	t_{PHL}	0.93	1.74	2.04	1.81	2.12
IBCMOS	-	CMOS INPUT BUFFER	t_{PLH}	1.11	2.08	2.42	2.16	2.51
1		WITH 2 INPUT NAND GATE	t_{PHL}	0.72	1.35	1.54	1.40	1.60

OUTPUT BUFFER CELLS (CMOS)				Typical Propagation Delay (ns)	Worst case Propagation Delay (ns)			
					Commercial		Industrial	
					Fanout		Fanout	
Name	Cells	Description	Symbol	Fanout=10pF	10pF	50pF	10pF	50pF
OP 3	-	STANDARD OUTPUT BUFFER	t_{PLH}	1.26	2.36	8.35	2.45	8.68
			t_{PHL}	0.92	1.72	4.72	1.79	4.91
OP 6	-	MEDIUM OUTPUT BUFFER	t_{PLH}	0.86	1.61	4.61	1.67	4.79
			t_{PHL}	0.70	1.31	2.81	1.36	2.92
OP 12	-	LARGE OUTPUT BUFFER	t_{PLH}	0.70	1.31	2.81	1.36	2.92
			t_{PHL}	0.56	1.05	1.80	1.09	1.87

Note:

Commercial worst case is 4.5V, 70 degree C operating, worst case processing.
Industrial worst case is 4.5V, 85 degree C operating, worst case processing.
Military worst case is 4.5V, 125 degree C operating, worst case processing .

For initial assessments of feasibility, worst case estimations of path delays can be derived from the typical propagation delays given for each cell (for a nominal 5 volt supply and 25 degrees C) by applying approximate derating factors which depend on the temperature and supply voltage the device is expected to experience, and also on processing variations.

* For temperature Zarlink Semiconductors has derived a derating multiplier (Kt) of +0.3% per degree C

* For supply voltage derating, a factor of (Kv) -20% per volt of VDD change should be used.

* For manufacturing variation (Kp), the tolerance is +50%, -30%.

So, for example, the *maximum* variation on typical propagation delays for commercial grade product will be at a supply voltage of 4.5 volts and an ambient temperature of 70 degrees C.

tpd (max) = Kp x Kv x Kt x tpd (typ)
=1.50 x (1+0.20(5.0 - 4.5)) x (1+0.003(70-25)) x tpd(typ)
=1.50 x 1.10 x 1.13 x tpd (typ)
=1.86 x tpd (typ)

The *minimum* delay, will be at a supply voltage of 5.5 volts and an ambient of 0 degrees C and can be calculated as follows:

tpd (min) =0.70 x (1-0.20(5.5-5.0)) x (1-0.003(25-0)) x tpd (typ)
=0.70 x 0.90 x 0.93 x tpd (typ)
=0.58 x tpd (typ)

A similar calculation may be done for any voltage and temperature relevant to the application. For example, the performance derating multiplier for worst case military grade characteristics is 2.15 times (=1.50x1.10x1.30) the commercial typical.

A table of the derating factors for the three standard operating environments is given below.

Product Grade	Temperature Range	**tpd(min)**	**tpd(max)**
Commercial:	0 to +70 degrees C	**0.58**	**1.86**
Industrial:	-40 to +85 degrees C	**0.51**	**1.95**
Military:	-55 to +125 degrees C	**0.48**	**2.15**

The actual path delay also depends on the interconnection loading on each of the gates, and on the size and layout of the chip, so it is difficult to give accurate guidelines for feasibility purposes. However, experience over many years suggests that the average interconnection load can be related to the fanout load on each gate. As a 'rule of thumb', for circuit blocks equivalent to about 2500 random logic gates, the AVERAGE interconnection load is one extra load unit for each load unit of fanout. For a circuit equivalent to roughly 25000 random logic gates, the AVERAGE interconnection load rises to two extra load units for each load unit of fanout.

The interconnection loading of large macrocells is totally dependant on the chip layout. To estimate the loading effect of long inter-macro tracks, an estimate of track length is required. The worst case capacitance of the metal tracks is approximately 0.3pF per mm length. (This figure applies to the first metal layer. The capacitance per unit length of the second metal layer is about half this value, but in general inter-macro signals use both metal 1 and metal 2 tracks.)

The tables on the facing page demonstrate the influence of load on propagation delay. The Megacell MVA60000 design manuals detail the variation of propagation delay with load for each cell. Please contact your local Design Centre for more information, and full support with performance estimates, system definition, and consultation on all aspects of ASIC design.

PACKAGING OPTIONS

Production quantities of MVA60000 devices are available in a wide range of industry-standard ceramic and plastic packages according to the codes shown below. Prototype samples are normally supplied in ceramic only. Where plastic production packages are requested, ceramic prototypes will be supplied in the nearest equivalent and tested to the final test specification.

		PACKAGE DESCRIPTION
DC	**DILMON**	Dual in Line, Multilayer ceramic. Brazed leads. Metal sealed lid. Through board.
DG	**CERDIP**	Dual in Line, Ceramic body. Alloy leadframe. Glass sealed. Through board.
DP	**PLASDIP**	Dual in Line, Copper or Alloy leadframe. Plastic moulded. Through board.
AC	**P.G.A.**	Pin Grid Array. Multilayer Ceramic. Metal sealed lid. Through board.
MP	**SMALL OUTLINE**	Dual in Line. 'Gullwing' formed leads. Plastic moulded. Surface mount.
LC	**LCC**	Leadless Chip Carrier. Multilayer ceramic. Metal sealed lid. Surface mount.
HC	**LEADED CHIP CARRIER**	Quad Multilayer ceramic. Brazed 'J' formed leads. Metal sealed lid. Surface mount.
GC	**LEADED CHIP CARRIER**	Quad Multilayer ceramic. Brazed flat leads. Metal sealed lid. Surface mount.
HG	**QUAD CERPAC**	Quad ceramic body. 'J' formed leads. Glass sealed. Surface mount.
GG	**QUAD CERPAC**	Quad ceramic body. 'Gullwing' formed leads. Glass sealed. Surface mount.
HP	**PLCC**	Quad Leaded plastic Chip Carrier. 'J' formed leads. Plastic moulded. Surface mount.
GP	**PQFP**	Quad plastic Flat Pack. 'Gullwing' formed leads. Plastic moulded. Surface mount.

The range of pin counts available for each package type is detailed below. Zarlink Semiconductors maintains several different variants for each package type and pin count to ensure that MVA60000 chips of various sizes can be packaged as required. In addition, new packages are continually being added to the range, so please consult your local Design Centre for all the up to date packaging options.

	PACKAGE TYPE											
PIN COUNT	**DP**	**DC**	**DG**	**MP**	**HP**	**GP**	**GG**	**HG**	**HC**	**LC**	**GC**	**AC**
8	X	X	X	X								
14	X	X	X	X								
16	X	X	X	X						X		
18	X	X	X	X						X		
20	X	X	X	X	X					X		
22	X	X	X									
24	X	X	X	X						X		
28	X	X	X	X	X			X	X	X		
40	X	X	X							X		
44					X	X	X	X	X	X		
48	X	X										
52						X						
64						X	X			X		
68					X			X	X	X		X
80						X	X					
84					X			X	X	X		X
100						X	X					X
120						X	X					X
128							X					
132											X	X
144						X	X					X
160						X	X					
172											X	
180												X
196											X	

DESIGN THERMAL MANAGEMENT

As gate integration capacity improves with CMOS process geometry reduction, designers now have the ability to design circuits of up to 80,000 gates. In these cases, the chip's power dissipation becomes a very important concern.

With such high gate complexities the power in the core logic becomes increasingly dominant. It becomes essential to offer ultra low power core logic to maintain an acceptable overall chip power dissipation. This is especially true when the device will be assembled in plastic packages.

One of the consequences of higher power consumption is elevated chip temperatures which means relatively expensive special packaging has to be considered - larger package sizes, heatsinking, and more costly assembly methods.

Zarlink Semiconductors' MVA60000 Megacell devices offer low power dissipation. At 5μW per gate per MHz for the core logic and 2μW per gate load, power dissipation is lower than most competitive cell-based designs, resulting in lower operating temperatures and higher inherent long term reliability.

MVA60000 POWER DISSIPATION CALCULATION

To estimate power dissipation for an MVA60000 design, first estimate the number of logic gates (2 input NAND equivalents) used in the design. If the design incorporates RAM blocks, the equivalent gate count for each block should be calculated using the table given on page16 (Paracell Library). From the architecture of the design, an estimate of the fraction of the logic that switches during each clock cycle is derived. This is obviously a rough average, but experience suggests that most circuits lie somewhere between 10% and 40%. For circuits that include RAM blocks the average is reduced, since only very small fractions of the RAM block are usually accessed during a clock cycle. (One 8 bit word from a 1k x 8 bit block for example.)

Another important factor in the power dissipation of an MVA60000 Megacell is the number of output signals switching on each clock cycle, and the loading on the outputs. (Integration of complete systems on an MVA60000 chip, often implies a large number of signal pins, many of which may be driving data buses.)

The calculation of an approximate total dissipation for a Megacell chip is demonstrated by the following example:

Number of used logic gates	25000
Number of bits of RAM used	1k x 8
RAM equivalent gate count	7500
Total equivalent gate count	32500
Fraction of gates switching each clock cycle	5%
Number of gates switching each clock cycle	4875
Power dissipation/gate/MHz (μW)	
(gate fanout typically 2 loads)	9
Total core dissipation/MHz (mW)	44
Number of I/O pads used as outputs	112
Fraction of outputs switching each clock cycle	20%
Number of outputs switching each clock cycle	22
Dissipation/output buffer/MHz/pF (μW)	25
Output loading in pF	50
Power/output buffer/MHz (mW)	1.25
Total output buffer dissipation/MHz (mW)	27.5
Total Power dissipation/MHz (mW)	72
Total Power at 10MHz clock rate (W)	**0.72**
Total Power at 25MHz clock rate (W)	**1.80**

The ability of the device package to disspiate power depends not only on its material and construction, but also on the techniques used in the assembly process (e.g. the die attach method). As a guide, devices which dissipate more than 1 Watt will almost certainly require ceramic packages, even for the commercial operating temperature range (0 to 70 degrees C). Please consult with your local Design Centre for support with power estimation and package choice.

MEGACELL DESIGN ROUTES

Zarlink Semiconductors offers a variety of routes to design MVA60000 Megacell ASICs. The logical design and simulation work can be performed by Zarlink Semiconductor engineers with experience of several thousand ASIC designs. However, many customers prefer to design ASICs themselves. Zarlink Semiconductor supports Megacell design by customers using the PDS software suite, or using several industry standard workstation systems.

Some experienced customers opt to perform the physical design of Megacell ASICs themselves. For this the PDS system is necessary. Visiting a local Zarlink Semiconductor Design Centre has proved to be a successful approach, especially for first time users of the layout tools, as experienced engineers can assist with the layout. Megacell designs incorporating mixed signal cells are usually performed by skilled Zarlink Semiconductor engineers as analogue performance tends to be sensitive to layout technique.

Zarlink Semiconductors' interface to customers is based on the formal Design Review procedure outlined on page 9. A particular set of information is required at each stage depending on the design route chosen. Once the design specification has been agreed between Zarlink Semiconductor project engineers and the design engineers the next stage of work can commence. Further information on

PDS DESIGN SYSTEM

PDS is Zarlink Semiconductors' ASIC computer-aided design system. It provides a fully-integrated, technology independent VLSI design system for all Zarlink Semiconductor CMOS Semi Custom products.

PDS allows the designer to perform all design activities from schematic entry, circuit debugging, fault grading, through to chip layout and generation of a test program for the production test of the finished ICs.

Logical design of MVA60000 Megacell devices is realised with the same software as is used for the new 1.0 micron CLA70000, and CLA60000 gate array families and GPS's 2 micron CMOS semicustom products. PDS runs on DEC VAX equipment (under VMS)* and comprises schematic entry, logic and fault simulation, extensive simulation analysis facilities and advanced library and configuration management tools. Layout and routing is also supported by PDS's interactive Megacell Layout Editor along with full back annotation. Hierarchical design with up to 20 levels is possible.

Supplemented by a three day training course for first-time users, PDS may be used either under licence at the designer's own premises or using design suites and equipment at a Zarlink Semiconductors Design Centre. Use of Design Centre facilities is at an attractive simple rental rate, which is inclusive of computer use.

** DEC, VAX and VMS are trademarks of Digital Equipment Corporation, USA*

DESIGN ROUTES

	PDS2 USED AT GPS DESIGN CENTRE		PDS2 USED BY CUSTOMER ON OWN PREMISES			GPS COMPLETES DESIGN	
						TURNKEY	WORKSTATION
ROUTES	**A**	**B**	**C**	**D**	**E**	**F**	**G**
DESIGN REVIEW 1							
LOGICAL DESIGN	CUSTOMER	CUSTOMER	CUSTOMER	CUSTOMER	CUSTOMER	GPS	CUSTOMER
DESIGN REVIEW 2							
PHYSICAL DESIGN	GPS	CUSTOMER	GPS	CUSTOMER	CUSTOMER (Design Centre)	GPS	GPS
DESIGN REVIEW 3							
PROTOTYPE MANUFACTURING				GPS			
PROTOTYPE EVALUATION				CUSTOMER			
DESIGN REVIEW 4							
PRODUCTION				GPS			

To ensure the Megacell ASIC works first time to specification, Zarlink Semiconductors operates a design audit procedure with four formal review meetings held either at the customer's premises or a local GPS Design Centre:

REVIEW 1: Checks that the required specification can be met by an MVA60000 Megacell device.

LOGICAL DESIGN: Implementation of the design (logic, memory, mixed signal cells) as a hierarchical netlist. The circuit's function is simulated for the eventual environmental conditions to be met by the chip. Definition of the test pattern and full fault simulation are standard procedures during this phase of a GPS ASIC design.

REVIEW 2: Checks that the results of the simulation meet the customer's requirements, and also finalises objectives for the physical design (optimisation of critical paths, placement of specific cells, pinout, and packaging issues etc).

PHYSICAL DESIGN: Placement and interconnection of the cells - using GPS's interactive layout package (Megacell Layout Editor or 'MLE'). This phase is particularly important for Megacells including mixed signal cells.
A final simulation is performed which uses actual track loads extracted from the physical design database to confirm device performance.

REVIEW 3: Establishes that all final simulation results meet the mutually agreed specifications. 'Sign-off' of this review starts the mask manufacture and processing cycle.

PROTO-TYPES: Zarlink Semiconductor manufactures thirteen or fourteen custom masks depending on the process variant required, and develops a test program from the simulation vectors. Zarlink Semiconductor fabricates wafers, assembles devices in the agreed prototype package, and supplies 10 prototypes as standard. Additional prototypes (ordered with the device development) may be supplied at extra cost.
en
tested
be

REVIEW 4: Confirms that the customer has evaluated the prototypes and approves the chip design for full-scale production.

MVA60000 MEGACELL LIBRARIES

MVA60000 Megacell designs use the extensive CLA60000 gate array cell libraries developed from a broad range of ASIC applications experience over more than 14 years. Transformation from a gate array to a cell-based design (to include larger RAM or ROM blocks for example) is a trivial operation. The cells are divided into several libraries depending on their complexity and function.

More than 180 gate-level and SSI functions are included in the MICROCELL library (Page 10) for implementation of 'glue' logic and customer specific macros. To increase design productivity, the 60-strong MACROCELL library (Page 14) already contains optimised SSI macro functions similar to standard TTL and CMOS logic families. A further 50, higher level, cells particularly suitable for digital signal processing functions, are to be found in the DSP MACROCELL library (Page 18). Memory cells (RAM and ROM) are compiled in each case, within the PARACELL library (Page16) to minimize the silicon area required for each block. PLAs are similarly generated. The 'PROC' MACROCELL library (Page 20) contains processor core macros, including the 2901 Bit Slice Processor and the 8085 8 bit processor.

Testing is becoming an increasingly important issue as chip design complexity increases. Zarlink Semiconductors is at the forefront of developments to implement JTAG Built In Self Test on semi-custom devices. The BIST library (page 17) currently contains 34 cells. The boundary scan cells can be configured to provide pseudo-random test vector generators and signature analysers. A 56-page Application Guide contains detailed information on how to incorporate BIST into ASIC designs, and is available on request.

Libraries are continually being enhanced, for example GPS engineers regularly design new macros specifically to customer request. So please contact your local Design Centre for the latest information.

MVA60000 MICROCELL LIBRARY

The MICROCELL library contains more than 180 gate level and SSI functions, input and output buffers, and supply pads.

LOGIC MICROCELLS:

Cell Name	Description	Cell Count	Typical Delay
BUF	Non-Inverting Signal Buffer Cell	2	1.0ns
ST1	Schmitt Trigger	4	1.0ns
DELAY	Delay cell	2	1.4ns
2INV	Dual Inverter	1	0.4ns
INV2	Inverter Dual Drive	1	0.4ns
INV4	Inverter Quad Drive	2	0.4ns
INV8	Inverter x8 Drive	2	0.4ns
NAND2	2-Input Nand Gate	1	0.5ns
ND3	3-Input Nand Gate	2	0.7ns
NAND3	3-Input Nand Gate + Inverter	2	0.7ns
2NAND3	Dual 3-Input NAND Gate	3	0.7ns
NAND4	4-Input NAND Gate	2	0.9ns
NAND5	5-Input NAND Gate	4	1.9ns
NAND6	6-Input NAND Gate	5	2.0ns
NAND8	8-Input NAND Gate	6	2.2ns
NOR2	2-Input NOR Gate	1	0.6ns
NR3	3-Input NOR Gate	2	0.8ns
NOR3	3-Input NOR Gate + Inverter	2	0.8ns
2NOR3	Dual 3-Input NOR Gate	3	0.8ns
NOR4	4-Input NOR Gate	2	1.0ns
NOR5	5-Input NOR Gate	4	1.9ns
NOR6	6-Input NOR Gate	5	2.0ns
NOR8	8-Input NOR Gate	6	2.4ns
A2O2I	2-Input AND to 2-Input NOR Gate + Inverter	2	0.8ns
O2A2I	2-Input OR to 2-Input NAND Gate + Inverter	2	0.8ns
2A2O2I	Dual 2-Input AND to 2-Input NOR Gate	3	0.8ns
2O2A2I	Dual 2-Input OR to 2-Input NAND Gate	3	0.8ns
2ANOR	2-Input ANDs to 2-Input NOR gate	2	0.9ns
2ONAND	2-Input ORs to 2-Input NAND Gate	2	0.9ns
A2O3I	2-Input AND to 3-Input NOR Gate	2	1.0ns
O2A3I	2-Input OR to 3-Input NAND Gate	2	1.0ns
A3O2I	3-Input AND to 2-Input NOR Gate	2	0.9ns
O3A2I	3-Input OR to 2-Input NAND Gate	2	1.1ns
A2O4I	Quad 2-Input ANDs to 4-Input NOR Gate	4	2.9ns
O2A4I	Quad 2-Input ORs to 4-Input NAND Gate	4	2.3ns
A4O2I	Dual 4-Input ANDs to 2-Input NOR Gate	4	2.0ns
O4A2I	Dual 4-Input ORs to 2-Input NAND Gate	4	2.6ns
3A2O3I	Triple 2-Input ANDs to 3-Input NOR Gate	3	1.8ns
3O2A3I	Triple 2-Input ORs to 3-Input NAND Gate	3	1.7ns
A2O2A2I	2-Input AND to 2-Input OR to 2-Input NAND	2	1.0ns
O2A2O2I	2-Input OR to 2-Input AND to 2-Input NOR	2	1.1ns
EX2	Exclusive OR Gate + Inverter	2	0.8ns
EXN2	Exclusive NOR Gate + Inverter	2	0.6ns
EXOR	Exclusive OR Gate + NAND Gate + Inverter	4	1.5ns
EXNOR	Exclusive NOR Gate + NOR Gate + Inverter	4	1.5ns
EXOR2	2-Input Exclusive OR Gate	3	1.3ns
EXNOR2	2-Input Exclusive NOR Gate	3	1.9ns
EXOR3	3-Input Exclusive OR Gate	6	3.3ns
EXNOR3	3-Input Exclusive NOR Gate	6	3.3ns

MVA60000 MICROCELL LIBRARY

The MICROCELL library actually uses basic cells identical to those in the CLA60000 1.4 micron gate array family

LOGIC MICROCELLS:

Cell Name	Description	Cell Count	Typical Delay
HADD	Half Adder + Inverter	4	2.1ns
SUM	Sum Block	4	2.0ns
CARRY	Carry Block + NOR Gate	4	1.7ns
FADD	Full Adder + NOR Gate	8	1.6ns
BMF1	Fast Full Adder 1	6	1.9ns
BMF2	Fast Full Adder 2	6	1.8ns
MUX2TO1	2 to 1 Multiplexer	3	1.5ns
MUX4TO1	4 to 1 Multiplexer	6	2.2ns
MUX8TO1	8 to 1 Multiplexer	12	3.0ns
MUXI2TO1	2 to 1 Inverting Multiplexer	2	1.4ns
MUXI4TO1	4 to 1 Inverting Multiplexer	4	2.6ns
MUXI8TO1	8 to 1 Inverting Multiplexer	12	3.1ns
CLKA	Basic Clock Driver	2	0.8ns
2CLKA	Dual Basic Clock Driver	3	0.5ns
CLKAP	Basic Clock Driver + Inverter	2	0.8ns
CLKAM	Basic Clock Driver + Inverter	2	0.8ns
CLKB	Large Clock Driver + Inverter	4	0.9ns
CLKBP	Large Clock Driver + Inverter	4	0.9ns
CLKE1	Clock Driver with Enable	4	1.9ns
CLKE2	Clock Driver with Enable	4	1.5ns
CLKE3	Clock Driver with Enable	8	2.0ns
TM	Buffered Transmission Gate	1	0.7ns
2TM	Transmission Gate for 2 to 1 Multiplexing	1	0.2ns
BDR	Bus Driver	4	1.7ns
TRID	Tri-State Driver	4	1.4ns
DL	Data Latch	2	1.4ns
DL2	Data Latch	2	1.4ns
DLRS	Data Latch with Set and Reset	3	1.7ns
DLARS	Data Latch with Set and Reset	4	0.9ns
DF	D-Type Flip-Flop	4	0.8ns
DFRS	D-Type Flip-Flop with Set and Reset	6	0.9ns
MDF	Multiplexed Master-Slave D-Type Flip-Flop	6	1.4ns
MDFRS	Multiplexed Master-Slave D-Type Flip-Flop with Set and Reset	8	1.7ns
M3DF	3 to1 Multiplexed Master-Slave D-Type Flip-Flop	8	0.8ns
M3DFRS	3 to 1 Multiplexed Master-Slave D-Type Flip-Flop with Set and Reset	10	0.9ns
JK	J K Flip Flop	8	0.8ns
JKRS	J K Flip Flop with Set and Reset	10	0.9ns
JBARK	JBAR - K Flip Flop	6	0.9ns
JBARKRS	JBAR - K Flip Flop with Set and Reset	8	1.0ns
BJBARK	Buffered J-K Flip-Flop	9	2.8ns
BJBARKRS	Buffered J-K Flip-Flop with Set and Reset	12	2.9ns
BDL	Buffered Data Latch	4	1.3ns
BDLRS	Buffered Data Latch with Set and Reset	6	1.6ns
BDLARS	Buffered Data Latch with Set and Reset	6	3.2ns
BDF	Buffered Master-Slave D-Type Flip-Flop	6	3.3ns
BDFRS	Buffered Master-Slave D-Type Flip-Flop with Set and Reset	9	3.8ns
BMDF	Buffered Multiplexed Master-Slave D-Type Flip-Flop	9	2.6ns
BMDFRS	Buffered Multiplexed Master-Slave D-Type Flip-Flop with Set and Reset	12	2.9ns

MVA60000 MICROCELL LIBRARY

INTERMEDIATE BUFFERS:

Cell Name	Description	Typical Delay
IBST1	Input Buffer with CMOS switching level	1.3ns
IBST2	Input Buffer with 2V switching level	1.9ns
IBSK1	Driver with Lightly Slewed Outputs	0.6ns
IBSK2	Driver with Medium Slewed Outputs	1.1ns
IBSK3	Driver with Heavily Slewed Outputs	2.2ns
IBTRID	Tri-State Driver	1.9ns
IBTRID1	Tri-State Driver with Lightly Slewed Outputs + 2 Inverters	2.1ns
IBTRID2	Tri-State Driver with Medium Slewed Outputs + 2 Inverters	3.1ns
IBTRID3	Tri-State Driver with Heavily Slewed Outputs + 2 Inverters	4.3ns
IBGATE	Large 2-Input NAND Gate + Large 2-Input NOR Gate	0.5ns
IB2BD	Dual High Power Inverters	0.4ns
IBCLKB	Large Clock Driver	0.9ns
IBDF	Master-Slave D-Type Flip-Flop	0.8ns
IBDFA	Master-Slave D-Type Flip-Flop	0.8ns
IBCMOS1	CMOS Input Buffer and Large 2-Input NAND Gate	0.8ns
IBCMOS2	CMOS Input Buffer and Data Latch	0.8ns
IBTTL1	TTL Input Buffer and Large 2-Input NAND Gate	0.8ns
IBTTL2	TTL Input Buffer and Data Latch	0.8ns
DRV3	Triple Output Internal Driver	0.4ns
DRV6	Hex Output Internal Driver	0.4ns

INPUT BUFFERS:

IPNR	Input Cell (with no Pullup or Pulldown resistors)	0.2ns
IPR1P	Input Cell with 1K-Ohm Pull-up Resistor	0.3ns
IPR1M	Input Cell with 1K-Ohm Pull-down Resistor	0.2ns
IPR2P	Input Cell with 2K-Ohm Pull-up Resistor	0.2ns
IPR2M	Input Cell with 2K-Ohm Pull-down Resistor	0.2ns
IPR3P	Input Cell with 4K-Ohm Pull-up Resistor	0.2ns
IPR3M	Input Cell with 4K-Ohm Pull-down Resistor	0.2ns
IPR4P	Input Cell with 100K-Ohm Pull-up Resistor	0.2ns
IPR4M	Input Cell with 100K-Ohm Pull-down Resistor	0.2ns
OSC	Crystal Oscillator Cell	15 MHz

OUTPUT BUFFERS:

OP1	Smallest Drive Output Buffer	0.6ns
OP2	Small Drive Output Buffer	0.5ns
OP3	Standard Drive Output Buffer	0.5ns
OP6	Medium Drive Output Buffer	0.5ns
OP12	Large Drive Output Buffer	0.5ns
OP5B	Standard Drive Non-Inverting Output Buffer	1.4ns
OP11B	Large Drive Non-Inverting Output Buffer	2.0ns
OPT1	Smallest Drive Tri-State Output Buffer	0.5ns
OPT2	Small Drive Tri-State Output Buffer	0.5ns
OPT3	Standard Drive Tri-State Output Buffer	0.5ns
OPT6	Medium Drive Tri-state Output Buffer	0.5ns
OPT12	Large Drive Tri-State Output Buffer	0.5ns
OPT4B	Standard Drive Non-Inverting Tri-State Output Buffer	0.9ns
OPT10B	Large Drive Non-Inverting Tri-State Output Buffer	1.2ns

MVA60000 MICROCELL LIBRARY

OUTPUT BUFFERS:

Cell Name	Description	Typical Delay
OPOD1	Smallest Drive Open-Drain Output Buffer	0.6ns
OPOD2	Small Drive Open-Drain Output Buffer	0.5ns
OPOD3	Standard Drive Open-Drain Output Buffer	0.5ns
OPOD6	Medium Drive Open-Drain Output Buffer	0.5ns
OPOD12	Large Drive Open-Drain Output Buffer	0.5ns
OPOD5B	Standard Drive Non-Inverting Open Drain Output Buffer	1.1ns
OPOD11B	Large Drive Non-Inverting Open Drain Output Buffer	1.4ns
OPOS1	Smallest Drive Open-Source Output Buffer	0.9ns
OPOS2	Small Drive Open-Source Output Buffer	0.6ns
OPOS3	Standard Drive Open-Source Output Buffer	0.5ns
OPOS6	Medium Drive Open-Source Output Buffer	0.4ns
OPOS12	Large Drive Open-Source Output Buffer	0.4ns
OPOS5B	Standard Drive Non-Inverting Open-Source Output Buffer	0.8ns
OPOS11B	Large Drive Non-Inverting Open-Source Output Buffer	1.1ns

SUPPLY PADS:

OPVP	VDD Power Pad (Outputs)
OPVM	GND Power Pad (Outputs)
OPVPB	VDD Power Pad (Outputs) : Break in VDD
OPVMB	GND Power Pad (Outputs) : Break in GND
OPVPBB	VDD Power Pad (Outputs) : Break in VDD and GND
OPVMBB	GND Power Pad (Outputs) : Break in GND and VDD
IBVP	VDD Power Pad (Buffers)
IBVM	GND Power Pad (Buffers)
IBVPB	VDD Power Pad (Buffers) : Break in VDD
IBVMB	GND Power Pad (Buffers) : Break in GND
IBVPBB	VDD Power Pad (Buffers) : Break in VDD
IBVMBB	GND Power Pad (Buffers) : Break in GND
LAVP1	Power Pad for Logic Array
LAVP2	Power Pad for Logic Array
LAVP3	Power Pad for Logic Array
LAVP4	Power Pad for Logic Array
LAVP5	Power Pad for Logic Array
LAVM1	Power Pad for Logic Array
LAVM2	Power Pad for Logic Array
LAVM3	Power Pad for Logic Array
LAVM4	Power Pad for Logic Array
LAVM5	Power Pad for Logic Array
LAGND	Power Pad (Vss) for Logic Array
LAVDD	Power Pad (Vdd) for Logic Array

SUPPLY CELLS:

Cell Name	Description	Cell Count	Typical Delay
GND	GND Cell	2	N/A
VDD	VDD Cell	2	N/A

MVA60000 MACROCELL LIBRARY

Many of these macrocells perform similar functions to the standard TTL and CMOS logic families. Contact your local Zarlink Semiconductor Design Centre for further information on integrating 74 or 4000 Series functions.

ADDERS:

Cell Name	Description	Cell Count	Typical Delay
ADA4	4 bit Binary Full Adders with Fast Carry	60	5.5ns
ADG4	Look Ahead Carry Generator	45	3.0ns

COUNTERS:

CNA4	BCD Counter/4 bit Latch BCD Decoder/Driver	90	7.0ns
CNB4	4 bit Counter Latch	121	6.6ns
CNC4	4 bit Synchronous Counter	65	4.2ns
CND4	4 bit Synchronous Binary Up/Down Counter	80	4.1ns
CND4A	4 bit Synchronous Binary Up/Down Counter with Reset	90	4.3ns
CNE4	4 bit Decade Counter	40	5.2ns
CNF4	4 bit Synchronous Binary Counter	30	7.0ns
CNG4	4 bit Synchronous Binary Counter with Enable	70	2.3ns

DECODERS:

DRA3T8	3 line to 8 line Decoder/Demultiplexer	22	2.7ns
DRA4T16	4 line to 16 line Decoder/Demultiplexer	105	3.8ns
DRA4T16A	4 line to 16 line Decoder/Demultiplexer with Reset	55	2.9ns
DRB3T8	3 line to 8 line Decoder/Demultiplexer with Address Registers	32	4.5ns
DRC3T8	3 line to 8 line Decoder/Demultiplexer with Address Latches	36	3.9ns
DRD2T4	2 line to 4 line Decoder/Demultiplexer	10	2.1ns
DRF4T10	4 line to 10 line BCD Decoder	24	2.6ns
DRG4T10	4 line to 10 line Excess 3 to Decimal Decoder	30	2.5ns
DRH4T10	4 line to 10 line Excess Gray to Decimal Decoder	24	3.0ns
DRI10	BCD to Decimal Decoder/Driver	24	2.5ns
DRJ7	BCD to 7-Segment Decoder/Driver	76	4.7ns
DRK7	BCD to 7-Segment Decoder/Driver	72	3.9ns
DRL7	BCD to 7-Segment Decoder/Driver	52	4.8ns

ENCODERS:

ENA8T3	8 line to 3 line Priority Encoder	33	3.8ns
ENB10T4	10 line to 4 line Priority Encoder	40	4.4ns

FLIP-FLOPS:

FFA8	8 bit Bistable Latches	20	1.4ns
FFB6	6 bit D-Type Flip-Flops with Clear	40	2.8ns
FFC4	4 bit D-Type Flip-Flops with Clear and Complementary Outputs	27	2.4ns
FFD8	Octal D-Type Flip-Flops with Clear	54	2.3ns

ALU/FUNCTION GENERATOR:

FGA4	Arithmetic Logic Unit/Function Generator	153	10.1ns

MVA60000 MACROCELL LIBRARY

These macrocells are constructed from the basic microcell library and are already placed and routed to give optimum use of the silicon area.

MAGNITUDE COMPARATORS:

Cell Name	Description	Cell Count	Typical Delay
MCA4	4 bit Magnitude Comparator	60	7.8ns

MULTIPLIERS:

MLA10	Decade Rate Multiplier	60	3.1ns
MLB4X4	4 bit Binary Multiplier with Tri-State Outputs	120	20.8ns
MLW7	7 bit Wallace Tree Multiplier with Tri-State Outputs	50	11.8ns

MULTIPLEXERS:

MXA8T1	8 line to 1 line Data Selector/Multiplexer	24	5.3ns
MXB4T1	4 line to 1 line Data Selector/Multiplexer with Tri-state Outputs	21	3.4ns
MXB4T1A	4 line to 1 line Data Selector/Multiplexer with Inverted Tri-state Outputs	21	2.7ns
MXC2T1	Quad 2 line to 1 line Data Selector/Multiplexer	14	1.7ns
MXC2T1A	Quad 2 line to 1 line Data Selector/Multiplexer with Inverted Outputs	12	0.9ns
MXD4T1	4 line to 1 line Data Selector/Multiplexer	12	3.3ns
MXE4T1	Dual 4 line to 1 line Data Selector/Multiplexer	12	3.4ns
MXF2T1	Quad 2 line to 1 line Multiplexer with Storage	30	2.9ns

PARITY GENERATORS:

PGA9	9 bit Odd/Even Parity Generator/Checker	26	7.3ns

MONITOR:

PERF	Performance monitor for MVA60000	96	

SHIFT REGISTERS:

SRA2	2 bit Parallel Out Serial Shift Registers with Clear	18	2.3ns
SRA4	4 bit Parallel Out Serial Shift Registers with Clear	30	2.7ns
SRA8	8 bit Parallel Out Serial Shift Registers with Clear	54	2.5ns
SRA8A	8 bit Parallel Out Serial Shift Registers with No Clear	38	2.4ns
SRB2	2 bit Parallel In Serial Out Shift Registers with Clear	24	3.5ns
SRB4	4 bit Parallel In Serial Out Shift Registers with Clear	40	3.8ns
SRB8	8 bit Parallel In Serial Out Shift Registers with Clear	72	3.8ns
SRB8A	8 bit Parallel In Serial Out Shift Registers with No Clear	57	3.5ns
SRC8	8 bit Parallel In Serial Out Shift Registers	72	3.2ns
SRD4	4 bit Serial In Parallel Out Shift Registers	30	2.6ns
SRE4	4 bit Parallel In Parallel Out Shift Registers with JKBAR Input	50	3.5ns
SRF8	8 bit Shift and Store Registers with Tri-State Outputs	115	2.8ns
SRG4	4 bit Bidirectional Universal Shift Registers	60	2.4ns
SRJ4	4 bit Parallel Access Shift Register	33	4.9ns
SRK5	5 bit Shift Register	44	3.5ns

MVA60000 PARACELLS

Using Zarlink Semiconductors' PDS software suite allows designers to compile exactly the RAM, ROM, and PLA blocks required by the design. This promotes efficient use of the silicon area. One line of code defines exactly the paracell size and organisation of the block. An approximate gate count (NAND2 equivalents), and typical access and cycle times are detailed below for a range of compiled paracell RAM, ROM, and PLA blocks.

PARACELL RAM (RAMB):

Organisation	Cell Count	Cycle Time (typ)	Access Time (typ)
128 x 8	1270	17ns	14ns
256 x 8	2100	17ns	14ns
512 x 8	3250	19ns	15ns
1024 x 8	5870	23ns	18ns
2048 x 8	10050	26ns	21ns
128 x 16	2150	16ns	13ns
256 x 16	3420	18ns	15ns
512 x 16	5850	22ns	17ns
1024 x 16	10000	25ns	20ns
128 x 32	3250	18ns	14ns
256 x 32	6200	22ns	17ns
512 x 32	10480	25ns	20ns

PARACELL ROM (ROMCLKD):

128 x 8	290	21ns	16ns
256 x 8	380	22ns	17ns
512 x 8	540	24ns	19ns
1024 x 8	880	28ns	23ns
2048 x 8	1350	36ns	30ns
128 x 16	390	22ns	17ns
256 x 16	540	23ns	18ns
512 x 16	790	25ns	20ns
1024 x 16	1250	29ns	24ns
2048 x 16	2280	37ns	31ns
128 x 32	610	24ns	19ns
256 x 32	800	25ns	20ns
512 x 32	1260	27ns	22ns
1024 x 32	2130	31ns	24ns
2048 x 32	3690	39ns	33ns

PARACELL PLA (PLANAND):

Inputs	Product Terms	Outputs	Cell Count	Cycle Time	Access Time
4	8	2	40	12ns	10ns
8	16	8	70	16ns	14ns
8	64	16	170	21ns	18ns
8	64	32	225	22ns	19ns
12	128	64	620	33ns	29ns

PARACELL PLA (PLANOR):

12	8	4	110	8ns	4ns
16	16	8	160	10ns	4ns
16	32	16	240	11ns	4ns
32	64	32	605	17ns	8ns
32	80	64	920	19ns	6ns

MVA60000 JTAG/BIST CELL LIBRARY

As the number of gates per device pin increases, it is becoming more and more difficult to devise input signals which will allow adequate analysis of functionality from the chip's I/O pins. GPS gate arrays and Megacell designs aim for a level of fault detection by the simulation pattern (test vectors) of better than 90%. GEC Plessey Semiconductors is committed to comprehensive testability in order to produce ASICs which are right first time. Therefore, GPS became an active member of the JTAG consortium, and is at the forefront of Scan-Path and Built-In-Self-Test methods for ASICs. GPS will fully support the JTAG/IEEE P1149-1 specification.

The 'time to market' is a particularly important factor with today's decreasing product lifecycles, so many designers of complex chips prefer to include JTAG/BIST functions to shorten development timescales, despite a small increase in chip area (and a slight degradation of performance in some cases). GPS provides an extensive range of pre-designed cells to allow easy implementation of JTAG principles. A detailed Application Guide on the use of BIST methodologies is available from your local GEC Plessey Semiconductors Design Centre.

TRANSPARENT TEST REGISTER CELLS:

Cell Name	Description	Cell Count	Typical Delay
JTRDU4	4 bit Transparent Test Register with Update Latches	102	
JTRDU8	8 bit Transparent Test Register with Update Latches	150	
JTRDU16	16 bit Transparent Test Register with Update Latches	246	
JTRDU24	24 bit Transparent Test Register with Update Latches	354	
JTRDU32	32 bit Transparent Test Register with Update Latches	450	
JTRDD4	4 bit Transparent Test Register	85	
JTRDD8	8 bit Transparent Test Register	125	
JTRDD16	16 bit Transparent Test Register	205	
JTRDD24	24 bit Transparent Test Register	295	
JTRDD32	32 bit Transparent Test Register	375	

CLOCKED TEST REGISTER CELLS:

JTRCU4	4 bit Clocked Test Register with Update Latches	102	
JTRCU8	8 bit Clocked Test Register with Update Latches	150	
JTRCU16	16 bit Clocked Test Register with Update Latches	246	
JTRCU24	24 bit Clocked Test Register with Update Latches	354	
JTRCU32	32 bit Clocked Test Register with Update Latches	450	
JTRCD4	4 bit Clocked Test Register	85	
JTRCD8	8 bit Clocked Test Register	125	
JTRCD16	16 bit Clocked Test Register	205	
JTRCD24	24 bit Clocked Test Register	295	
JTRCD32	32 bit Clocked Test Register	375	

TEST CONTROL CELLS:

JTAP	PDS BIST JTAG Interface Controller	722	
JTCLK	PDS BIST Clock Gating and Buffer Cell		
JTIDREG	PDS BIST Identification Register	216	

TEST REGISTER COMPONENT CELLS:

JTDUT	Data Bit transparent datapath with Update Latch (Tall)	12	2.0ns
JTDUF	Data Bit transparent datapath with Update Latch (Fat)	12	2.0ns
JTDDT	Data Bit transparent datapath (Tall)	10	1.5ns
JTDDF	Data Bit transparent datapath (Fat)	10	1.5ns
JTCUT	Data Bit clocked datapath with Update Latch (Tall)	12	2.6ns
JTCUF	Data Bit clocked datapath with Update Latch (Fat)	12	2.6ns
JTCDT	Data Bit clocked datapath (Tall)	10	0.8ns
JTCDF	Data Bit clocked datapath (Fat)	10	0.8ns
JTCT	Test Register Local Controller	35	
JTBF16	Test Register Buffer for 4 to19 databits	15	1.6ns
JTBF32	Test Register Buffer for 20 to 34 databits	25	2.1ns

MVA60000 DSP MACROCELL LIBRARY

Many ASICs are now used in digital signal processing applications. So Zarlink Semiconductor has used 14 years experience in ASICs and its expertise in DSP standard products to design over 40 Macrocells to simplify the design of this type of ASIC.

RIPPLE CARRY ADDERS:

Cell Name	Description	Cell Count	Typical Delay
ADR1	1 bit Ripple Carry Adder	8	2.7ns
ADR4	4 bit Ripple Carry Adder	32	2.7ns
ADR8	8 bit Ripple Carry Adder	64	5.4ns
ADR16	16 bit Ripple Carry Adder	128	10.7ns
ADR24	24 bit Ripple Carry Adder	192	15.2ns
ADR32	32 bit Ripple Carry Adder	256	20.0ns

CARRY SELECT ADDERS:

ADS8	8 bit Carry Select Adder	136	2.7ns
ADS16	16 bit Carry Select Adder	272	4.5ns
ADS24	24 bit Carry Select Adder	408	5.8ns
ADS32	32 bit Carry Select Adder	544	7.6ns
ADT8	8 bit Carry Select Adder, with reduced area	85	4.4ns
ADT16	16 bit Carry Select Adder, with reduced area	165	6.5ns
ADT24	24 bit Carry Select Adder, with reduced area	245	8.5ns
ADT32	32 bit Carry Select Adder, with reduced area	325	10.0ns

SUBTRACTOR BLOCKS:

ADSU4	4 bit Subtractor for use with Adder Cells	9	2.0ns
ADSU8	8 bit Subtractor for use with Adder Cells	18	2.0ns
ADSU16	16 bit Subtractor for use with Adder Cells	35	2.0ns
ADSU24	24 bit Subtractor for use with Adder Cells	53	2.0ns
ADSU32	32 bit Subtractor for use with Adder Cells	69	2.0ns

SHIFTERS (Arithmetic Right, Padded with M.S.B.):

SHA4	4 bit Arithmetic Right Shifter	20	2.3ns
SHA8	8 bit Arithmetic Right Shifter	72	4.1ns
SHA16	16 bit Arithmetic Right Shifter	216	5.0ns
SHA24	24 bit Arithmetic Right Shifter	468	5.5ns
SHA32	32 bit Arithmetic Right Shifter	630	5.5ns

SHIFTERS (Barrel Right, Padded with L.S.B. Data Exiting Shifter):

SHB4	4 bit Barrel Right Shifter	30	2.2ns
SHB8	8 bit Barrel Right Shifter	90	3.8ns
SHB16	16 bit Barrel Right Shifter	288	4.9ns
SHB24	24 bit Barrel Right Shifter	676	6.3ns
SHB32	32 bit Barrel Right Shifter	910	6.9ns

SHIFTERS (Logical Right/Left, Padded with Zeros):

SHL4	4 bit Logical Right Shifter	50	3.5ns
SHL8	8 bit Logical Right Shifter	162	5.2ns
SHL16	16 bit Logical Barrel Right Shifter	468	5.9ns
SHL24	24 bit Logical Right Shifter	1040	6.7ns
SHL32	32 bit Logical Right Shifter	1400	6.7ns

MVA60000 DSP MACROCELL LIBRARY

LOGIC UNITS (8 Function):

Cell Name	Description	Cell Count	Typical Delay
FGL04	4 bit Logic Unit	100	5.5ns
FGL08	8 bit Logic Unit	180	5.5ns
FGL016	16 bit Logic Unit	340	5.5ns
FGL024	24 bit Logic Unit	500	5.5ns
FGL032	32 bit Logic Unit	660	5.5ns

ARITHMETIC UNITS (8 Function):

FGAR4	4 bit Arithmetic Unit	117	9.8ns
FGAR8	8 bit Arithmetic Unit	286	10.6ns
FGAR16	16 bit Arithmetic Unit	507	12.4ns
FGAR24	24 bit Arithmetic Unit	728	13.8ns
FGAR32	32 bit Arithmetic Unit	949	15.1ns

MULTIPLIERS AND ASSOCIATED CELLS:

BMA8X8	Mixed Mode Multiplier (8 x 8 bits)	1080	23.0ns
BMA16X16	Mixed Mode Multiplier (16 x 16bits)	2900	40.0ns
BTHE1	3 input, three-bits-at-a-time Booth Encoder	15	2.3ns
BTHD1	Non-inverting, three-bits-at-a-time Booth Decoder	4	1.7ns
BTHD2	Inverting, three-bits-at-a-time Booth Decoder	4	1.7ns

MVA60000 MIXED SIGNAL CAPABILITY

Zarlink Semiconductors has designed mixed signal Megacell devices on 2.0 and 1.4 micron CMOS technologies over many years. The Double Polysilicon variant of the 1.4 micron process (VM) provides accurate capacitance and resistor values which greatly enhances analog performance. The close tolerance and low temperature coefficient of the second polysilicon layer (Sheet Resistance = 200 ohms per square ±15%, nominal Temperature Coefficient = 50ppm) allows integration of precision resistors in a minimum of silicon area.

Experience indicates that most mixed signal designs are specific to their application, with existing designs being modified to meet the customer's precise requirements. Experienced Zarlink Semiconductor engineers perform the design and layout of mixed signal chips in close collaboration with customers, as the analog performance of such devices depends critically on the physical design.

Some examples of the cells we have designed for mixed signal Megacell devices, their equivalent area in terms of basic logic gates, and some of their key parameters, are as follows:

Cell Name	Description	Cell Count	Performance
ANCMPP	Low Power P-Channel Comparator	48	Isupply=120µA
ANMGPAMP	Op-Amp Cell with Power Down	40	BW=1.75MHz
ANSADC8	8 bit, Successive Approximation Analogue to Digital Convertor Cell	870	Tconvert=20µs
ANSDAC8	8 bit, Digital to Analogue Convertor Cell	755	Tsettle=20µs
ANMPLL	Phase Locked Loop and VCO Cell	308	Fmax=16MHz
ANBGR	Digitally Trimmable Bandgap Reference Cell	598	TempCo=50ppm
ANMDTMF	DTMF Generator Cell	188	THD=0.5%
ANMVOL	Digitally Controlled Analogue Attenuator	212	+5dB to -31dB
ANSAH16	16 way Multiplexed Sample and Hold	595	Droop= 5mV/ms

MVA60000 PROCESSOR MACROCELL LIBRARY

There is an increasing trend towards the integration of processor blocks on ASIC devices. To meet these demands Zarlink Semiconductors has developed macrocells functionally equivalent to the popular 2901 Bit Slice Processor, and the industry standard 8085 8 bit Processor. Both processor cells have been designed in a minimum of silicon area, equivalent in gate array terms to a utilisation of better than 70%. The MI8085 cell also has an extended instruction set compared to the discrete version. Details are outlined below.

PROCESSOR MACROCELLS:

Cell Name	Description	Cell Count	Performance
MI2901	4 bit Bit Slice Processor equivalent to the 2901	1200	40MHz
MI8085	8 bit microprocessor core equivalent to the 8085	14000	15MHz

Testing of complex ASICs integrating these processor type macrocells can pose problems. Zarlink Semiconductor has already included BIST structures within the MI8085 macro to facilitate testing when embedded within an MVA60000 Megacell ASIC.

Development of new processor macrocells is continuing. Zarlink Semiconductor is currently designing a set of macros to emulate many of the functions of the processor and support devices used in a typical personal computer.

MVA60000 MACROCELLS FROM STANDARD PRODUCTS

Zarlink Semiconductors' leading edge CMOS standard products, in radio communications, data conversion, Digital Signal Processing, and other markets are designed using Megacell techniques, cells, and software. Many of these high technology products, which have been proven in volume production, are therefore compatible with Megacell ASIC designs. A customised 16 bit x 16 bit Pipelined Multiplier cell and a 256 x 16 bit RAM cell capable of 40MHz operation are examples from the DSP arena. Other examples are a 8 bit video speed DAC, and many of the new radio communications products now in design. Please contact your local Design Centre for further information on the integration of standard products into MVA60000 Megacell ASICs.

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