PLESSEY Semiconductors — CMOS

MV8860

DTMF DECODER

The MV8860 detects and decodes all 16 DTMF tone pairs. The device accepts the high group and low group square wave signals from a DTMF filter (MV8865) and provides a 3-state buffered 4-bit binary output. The clock signals are derived from an on-chip oscillator requiring only a single resistor and low cost crystal as external components. The MV8860 is implemented in CMOS technology and incorporates an on-chip regulator, providing low power operation and power supply flexibility.

The MV8860 is available in Plastic DIL (DP) and Ceramic DIL (DG), both with an operating temperature range of −40°C to +85°C.

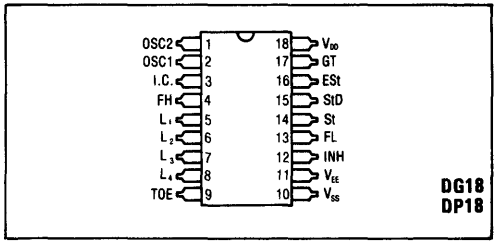


Fig.1 Pin connections (top view)

FEATURES

- 18 Pin DIL Package
- Central Office Quality Detection
- Excellent Voice Talk-Off
- Detect Times down to 20 ms
- Single Supply 5V, or 8 to 13 V Operation
- Latched 3-State Buffered Outputs
- Detects All 16 DTMF Combinations
- Uses Inexpensive 3.58 MHz Crystal
- Low Power CMOS Circuitry
- Adjustable Acquisition and Release Times
- Equivalent to MT8860X

APPLICATIONS

In DTMF Receivers For:

- End-to-end Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

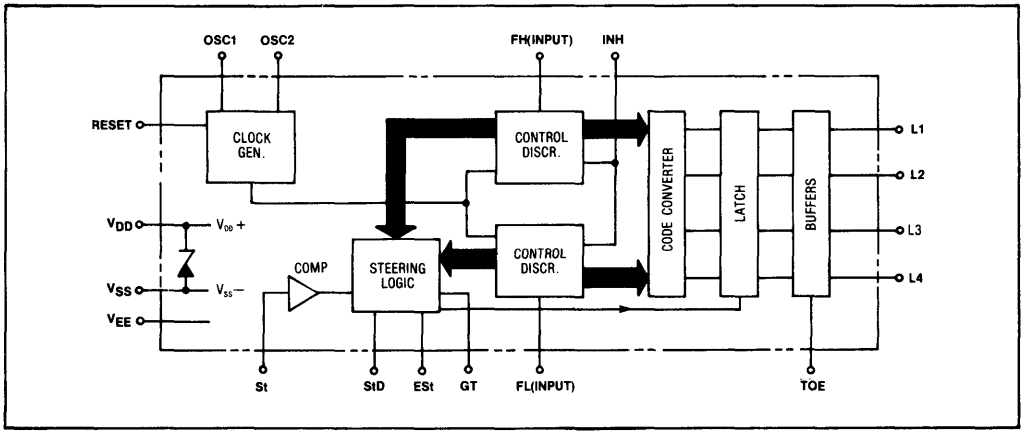


Fig.2 MV8860 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; f_c = 3.579545MHz
5 V operation: V_{DD} - V_{EE} = 5V, V_{SS} = V_{EE}, connections as Fig.5a
12 V operation: V_{DD} - V_{EE} = 12V, R_{SSEE} = 900Ω, connections as Fig.5b
Outputs not loaded
For input current parameters only, V_{IH} = V_{IHO} = V_{DD}, V_{IL} = V_{EE}, V_{ILO} = V_{SS}
All voltages referenced to V_{EE} unless otherwise noted.

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions
1	SUPPLY	Operating Supply Voltage (V_{DD} - V_{EE})		V_{DD}	4.75	5	5.25	V	Connections Fig. 5a
2					8		13	V	Connections Fig. 5b
3		Internal Logic Ground Voltage (V_{DD} - V_{SS})		V_{DDSS}	4.75		5.25	V	Connections Fig. 5a
4					6.0	6.5	7.5	V	Connections Fig. 5b
5		Operating Supply Current		I_{DD}		1.3	4	mA	5V
6						2.5	5	mA	12V V_{DD} - V_{SS} = 5.5V
7		Internal Logic Ground Pin Current		I_{SS}		5.5	6.7	mA	12V R_{SSEE} = 900Ω
8		Operating Power Consumption		P_O		6.5		mW	5V
9						66		mW	12V
10	INPUTS	High Level Input Voltage (All Inputs Except OSC1)		V_{IH}	3.5	4		V	5V
11					8.5	9		V	12V
12		Low Level Input Voltage (All Inputs Except OSC1)		V_{IL}		1	1.5	V	5V
13						3	3.5	V	12V
14		High Level Input Voltage OSC1		V_{IHO}	3.5	4.5		V	5V
15					10.5	11		V	12V
16		Low Level Input Voltage OSC1		V_{ILO}		0.5	1.5	V	5V Ref V_{SS}
17						0.5	1.5	V	12V Ref V_{SS}
18		Steering Input Threshold Voltage		V_{TSt}	2.04	2.27	2.5	V	5V
19					5.4	6.0	6.6	V	12V
20		Pull Down Sink Current (INH)		I_{IHI}	10	25	75	μA	5V
21					10	190	400	μA	12V
22		Pull Up Source Current (TOE)		I_{ILT}	2	7	45	μA	5V
23					10	55	250	μA	12V
24		Input High Leakage Current		I_{IH}		0.1	1.5	μA	5V or 12V
25		Input Low Leakage Current		I_{IL}		0.1	1.5	μA	
26	OUTPUTS	High Level Output Voltage (All Outputs Except OSC2)		V_{OH}	4.9			V	5V
27					11.9			V	12V
28		Low Level Output Voltage (All Outputs Except OSC2)		V_{OL}			0.1	V	5V
29							0.1	V	12V
30		High Level Output Voltage OSC2		V_{OHO}	4.9			V	5V
31					11.9			V	12V
32		Low Level Output Voltage OSC2		V_{OLO}			0.1	V	5V Ref V_{SS}
33							0.1	V	12V Ref V_{SS}
34		Output Drive Current (All Outputs Except OSC2)	P Channel Source	I_{OH}	0.4	0.6		mA	5V V_{OH} = 4.5V
35					0.5	0.8		mA	12V V_{OH} = 11.5V
36			N Channel Sink	I_{OL}	0.8	1.2		mA	5V V_{OL} = 0.5V
37					1.0	1.6		mA	12V V_{OL} = 0.5V
38		Output Drive Current OSC2	P Channel Source	I_{OHO}	90	120		μA	5V V_{OH} = 4.5V
39					90	120		μA	12V V_{OH} = 11.5V
40			N Channel Sink	I_{OLO}	100	160		μA	5V V_{OL} = 0.5V
41					100	160		μA	12V V_{SS} = 0.5V
42		Tristate Output Current (High Impedance State)	L_1 - L_4 = H	I_{OZ}		0.035	1.5	μA	5V Appl V_{OL} = 0V
43			L_1 - L_4 = L			0.1	1.5	μA	5V Appl V_{OH} = 5V
44			L_1 - L_4 = H			0.1	1.5	μA	12V Appl V_{OL} = 0V
45			L_1 - L_4 = L			0.3	1.5	μA	12V Appl V_{OH} = 12V

All "typical" parametric information is for design aid only, not guaranteed and not subject to production testing.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; V_{DD} = +5V; f_c = 3.579545MHz

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions
1	DETECTOR	Tone Frequency Deviation Accept		Δf_A			±2.5	% Nom.	
2		Tone Frequency Deviation Reject		Δf_R	±3.5			% Nom.	
3		Tone Present Detection Time		t_{DP}	6		10	ms	
4		Tone Absent Detection Time		t_{DA}	0.6	4	10	ms	
5		Guard Time (Adjustable)		$t_{GT(P\ or\ E)}$		20		ms	See Fig. 3
6		Time to Receive = (t_{DP} + t_{GTP})		t_{REC}	28	30	35	ms	Fig. 7a R = 300k Ω
7		Invalid Tone Duration (f_n of $t_{\overline{REC}}$)		$t_{\overline{REC}}$			20	ms	C = 0.1μF
8		Interdigit Pause = (t_{DA} + t_{GTA})		t_{ID}	30			ms	
9		Acceptable Drop Out (f_n of t_{ID})		t_{DO}			20	ms	
10	I/P	FL FH Input Transition Time		t_T			1.0	us	10% - 90% V_{DD}
11		Capacitance Any Input		C		5	7.5	pF	
12	OUTPUTS	Propogation Delay St to L_1 - L_4		t_{PL}		8	11	μs	V_{DD} 5V
13						8	11	μs	V_{DD} 12V
14		Propogation Delay St to StD		t_{PStD}		12	14	μs	V_{DD} 5V
15						12	14	μs	V_{DD} 12V
16		Propogation Delay TOE to L_1 - L_4	Enable	t_{PTE}		300		ns	V_{DD} 5V
17						200		ns	V_{DD} 12V
18			Disable	t_{PTD}		300		ns	V_{DD} 5V
19						200		ns	V_{DD} 12V
20	CLOCK	Crystal/Clock Frequency		f_c	3.5759	3.5795	3.5831	MHz	OSC 1 / OSC 2
21		Clock Input (OSC 1)	Rise Time	t_{LHCI}			110	ns	10% - 90% / Externally
22			Fall Time	t_{HLCI}			110	ns	V_{DD} = V_{SS} / Applied
23			Duty Cycle	DC_{CI}	40	50	60	%	/ Clock
24		Clock Output (OSC 2)	Capacitive Load	C_{LOC}			30	pF	With Clock Drive to OSC 1
25				C_{LOX}				nF	Sinusoidal Output With Crystal

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max	
V_{DD} - V_{EE}			16	V
V_{DD} - V_{SS} (Low Impedance Supply)			5.5	V
Voltage on any pin except OSC1 OSC2		V_{EE} −0.3	V_{DD} +0.3	V
Voltage OSC1 OSC2		V_{SS} −0.3	V_{DD} +0.3	V
Max current at any pin (except V_{DD} & V_{EE})			10	mA
Operating Temperature	DP/DG Package	−40	+85	°C
Storage Temperature	DG Package	−55	+175	°C
	DP Package	−55	+125	°C

		Max
Power Dissipation	DG Package*	1000mW
	DP Package**	450mW

* Derate 16mW/°C above 75°C
** Derate 6.3mW/°C above 25°C
All leads soldered to PC board.

Original Tone Character		TOE	L4	L3	L2	L1
	X	L	Z	Z	Z	Z
DR	1	H	L	L	L	H
	2	H	L	L	H	L
	3	H	L	L	H	H
	4	H	L	H	L	L
	5	H	L	H	L	H
	6	H	L	H	H	L
	7	H	L	H	H	H
	8	H	H	L	L	L
	9	H	H	L	L	H
	0	H	H	L	H	L
D	*	H	H	L	H	H
	#	H	H	H	L	L
	A	H	H	H	L	H
	B	H	H	H	H	L
	C	H	H	H	H	H
	D	H	L	L	L	L

(a) Output coding

Detected Character	INH	ESt
None	Ø	L
X	L	H
DR	H	H
D	H	L

(b) Inhibit function

ESt	St	GT	StD*
L	L	L	L
H	L	Z	L
L	H	Z	H
H	H	H	H

(c) Steering

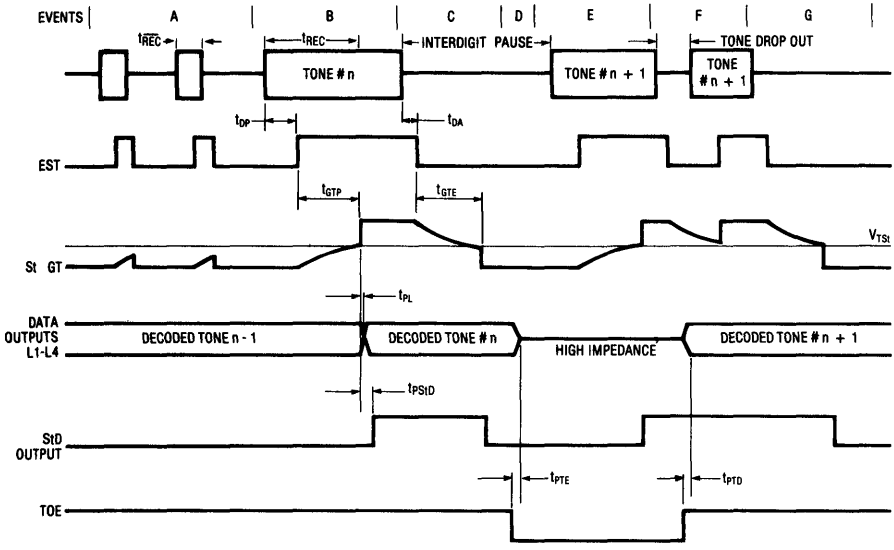
* DELAYED WRT St.

FOR THE PURPOSE OF THESE TABLES CONSIDER:

$V_{St} < V_{TSt}$ LOGIC LOW (L)
$V_{St} > V_{TSt}$ LOGIC HIGH (H)

H = LOGIC HIGH L = LOGIC LOW
Ø = "DON'T CARE" LOGIC HIGH OR LOW
Z = HIGH IMPEDANCE X = ANY CHARACTER

Table 1 Coding data



A) SHORT TONE BURSTS : DETECTED, TONE DURATION IS INVALID
B) TONE # n IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
C) END OF TONE # n IS DETECTED AND VALIDATED.
D) 3 STAGE OUTPUTS DISABLED (HIGH IMPEDANCE).
E) TONE # n + 1 IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
F) TRISTATE OUTPUTS ARE ENABLED. ACCEPTABLE DROP OUT OF TONE # n + 1 DOES NOT REGISTER AT OUTPUTS.
G) END OF TONE # n + 1 IS DETECTED AND VALIDATED.

Fig.3 Timing diagram

PIN FUNCTIONS

Pin	Name	Description	
1	OSC2	CLOCK OUTPUT	3.58MHz crystal with parallel 5MΩ resistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
2	OSC1	CLOCK INPUT	
3	IC	Internal connection for testing only (reset) Note 1	
4	FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter	
5	L1	Data Outputs. 3 state buffered Provides 4 Bit binary word corresponding to the tone pair decoded, when enabled by TOE See Table 1 for state table	
6	L2		
7	L3		
8	L4		
9	TOE	3 state output enable input. Logic high on this input enables outputs L1-L4. Internal pull up	
10	V_{SS}	Internal logic ground. For V_{DD} - V_{EE} = 5V V_{SS} connected to V_{EE}. For V_{DD} - V_{EE} > 8V, V_{SS} connected via resistor to V_{EE} see Fig. 5	
11	V_{EE}	Negative power supply. External logic ground	
12	INH	Inhibit input. Logic high inhibits detection of tones representing characters #, *, A, B, C, D. Internal pull down	
13	FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter	
14	St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs Voltage< V_{TSt} on this pin frees the device to accept a new tone pair. See Table 1c and Functional Description	
15	StD	Delayed Steering Output. Flags when a valid tone pair has been received. Presents logic high when output latch updated. When St voltage exceeds V_{TSt}. Returns to logic low when St voltage falls below V_{TSt}	
16	ESt	Early Steering Output. Presents a logic high immediately the digital algorithm detects a recognisable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low	
17	GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt (See Table 1c)	
18	V_{DD}	Positive power supply	

Note 1: Must be left open circuit.

OPERATING NOTES

The MV8860 is a CMOS Digital DTMF detector and decoder. Used in conjunction with a suitable DTMF filter (MV8865) it can detect and decode all 16 Standard DTMF tone pairs, accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MV8860 must be preceded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sinewave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The high group and low group rectangular waves are applied to the MV8860s FH and FL inputs, respectively. The MV8865 DTMF filter provides these functions.

Within the MV8860 the FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators, Fig.2) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both high group and low group signals have been simultaneously detected, a flag ESt (Logic High), is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig.3) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of 'tone absent' before a valid received tone is recognised as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig.7a) is charged via resistor R from ESt which a DTMF tone pair is detected. After a period t_{GTP}, V_C exceeds the St input threshold voltage V_{TSt}, setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (Table 1c) and timing diagram (Fig.3).

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents a 4 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs L_1 to L_4. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_C (Fig.7a) falling below V_{TSt}.

Increasing the 'time to receive' (t_{REC}) tends to further improve talk off performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal to noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig.7.

When L_1 to L_4 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The MV8860 may be operated from either a 5V or 8 to 13V supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig.5.

When using the MV8860 with the MV8865 DTMF filter it is only necessary to use the MV8865 crystal oscillator (see Fig.6). When using the higher supply voltage range the MV8865 OSC2 output should be capacitively coupled to the MV8860 OSC1 input as shown in Fig.6.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves talk off due to the reduced number of detectable tones.

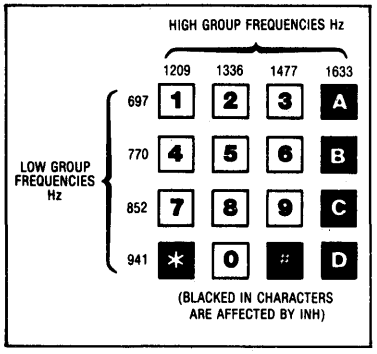


Fig.4 DTMF matrix, indicating character-tone pair correspondence

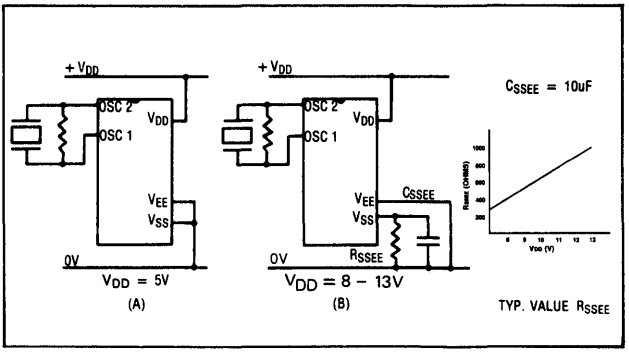
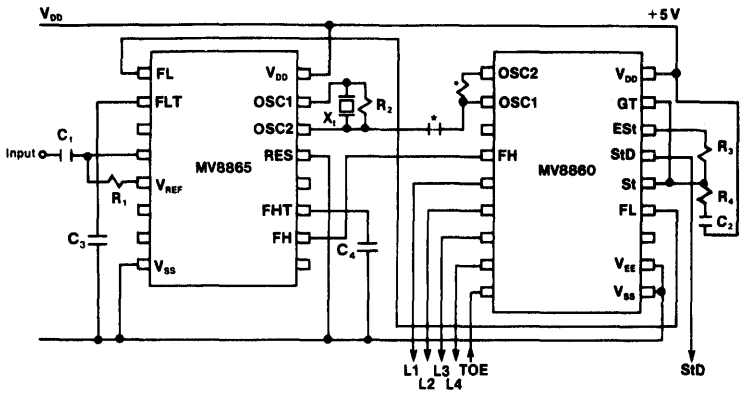


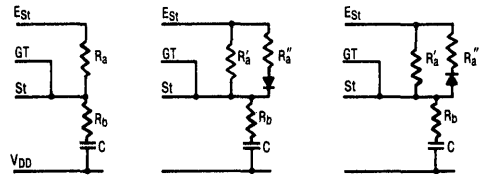
Fig.5 Power supply connection options



TYPICAL PERFORMANCE

DYNAMIC RANGE	30dB
TWIST	± 10dB
ACC. S/N RATIO	14dB
T_{REC}	30ms

Fig.6 Single-ended input receiver using the MV8865 (5 V operation)



$T_{GTP} = T_{GTE}$ (A)

$T_{GTP} < T_{GTE}$ (B)

$T_{GTP} > T_{GTE}$ (C)

$$T_{GTP} = C\,(R_a + R_b)\,\mathrm{Log_n}\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{DD} - V_{TSt}}\right)$$

$$T_{GTE} = C\,(R_a + R_b)\,\mathrm{Log_n}\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{TSt}}\right)$$

FOR V_{OHESt}, V_{OLESt} Symetric About $V_{TSt} = \frac{1}{2} V_{DD}$

WITH $R_b < 0.1\ R_a$ $\qquad R_b \geq V_{DD} - V_{EE}$ KΩ

$$R_b < 0.1\left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$$

A) $T_{GTP} = T_{GTE} \triangleq 0.69\ R_a\ C\left(1 - \frac{R_b}{2\,R_a}\right)$

B) T_{GTP} } $\triangleq 0.69\ C\left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$

C) T_{GTE} }

B) T_{GTE} }

C) T_{GTP} } $\triangleq 0.69\ R_a'\ C$

Fig.7 Guard time adjustment