MV6601C Datasheet

MVD-6601-04-DS-EN
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Revision History

Date	Version	Description
2007/07/05	0.1	Initial Draft
2007/07/06	0.2	Added Boot Up Sequence, Overview, Group Connection Diagram. Modified Tables, Pin assignment, Pin Description
2007/07/09	0.3	Remove Section 1.3 Advance Feature List, Modify Pin Description, Makes viewable graphics
2007/07/11	0.4	Edit Acronym and Abbreviations
2008/05/10	0.6	Update
2008/05/12	0.7	Update

1. General Description

The MV6601C™ multi-core processor is a versatile high-performance, low-power, high integration system-on-chip (SoC) targeted at multimedia enabled cell phones, personal media players (PMP), multimedia clients, and devices where low power multimedia features are valued.

The MV6601C SoC features a multimedia processing engine that removes the need for additional external DSP chip. With built-in TFT LCD controller, MV6601C is designed to support directly driver LCD module with a 18bit RGB666 LCD controller and diver, and support both 8bit parallel camera input and output interface conforming to YCbCr 4:2:2 format. With built-in Audio DAC & Amplifier, MV6601C is designed to support both digital and analog audio output, support digital audio protocol - I2S, and can output analog audio directly or with headphone amplifier.

The MV6601C also including various host processor interface (I2C/SPI/UART/LCM-Like), NOR Flash interface, I^2C & SPI serial interfaces, PWM output port, the MV6601C is an ideal choice for system integrators seeking to maximize performance and minimize system cost.

The MV6601C stacked with 8M bytes SDRAM in single package.

The MV6601C chip also supports RISC instruction set which enables user customization. Designed for minimal integration effort for multimedia resolutions, maximum performance at low power, the device only needs to run at speed no more than 150 MHz so the overall power dissipation is less than 250mW. In addition, MV6601C is integrated with on-chip memory controllers and flexible input/output options and can run a variety of operating systems.

2. Feature

2.1 Processor

- Integrated RISC core supports 32-bit architecture and instruction set
- Multi-core “Class-DSP” for multimedia processors

2.3 Multimedia Decoder

- Support various video format: MPEG1/2/4, H.264, AVS, RM/RMVB, AVI
- Support various video solution QVGA/CIF/QQVGA/QCIF @ 30fps
- Support various audio format: MP3/AAC/AAC+

2.4 Video Interface

- Support LCD display base on RGB565 /RGB666 format
- Support directly driver the TFT color LCD module
- YUV 4:2:2 outputs for emulate as camera sensor connect to host
- YUV 4:2:2 input for connect to camera sensor module
- Support multi-resolution with video scalar
- Support overlay and OSD with alpha blending
- Support hue and gamma correct

2.5 Audio Interface

- Support digital audio interface I2S input & output for external audio codec.
- Support stereo analog audio output with built-in audio DAC
- Support directly stereo headphone output with built-in 24mW amplifier

2.6 Host Interface

- Support various serial interfaces (slave to host) I2C, SPI, UART
- Support various parallel interface (slave to host) LCM-like 8-bit memory bus interface

2.8 Peripheral Interface

- Most of pins in MV6601C can act as GPIO
- Serial peripheral (master) interface: I2C, SPI
- 4 channel PWM outputs

2.9 Memory Controller

- 4 channel independent Multi-priority based DMA
- Support Self-boot NOR Flash size up to 8M bytes

2.10Stack SDRAM

- Stack with 8M bytes SDRAM in single package
- Stack SDRAM speed up to PC133

2.11Power and Package

- Operating voltages
  - Core: 1.2V
  - PLL: 1.2V (Sensitive)
  - Host interface: 1.8V ~ 3.3V
  - General I/O: 1.8V ~ 3.3V
  - SDRAM: 2.3V ~ 2.7V
  - Analog: 2.7V ~ 3.6V
- Multiple power domains and gated clocks
- Power modes: Active and Shutdown
- 0.13 µm CMOS
- Package: 0.5mm pitch, 10mmX10mmX1.2mm, 208 ball TFBGA

3. Block Diagram

The following figure shows the functional block diagram.

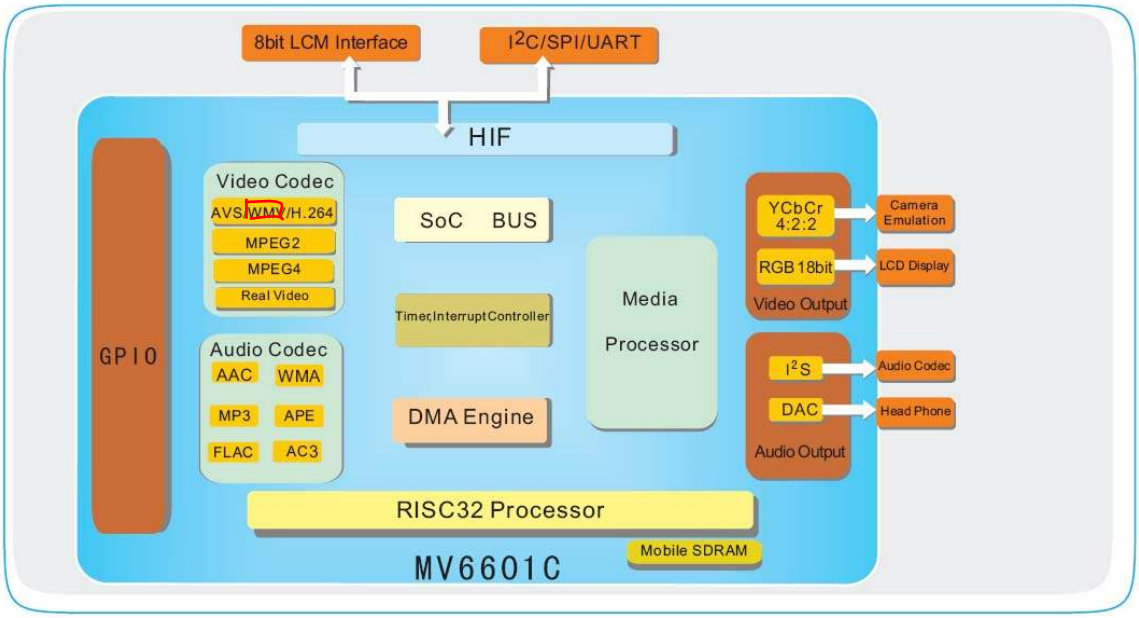


Figure 1 Functional block diagram

4. Functional Description

4.1 32-bit RISC Core

MV6601C integrated a general purpose RISC processor, which provides a versatile high integrate, high-performance, low-power SoC. It also supports 32-bit architecture and instruction set. The cache is a four ways associative type with separate 16K bytes instruction and 16K bytes data. Our general purpose RISC processor supports essential instructions and features which are found in industry-standard RISC processors such as ARM and PPC.

4.2 Multi-core "Class-DSP"

4.2.1 RICE Processor Description

The Mavrix's 32-bit RISC Processor named RICE (RISC Instruction Core Engine) is designed to be used as the backbone for all Mavrix's Class Oriented Pipeline Processors. Therefore, the RICE was architected from inception with power, area, and performance in mind. The focus is to make the RICE nimble but complete. Architectural simplicity not only leads to small area and low power, it also facilitates firmware coding and future enhancements. The RICE has the essential instructions and features that are found in industry-standard RISC processors such as ARM and MIPS, with the coprocessor support needed for the Mavrix's class specific instructions.

4.2.2 Matrix Processor Description

The Mavrix M2 Matrix Processor is an innovative Multimedia Processing core designed to accelerate the processing of popular media compression/decompression schemes. The M2's unique Matrix data path and instruction set allows for efficient processing of H.264/AVC, JPEG/MPEG, RM/RMVB in a fully programmable core.

4.3 DMA Controller

The Global DMA is a general purpose direct memory access controller. It is in charge of moving data between different internal modules and external devices. The global DMA servers the following DMA clients: peripheral devices, DRAM, Video processor.
There are 4 independent channels, one per source and destination pair. Each source and destination address is programmable, and data endian is programmable conversion during transfer. Interrupt generation on transfer complete.

4.4 Host Interface

The MV6601C provides various host interfaces which allows an external master to connect to MV6601C. By the software level, a pair of software API will be implemented inside the MV6601C SoC and the host processor (We call the software run at the host processor as "HIF" supplied by Mavrix). Commands from host will be sent to MV6601C, explained and executed by MV6601C, and also information inside MV6601C will be obtained by the host.
Briefly, it is the main interface which exchanges data by MV6601C to help our customer to integrate whole MV6601C function. Media streaming is also send to MV6601C for viewing by the host interface.
The MV6601C supports multiple types of serial host interface and one parallel interface.
The CPU interprets the host commands, performs corresponding operations and then sends the status back to the host processor.
Optionally, MV6601C also output one level-trigger signal to interrupt the host. (INTR)
The MV6601C supports the following types of host interfaces:

- I2C (slave)
- SPI (slave, mode 0/1/2/3)
- UART
- LCM-like 8-bit I80 interface

Note: The data field may contain multiple bytes when necessary.

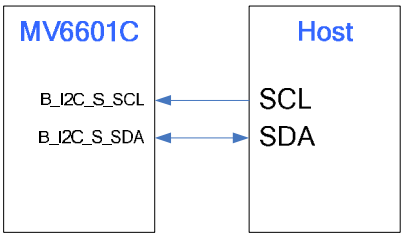
Note: Multiple bytes data is transfer by Little-Endian that is low byte transferred first.

Note: Since MV6601C RISC is based on 32bit access, all data bytes after the addresses are treated as 4-chained bytes. That is, the API in the host processor will group 4 consecutive bytes access together as a single 32bit access.

4.4.1. I2C Interface

The MV6601C acted as an I²C slave. Through the IO-Trap configuration, alternative I²C slave addresses can be selected (Default address is 0x65).

The speed of I²C interface in MV6601C is up to 1.5Mbps.



The following diagram shows the access timing:

Write Timing: To write data to MV6601C, only one I²C cycle is needed, both the command and the contents are send to the bus.

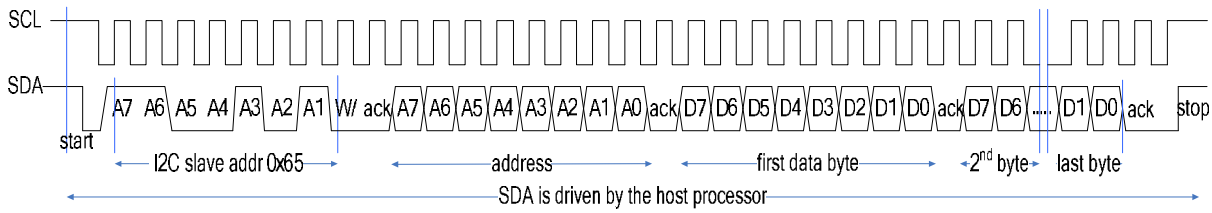


Figure 2 I²C write timing – multiple bytes access

Read Timing: To read from MV6601C, two I²C cycles are needed. First cycle writes the register address to be accessed from, and second cycle read the contents.

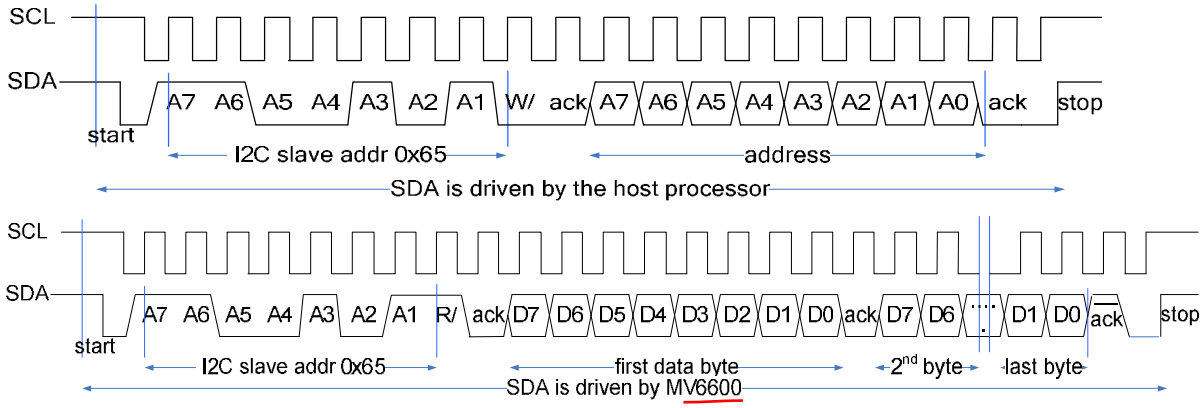


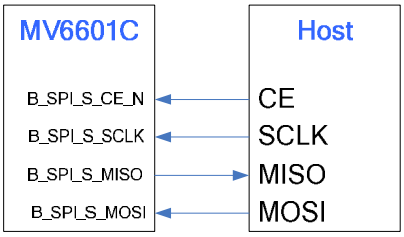
Figure 3 I²C read timing

Note: When write data to slave, the ACK handshake is always needed and driven by the I²C slave device - MV6601C. When read data from MV6601C, the ACK handshake should be driven by the host.

4.4.2. SPI Interface

The “Serial Peripheral Interface” (SPI) is a synchronous four wires serial link used to connect to MV6601C. The two serial data lines with “Master out, Slave in” (MOSI) or “Master In, Slave out” (MISO) signals. MV6601C supports all four clocking modes for data exchange, and the serial clock frequency is up to 24MHz. Each clock cycle shifts data out and data in; the clock doesn’t cycle except when there is data to shift. An IO-Trap option defines the access clocking mode.

The access mode can be read or write, depending on the bit-7 of address transfer. Multiple data bytes can be transferred, following the address.



The following diagrams illustrate the timing of MV6601C access via the SPI serial interface.

SPI mode-0 (clock stops at logic 0 when idle, rising edge latch data)

Write Cycle Timing

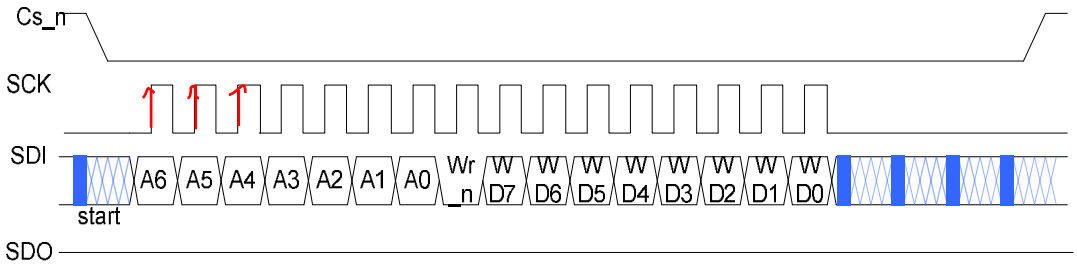


Figure 4 SPI mode-0 write timing

Read Cycle Timing

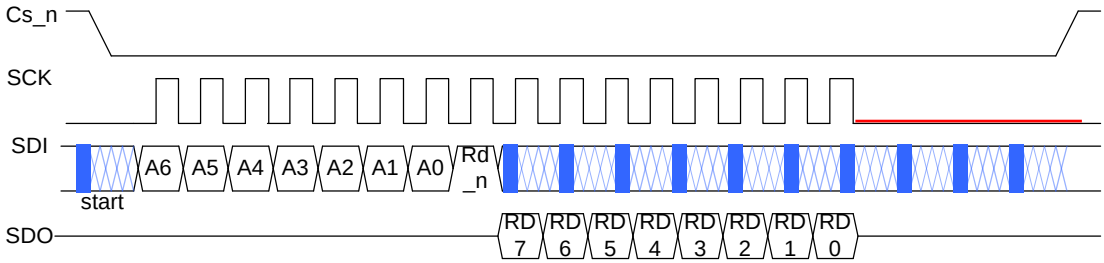


Figure 5 SPI mode-0 read timing

SPI mode-1 (clock stops at logic 0 when idle, falling edge latch data)

Write Cycle Timing

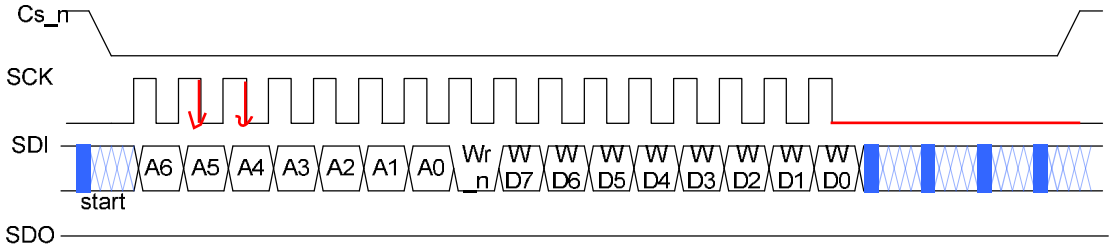


Figure 6 SPI mode-1 write timing

Read Cycle Timing

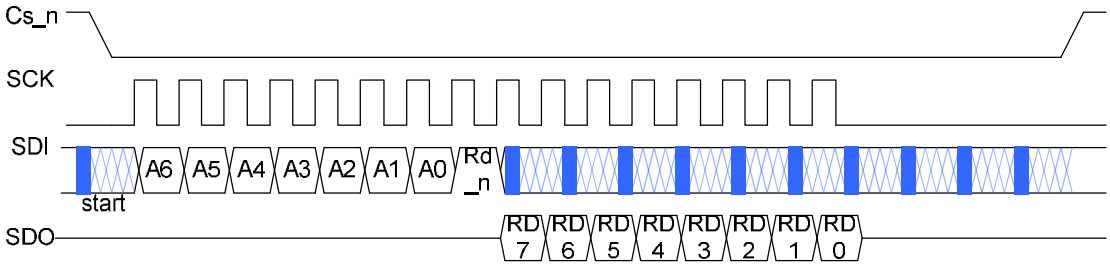


Figure 7 SPI mode-1 read timing

SPI mode-2 (clock stops at logic 1 when idle, falling edge latch data)

Write Cycle Timing

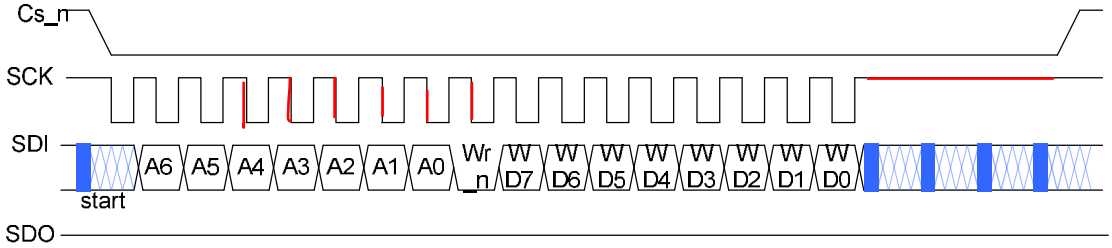


Figure 8 SPI mode-2 write timing

Read Cycle Timing

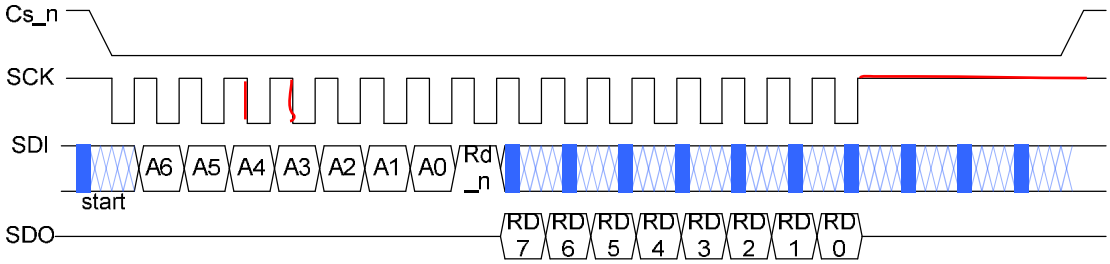


Figure 9 SPI mode-2 read timing

SPI mode-3 (clock stops at logic 1 when idle, rising edge latch data)

Write Cycle Timing

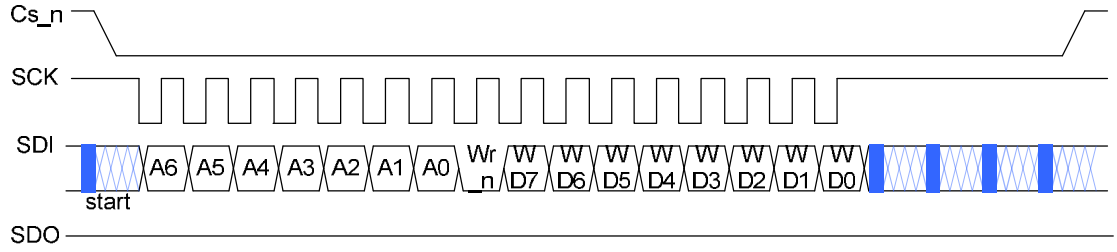


Figure 10 SPI mode-3 write timing

Read Cycle Timing

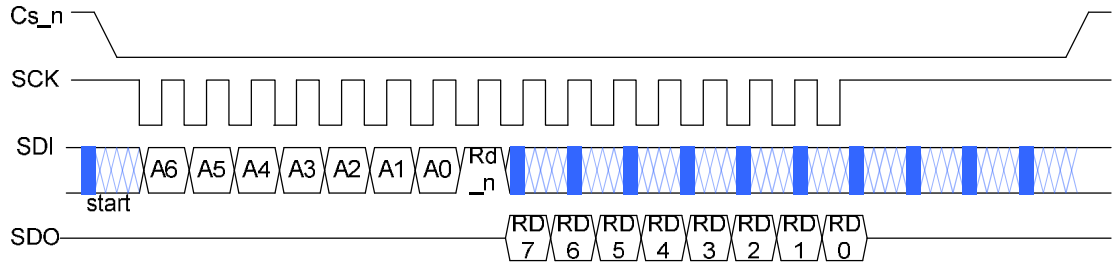


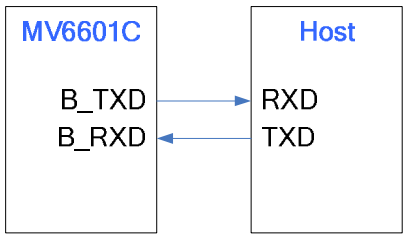
Figure 11 SPI mode-3 write timing

4.4.3. UART Interface

MV6601C provide an UART serial interface connect to host. MV6601C need 9-bit data transfer protocol. The last bit “bit-8” defines whether the transfer is a command or a data. All data transfer must be followed by one command transfer.

The command transfer defines the access address and mode. The access mode can be read or write, depending on eighth bit “bit-7” of the command. The write transfer can send multiple data followed by one command. The read transfer send the read command at first, after MV6601C received the read command, it would transfer following data back to host.

The default baud rate is 9600bps after hardware reset, and The baud rates can be programmed from 1200bps to 1.5Mbps. The time interval between each read byte is also programmable from 0 to 255 bits.



The following diagrams show the timing.

Write Cycle Timing

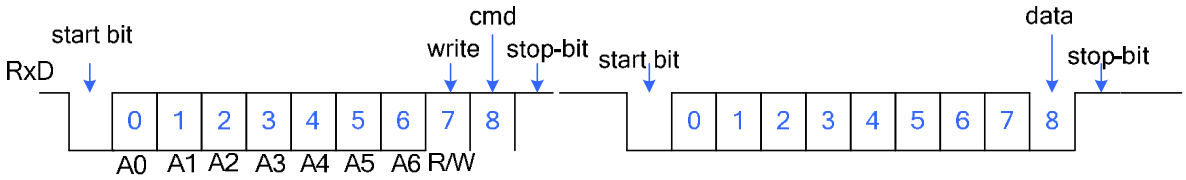


Figure 12 UART write timing

Read Cycle Timing

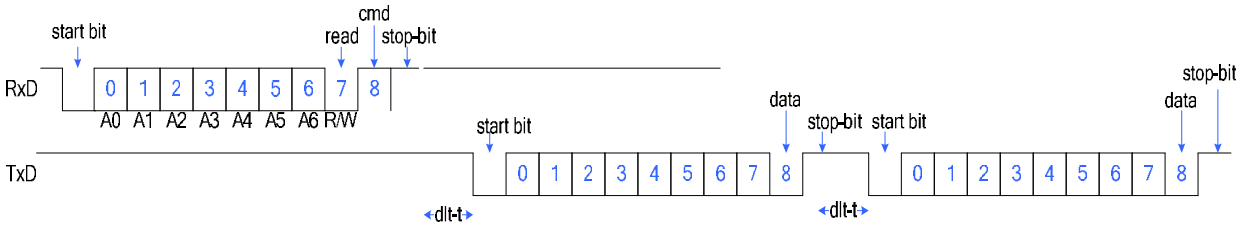


Figure 13 UART read timing

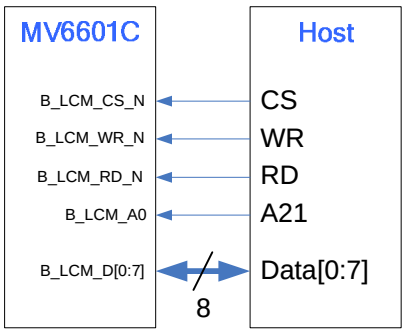
Note: The (dlt-t) represents the internal time between each read data transfer.

4.4.4. LCM-Like 8-bit I80 Interface

The MV6601C also provides an 8bit width parallel interface, which is a memory bus and standard RAM interface, and which could significantly improve the data throughput. The interface is compatible to the LCD Module (LCM) interface meeting the I80 interface protocol, so we call it LCM-Like.

The command is send when A0 is low, and the data is send/receive when A0 is high. Due to MV6601C access in 32bit width, so four clock cycles complete one transfer, and it uses LSB data format transfer.

The CS desert indicates one transfer beginning, so must always keep CS low in one transfer duration time.



CAUTION: The MV6601C LCM-Like interface is 8bit width, but the host may be 16bit or 32 bit width system. In both case, it should put the address at the MSB of command, may fill zero at begin bytes.

Write Cycle Timing

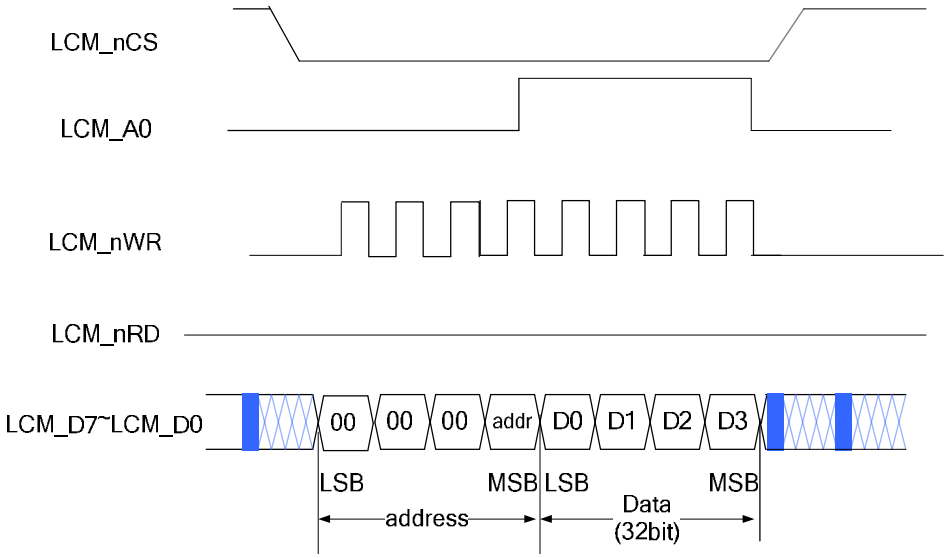


Figure 14 LCM I80 interface write timing

Read Cycle Timing

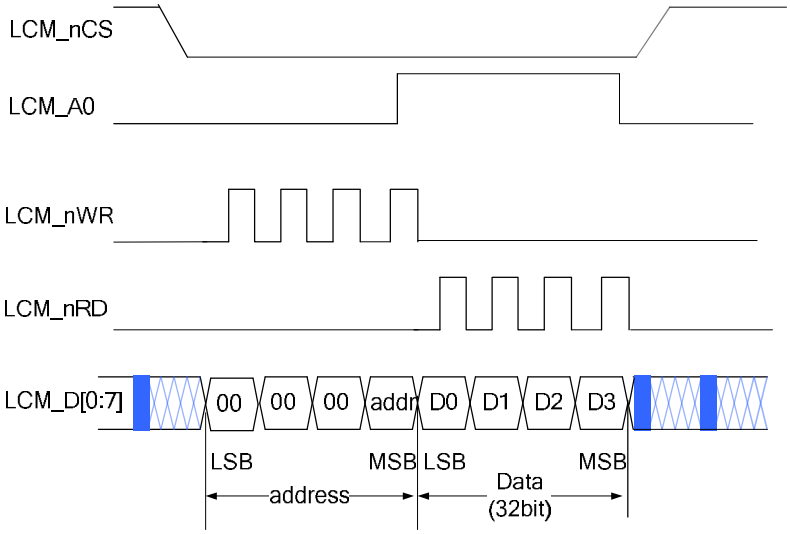


Figure 15 LCM I80-series interface read timing

4.5. Peripheral Interface

In addition, MV6601C also supports multiple types of peripheral interfaces to control and communication to other peripheral devices.

MV6601C supports the following types of peripheral interfaces:

- 1 I2C master interface

- 1 SPI master interface
- 4 PWM output
- GPIO

4.5.1 I²C

To communicate with peripheral devices, MV6601C will act as an I2C master. The interface timing and read/write protocol are the same as the interface used by the host interface. Please refer to the host interface section for detail.

4.5.2 SPI

Similar to the I2C master interface, MV6601C also supports a SPI serial interface in master mode. The MV6601C supports all four SPI clocking modes. Please refer to the host interface section for detail.

4.5.3 PWM

PWM (Pulse Width Modulation) block is a powerful interface for controlling analogy circuits with a processor's digital outputs. PWM is a way of digitally encoding analogy signal levels. There are four PWM output pins in the MV6601C.

PWM Timing Diagram

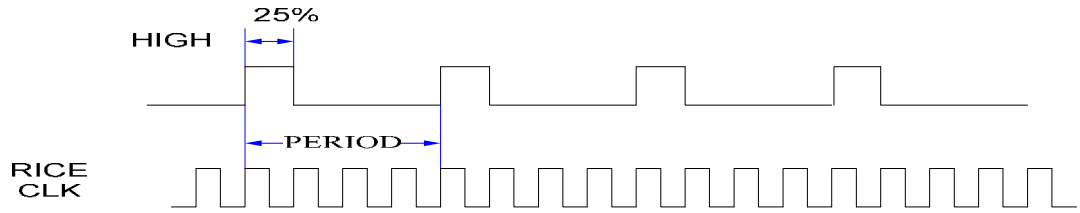


Figure 16 WM timing diagram

4.6. Display Interface

The Display Interface controller block is designed to output images to an LCD panel display or to the Camera sensor input of Host processor. And it also has a camera sensor input port that can receive image data from the sensor and put into memory via DMA, or directly bypass all sensor signals to output port.
This interface have rich feature which including Video scalar, Display Overlay, 16/18bit RGB output, 8bit YUV output, GAMMA control, Alpha blending.

4.7.1 Display Scalar

MV6601C implements a video scalar in its display path, Depending on the register setting, the scalar can handle quarter Macro Block (SMB) inputs (Media streaming

playback). The input to the display and scaling block is assumed to be DRAM.
In the LCD parallel display modes, the pixel format is selectable as YCbCr 4:2:2 or YCbCr 4:2:0, and the pixel placement within DRAM is assumed to be planar. That is, Y, Cb, and Cr are all separately placed in the source memory instead of interleaved together. The scalar allows for integer decimation by 2. In both horizontal or vertical direction and an independently controlled fractional horizontal and vertical scale down to 2X. Both the Camera Emulation output and the LCD parallel output can be scaled.
Please note that since the scalar hardware sometimes needs to handle SMB inputs, a built-in buffer is required. To reduce the overall buffer size, the width of input frame to Scalar block should be restricted to be no larger than 800 pixels (Y being the worst case).

4.7.2 Image Control

The MV6601C can easily adjust image parameters, including Hue saturation and Gamma. The Gamma adjustment uses the 16-element color palette.
The overlay images can be mixed with graphic image through Alpha Blending mode, thus to form applications such as transparent menu.

4.7.3 Display Overlay

To allow for users to draw menus icons over the video in the display output, MV6601C implements a graphics overlay sub-block. The display overlay merges inputs from a separate DRAM location (a graphics buffer) to the output of the Color-Space-Conversion sub block. It is up to the firmware to define the size of the graphic buffer as well as the “overlay area”. The overlay region is defined as a single region with starting line number as well as ending line number. (Only the y-direction can be specified, the x-direction is assumed to be entire row)

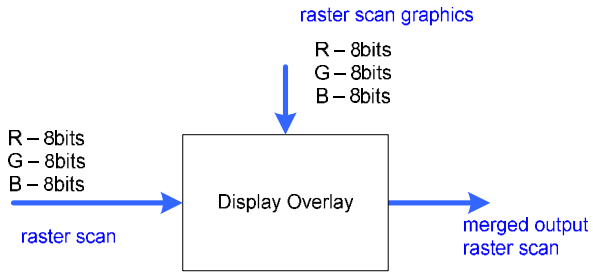


Figure 17 Display overlay block diagram

4.7.4 Camera Emulation Output

The MV6601C supports a camera emulation output interface. This interface can be used by the host processor to obtain media graphic data from MV6601C for display by the host processor. The camera emulation output port supports the Camera YUV 4:2:2 display data outputs, QVGA 320x240 at 30fps.
The LCM_MCLK is used as master clock supplied by the host (or outside oscillator) to

MV6601C. The MV6601C will generate an internal pixel clock (LCD_PCLK) based on the MCLK. Since the frequency of the master clock is normally multiples of the pixel-clock, the MV6601C utilizes an internal divider for the internal pixel clock generation and synchronization to the input clock. In addition, LCD_VS and LCD_HS provide the necessary vertical sync (frame valid) and horizontal sync (line valid) signals to the host. Display data is streamed to the host via the 8bit YUV bus which supports YCbCr 4:2:2 formats. The data output can either be in the sequence of Y0-Cb-Y1-Cr or Cb-Y0-Cr-Y1 format. The following figures illustrate the interconnection examples between the MV6601C and a host processor supporting camera-interfaces.

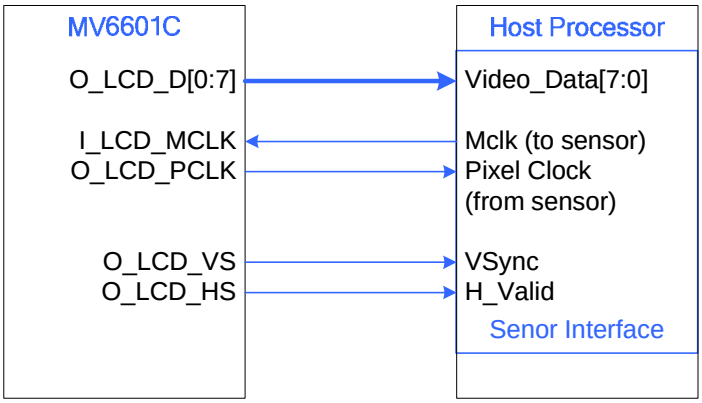


Figure 18 Sensor mode interface (VSync + H_Valid)

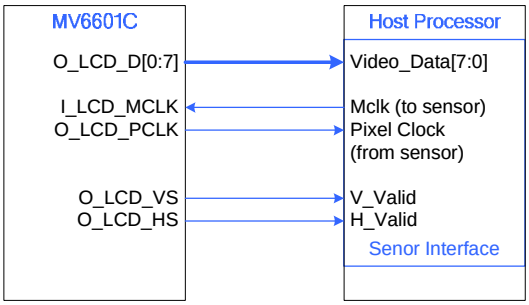


Figure 19 Sensor mode interface (V_Valid + H_Valid)

Data Transfer Timing

This sub-section describes the timings in Sensor Mode: (VSync + H_Valid) & (V_Valid + H_Valid) for the video data transfer between MV6600 and the host processor.

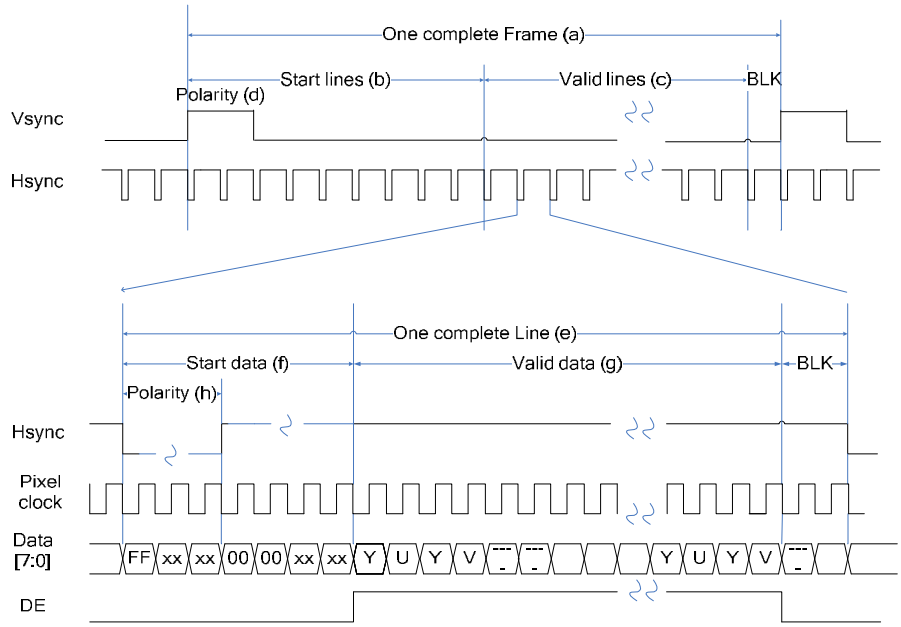


Figure 20 Sensor mode interface YUV data transfer timing (VSync + H_Valid)

Symbol	Name	Unit	Value	Range
a	VS Period	Line	250	0~4096
b	Start blank lines	Line	10	0~1024
c	Valid lines	Line	240	0~1024
d	Active phase	Line	2	0~4096
e	HS Period	Dot	800	0~4096
f	Start blank dots	Dot	140	0~1024
g	Valid dots	Dot	640	0~1024
h	Active phase	Dot	40	0~4096

Note: During this particular sensor mode, polarity for VSync and H_Valid, are programmable as either active high or active low. Pulse width for the vertical synchronization is programmable, and both horizontal blanking and vertical blanking are programmable. In addition, the number of dummy pixels at the beginning of each line and the number of dummy lines (will show up as a delay before H_Valid goes active after VSync) at the beginning of each frame are programmable as well.

4.7.5 LCD Display Controller

The MV6601C provides a parallel interface to driver the LCD panels. The LCD display interface is based on 18/16 bit RGB format. The RGB protocol uses vertical and horizontal synchronization signals (VS and HS) to construct timing of a display frame. Either 18bit or 16bit RGB data is sent to the LCD per clock. Max frame rate is 60 fps.

The configuration for the LCD interface is summarized below:

- 18-bit RGB interface – RGB666 format

- 16-bit RGB interface – RGB565 format

Note: If the LCD panel is 16-bit RGB 565 format, LCD_R0 and LCD_B0 are open drain.

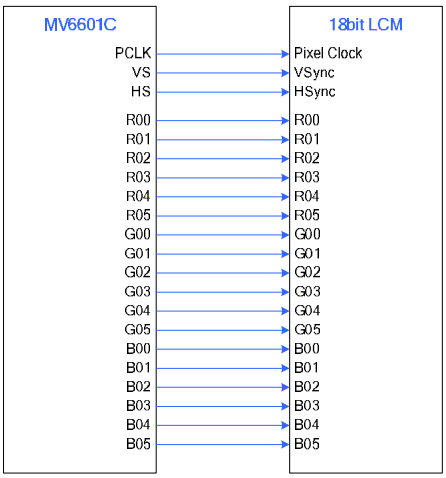


Figure 21 LCD display interface (18-bit RGB666)

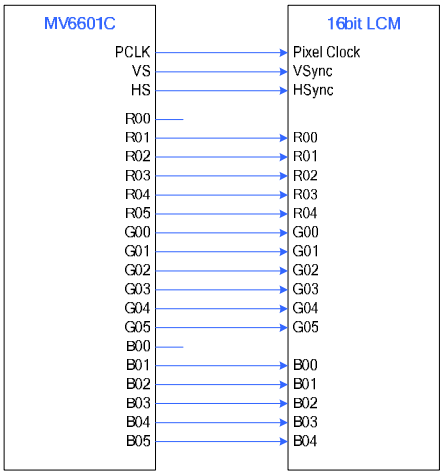


Figure 22 LCD display interface (16-bit RGB565)

Data Transfer Timing

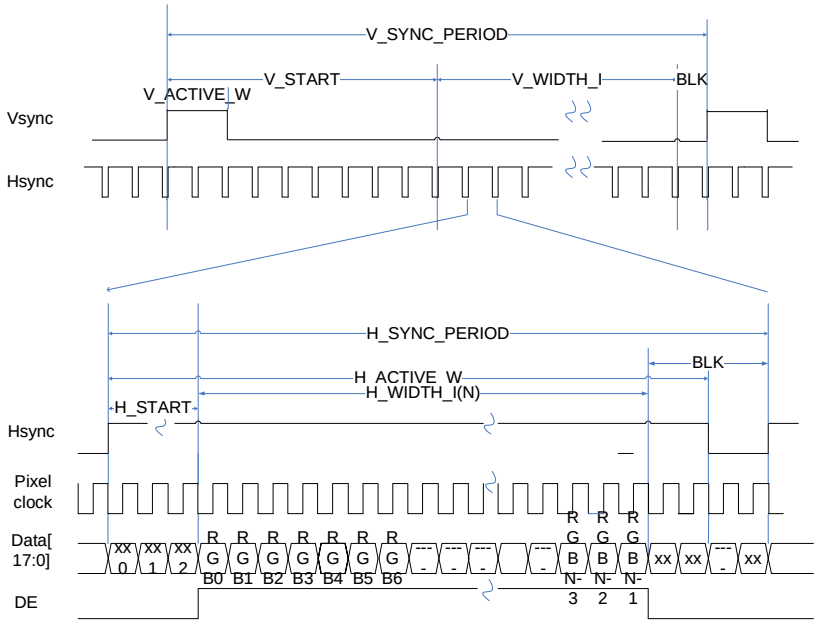


Figure 23 LCD (18bit/16bit) transfer mode – (VSync + HSync)

Note: When in LCD data transfer mode, polarity for vertical synchronization (VSync) and horizontal synchronization (HSync) are programmable as either active high or active low. Pulse width for the VSync and the pulse width for the HSync are both programmable. Both horizontal blanking time and vertical blanking time are also programmable. And finally, the number of dummy pixels at the beginning of each line and the number of dummy lines at the beginning of each frame are programmable.

4.7. Audio Interface

The Audio Interface controller block is designed to output audio data to an internal or external audio DAC, base on I2S protocol. And it also has a digital audio data input port that can receive audio data from external device and put into memory via DMA, or directly bypass all I2S signals to output port.
The built-in stereo audio DAC can output audio in analog (Line out), and headphone output through built-in headphone amplifier, so it can directly driver stereo headphone.

4.8.1 I²S Audio Interface

The following diagram shows the connection between the MV6601C and an external audio DAC in the playback mode application (video clip playback, audio playback). The MV6601C provides the master I2S clock and the I2S DAC that are controlled via the I2C or SPI interface in master mode.

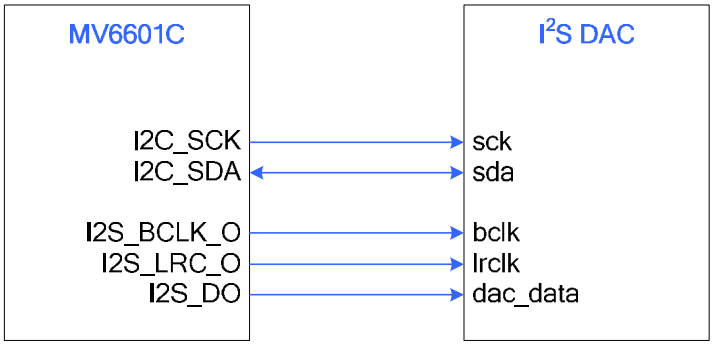


Figure 24 Connection between MV6601C and an external DAC

I2S Controller Timing Diagram

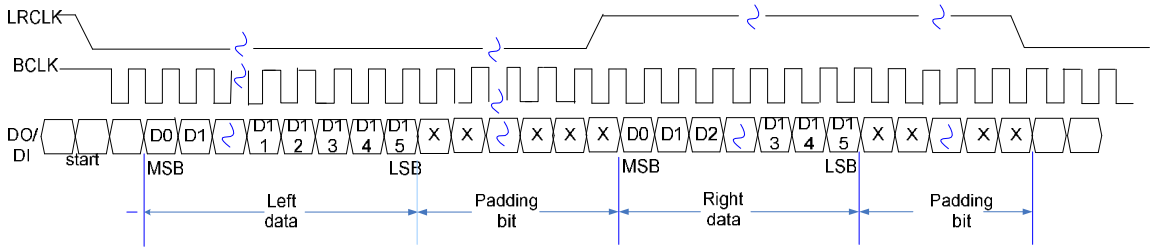


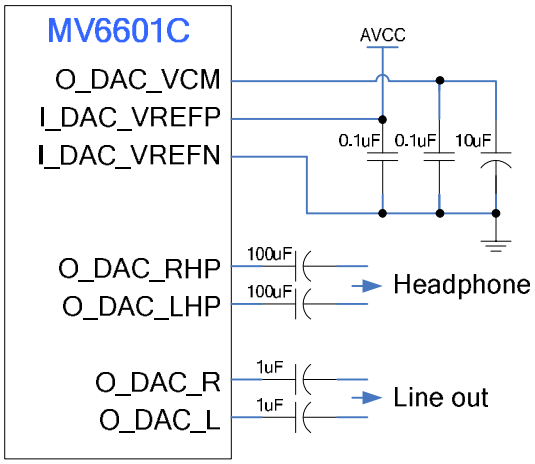
Figure 25 I2S controller read/write timing

4.8.2 Internal Audio DAC

MV6601C integrates a low-cost stereo audio DAC with single-ended analog voltage input and output. The DAC employ anti-pop and de-emphasis filter. It provides power down mode, which works on the DAC simultaneously; customer can control the headphone power and DAC power separately. It also supports digital loop back.

The following list is the features of the internal audio DAC:

- Supports 16/18/20/24-bit input format
- Analog supply range: 2.7 V ~ 3.6 V
- 90 dB SNR sigma-delta DAC @ 48 kHz A-weighted
- Supports 8 kHz – 192 kHz sampling rate
- 90 dB DR sigma-delta DAC @ 48 kHz A-weighted
- Digital interpolation filter
- Stereo line outputs
- De-emphasis filter supports 44.1 kHz, 32 kHz and 48 kHz



4.8. Memory Interface

The MV6601C SoC contains two external memory controllers, one for SDRAM and one for static device (NOR Flash).

4.9.1 NOR Flash Controller

The MV6601C supports flash and boot memory controller type. The flash interface has 23 address pins, so it can support 8M single chip flash. The data width bus is 8bit.

For reading data from the flash, when CE and OE are low and WE is high, data stored at the memory location determined by the address pin is asserted on the outputs. The outputs are put in the high impedance state whenever CE or OE is high. This dual-line control gives designers flexibility to extend the flash capacity.

When using flash address pin number less than 23, example a flash only has 19 pins. Then we must connect flash to MV6601C address pin A0-A18.

Read Timing Diagram

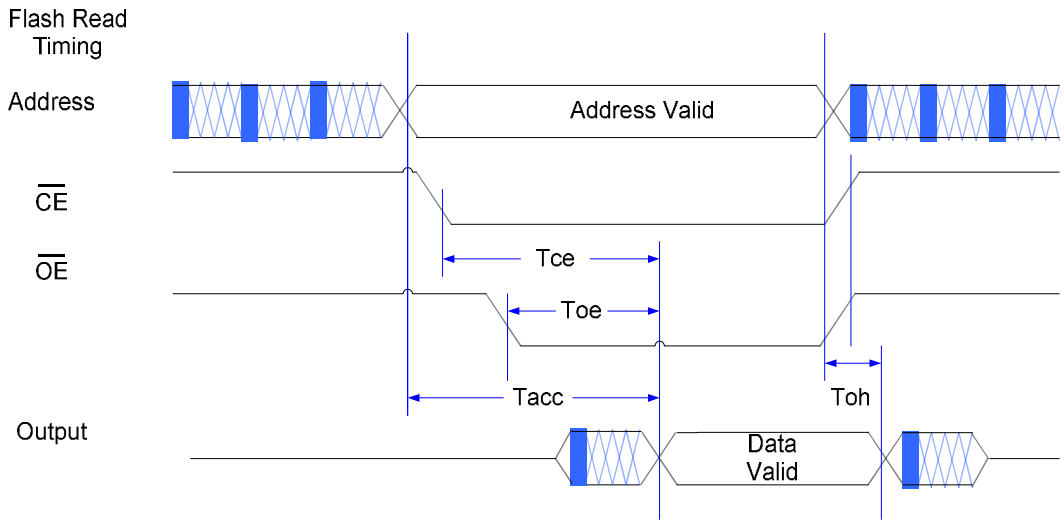


Figure 26 Flash read timing

Program Timing Diagram

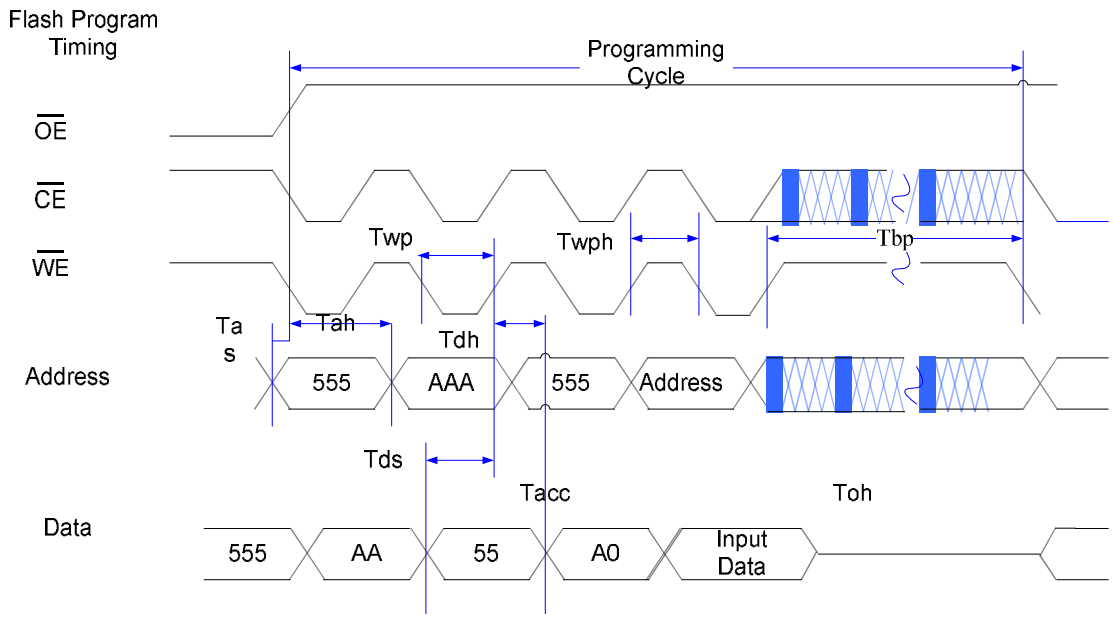


Figure 27 Flash program timing

4.9. GPIO

4.10.1 General Purpose Input/Output Interface

Most pins on the MV6601C board can act as GPIO. There are 105 GPIO pins.

Each GPIO_ENB bit is reset to 1'b1, except for those GPIO pins that are shared with the host interfaces, JTAG, EJAG, and FLASH, which are powered on to functional mode. All other GPIO-able pins power on to GPIO functional mode.

5. Signal Description

5.1 Pins Description

No.	Pin Name	Dir.	Description	Default	Memo
System (6 pins)					
1	I_RST_N	I(*1)	External reset	(*2)	(*3)
2	I_TEST	I	0: Normal chip operation.	-	
3	B_OSC_IO	OSC	Crystal output or external clock input	-	
4	I_OSC_I	OSC	Crystal input	-	
5	I_OSC_Z	I	0: Use internal oscillator with crystal 1: Use external clock input	IN	
6	I_OSC_F	I	0: Crystal frequency is 12~24MHz 1: Crystal frequency is 24~48MHz	IN	
Host Interface (20 pins)					
1	B_I2C_S_SCL	B	I2C clock pin	FUNC	
2	B_I2C_S_SDA	B	I2C data pin	FUNC	
3	B_SPI_S_CE_N	B	SPI chip enable pin	FUNC	
4	B_SPI_S_SCLK	B	SPI clock pin	FUNC	
5	B_SPI_S_MISO	B	SPI master in slave out	FUNC	
6	B_SPI_S_MOSI	B	SPI master out slave in	FUNC	
7	B_TXD	B	UART transfer data out	FUNC	
8	B_RXD	B	UART receive data in	FUNC	
9	B_LCM_CS_N	B	LCM chip select	FUNC	
10	B_LCM_WR_N	B	LCM write clock	FUNC	
11	B_LCM_RD_N	B	LCM read clock	FUNC	
12	B_LCM_A0	B	LCM address select	FUNC	
13	B_LCM_D0	B	LCM data 0	FUNC	
14	B_LCM_D1	B	LCM data 1	FUNC	
15	B_LCM_D2	B	LCM data 2	FUNC	
16	B_LCM_D3	B	LCM data 3	FUNC	
17	B_LCM_D4	B	LCM data 4	FUNC	
18	B_LCM_D5	B	LCM data 5	FUNC	
19	B_LCM_D6	B	LCM data 6	FUNC	
20	B_LCM_D7	B	LCM data 7	FUNC	
LCD Controller Interface (23 pins)					
			RGB mode / YUV mode		

1	B_LCD_DE	B	LCD data enable pin	YUV data enable pin	IN	
2	I_LCD_MCLK	I	LCD main clock input	YUV main clock input	IN	
3	O_LCD_PCLK	O	LCD pixel clock	YUV pixel clock	IN	
4	O_LCD_HS	O	LCD Hsync clock	YUV Hsync clock	IN	
5	O_LCD_VS	O	LCD Vsync clock	YUV Vsync clock	IN	
6	O_LCD_D0	O	RED data 0	YUV0	IN	
7	O_LCD_D1	O	RED data 1	YUV1	IN	
8	O_LCD_D2	O	RED data 2	YUV2	IN	
9	O_LCD_D3	O	RED data 3	YUV3	IN	
10	O_LCD_D4	O	RED data 4	YUV4	IN	
11	O_LCD_D5	O	RED data 5	YUV5	IN	
12	O_LCD_D6	O	GREEN data 0	YUV6	IN	
13	O_LCD_D7	O	GREEN data 1	YUV7	IN	
14	B_LCD_D8	B	GREEN data 2		IN	
15	B_LCD_D9	B	GREEN data 3		IN	
16	B_LCD_D10	B	GREEN data 4		IN	
17	B_LCD_D11	B	GREEN data 5		IN	
18	B_LCD_D12	B	BLUE data 0		IN	
19	B_LCD_D13	B	BLUE data 1		IN	
20	B_LCD_D14	B	BLUE data 2		IN	
21	B_LCD_D15	B	BLUE data 3		IN	
22	B_LCD_D16	B	BLUE data 4		IN	
23	B_LCD_D17	B	BLUE data 5		IN	
Camera Interface (12 pins)						
1	O_C_MCLK	O	Sensor main clock output		IN	
2	I_C_PCLK	I	Sensor pixel clock input		IN	
3	B_C_HS	B	Sensor Hsync pin		IN	
4	B_C_VS	B	Sensor Vsync pin		IN	
5	B_C_YUV0	B	Sensor YUV 0		IN	
6	B_C_YUV1	B	Sensor YUV 1		IN	
7	B_C_YUV2	B	Sensor YUV 2		IN	
8	B_C_YUV3	B	Sensor YUV 3		IN	
9	B_C_YUV4	B	Sensor YUV 4		IN	
10	B_C_YUV5	B	Sensor YUV 5		IN	
11	B_C_YUV6	B	Sensor YUV 6		IN	
12	B_C_YUV7	B	Sensor YUV 7		IN	
Audio Interface (14 pins)						

1	B_I2S_I_CLK	B	I2S input main clock	IN	
2	B_I2S_I_LRCK	B	I2S input LeftRight clock	IN	
3	B_I2S_I_DATA	B	I2S input data signal	IN	
4	B_I2S_O_MCLK	B	I2S output clock	IN	
5	B_I2S_O_CLK	B	I2S output main clock	IN	
6	B_I2S_O_LRCK	B	I2S output LeftRight clock	IN	
7	B_I2S_O_DATA	B	I2S output data signal	IN	
8	O_DAC_VCM	O	DAC common mode voltage	-	
9	I_DAC_VREFP	I	DAC positive reference voltage	-	
10	I_DAC_VREFN	I	DAC negative reference voltage	-	
11	O_DAC_LHP	AO	Left headphone sound output	-	
12	O_DAC_RHP	AO	Right headphone sound output	-	
13	O_DAC_R	AO	Stereo sound right output	-	
14	O_DAC_L	AO	Stereo sound left output	-	
ADC Interface (11 pins)					
1	B_CLK_RST	B	Clock module reset control pin	IN	
2	B_CLK_PWDN	B	Clock module power down control pin	IN	
3	O_CLK_OUT	B	Clock module output	OUT	
4	O_ADC_VCM	AO	ADC common mode voltage	-	
5	O_ADC_VREF	AO	ADC reference voltage	-	
6	O_ADC_VRP	AO	ADC positive reference voltage	-	
7	O_ADC_VRN	AO	ADC negative reference voltage	-	
8	I_ADC_QP	AI	Q channel + input	-	
9	I_ADC_DN	AI	Q channel – input	-	
10	I_ADC_IP	AI	I channel + input	-	
11	I_ADC_IN	AI	I channel – input	-	
Peripheral Interface (12 pins)					
1	B_PWM0	B	Pulse width modulator output 0	IN	
2	B_PWM1	B	Pulse width modulator output 1	IN	
3	B_PWM2	B	Pulse width modulator output 2	IN	
4	B_PWM3	B	Pulse width modulator output 3	IN	
5	B_I2C_M_SCL	B	(Master) I2C clock pin	IN	
6	B_I2C_M_SDA	B	(Master) I2C data pin	IN	
7	B_SPI_M_CE_N	B	(Master) SPI chip enable	IN	
8	B_SPI_M_SCLK	B	(Master) SPI clock	IN	
9	B_SPI_M_MISO	B	(Master) SPI master in slave out	IN	
10	B_SPI_M_MOSI	B	(Master) SPI master out slave in	IN	
11	B_GPIO_0	B	GPIO 0	IN	
12	B_GPIO_1	B	GPIO 1	IN	

NOR Flash Controller (35 pins)					
1	B_NOR_RST_N	B	NOR Flash reset pin	FUNC	
2	B_NOR_CE_N	B	NOR Flash chip enable pin	FUNC	
3	B_NOR_WE_N	B	NOR Flash write enable pin	FUNC	
4	B_NOR_OE_N	B	NOR Flash out put enable pin	FUNC	
5	B_NOR_D0	B	NOR Flash data 0	FUNC	
6	B_NOR_D1	B	NOR Flash data 1	FUNC	
7	B_NOR_D2	B	NOR Flash data 2	FUNC	
8	B_NOR_D3	B	NOR Flash data 3	FUNC	
9	B_NOR_D4	B	NOR Flash data 4	FUNC	
10	B_NOR_D5	B	NOR Flash data 5	FUNC	
11	B_NOR_D6	B	NOR Flash data 6	FUNC	
12	B_NOR_D7	B	NOR Flash data 7	FUNC	
13	B_NOR_A0	B	NOR Flash address 0	FUNC	
14	B_NOR_A1	B	NOR Flash address 1	FUNC	
15	B_NOR_A2	B	NOR Flash address 2	FUNC	
16	B_NOR_A3	B	NOR Flash address 3	FUNC	
17	B_NOR_A4	B	NOR Flash address 4	FUNC	
18	B_NOR_A5	B	NOR Flash address 5	FUNC	
19	B_NOR_A6	B	NOR Flash address 6	FUNC	
20	B_NOR_A7	B	NOR Flash address 7	FUNC	
21	B_NOR_A8	B	NOR Flash address 8	FUNC	
22	B_NOR_A9	B	NOR Flash address 9	FUNC	
23	B_NOR_A10	B	NOR Flash address 10	FUNC	
24	B_NOR_A11	B	NOR Flash address 11	FUNC	
25	B_NOR_A12	B	NOR Flash address 12	FUNC	
26	B_NOR_A13	B	NOR Flash address 13	FUNC	
27	B_NOR_A14	B	NOR Flash address 14	FUNC	
28	B_NOR_A15	B	NOR Flash address 15	FUNC	
29	B_NOR_A16	B	NOR Flash address 16	FUNC	
30	B_NOR_A17	B	NOR Flash address 17	FUNC	
31	B_NOR_A18	B	NOR Flash address 18	FUNC	
32	B_NOR_A19	B	NOR Flash address 19	FUNC	
33	B_NOR_A20	B	NOR Flash address 20	FUNC	
34	B_NOR_A21	B	NOR Flash address 21	FUNC	
35	B_NOR_A22	B	NOR Flash address 22	FUNC	
Test Interface (21 pins)					
			JTAG	GPIO	
1	B_TCK	B	JTAG test clock	FUNC	

2	B_TDI	B	JTAG test data in		FUNC	
3	B_TDO	B	JTAG test data out		FUNC	
4	B_TMS	B	JTAG test mode select		FUNC	
5	B_EJ_TCK	B	EJTAG test clock		FUNC	
6	B_EJ_TDI	B	EJTAG test data in		FUNC	
7	B_EJ_TDO	B	EJTAG test data out		FUNC	
8	B_EJ_TMS	B	EJTAG test mode select		FUNC	
9	B_EJ_TRST_N	B	EJTAG test reset		FUNC	
Power / Ground (43 pins)						
1	VCCK	PG	Voltage supply of core		-	
2	VCCK	PG	Voltage supply of core		-	
3	VCCK	PG	Voltage supply of core		-	
4	VCCK	PG	Voltage supply of core		-	
5	VCCK	PG	Voltage supply of core		-	
6	VCCK	PG	Voltage supply of core		-	
7	VCCK	PG	Voltage supply of core		-	
8	VCCK	PG	Voltage supply of core		-	
9	VCCK	PG	Voltage supply of core		-	
10	VCCK	PG	Voltage supply of core		-	
11	VCCK	PG	Voltage supply of core		-	
12	GNDK	PG	Ground of core		-	
13	GNDK	PG	Ground of core		-	
14	GNDK	PG	Ground of core		-	
15	GNDK	PG	Ground of core		-	
16	GNDK	PG	Ground of core		-	
17	GNDK	PG	Ground of core		-	
18	GNDK	PG	Ground of core		-	
19	GNDK	PG	Ground of core		-	
20	GNDK	PG	Ground of core		-	
21	GNDK	PG	Ground of core		-	
22	GNDK	PG	Ground of core		-	
23	VCCIO_BB	PG	Voltage supply of host interface		-	
24	VCCIO_BB	PG	Voltage supply of host interface		-	
25	VCCIO_BB	PG	Voltage supply of host interface		-	
26	VCCIO_SPI	PG	Voltage supply of SPI interface		-	
27	VCCIO_C	PG	Voltage supply of camera interface		-	
28	VCCIO_CLK	PG	Voltage supply of clock controller		-	
29	VCCIO_PWM	PG	Voltage supply of PWM		-	
30	VCCIO_NOR	PG	Voltage supply of NOR Flash controller		-	

31	VCCIO_NOR	PG	Voltage supply of NOR Flash controller	-	
32	GNDIO	PG	Ground of IO	-	
33	GNDIO	PG	Ground of IO	-	
34	GNDIO	PG	Ground of IO	-	
35	GNDIO	PG	Ground of IO	-	
36	GNDIO	PG	Ground of IO	-	
37	GNDIO	PG	Ground of IO	-	
38	GNDIO	PG	Ground of IO	-	
39	GNDIO	PG	Ground of IO	-	
40	GNDIO	PG	Ground of IO	-	
41	VCC3IO	PG	Voltage supply of I/O	-	
42	GND3IO	PG	Ground of IO	-	
43	VCCIO_LCD	PG	Voltage supply of LCD controller	-	
44	VCCIO_LCD	PG	Voltage supply of LCD controller	-	
45	GNDIO_LCD	PG	Ground of LCD controller	-	
46	GNDIO_LCD	PG	Ground of LCD controller	-	
47	VCCIO_SD	PG	Voltage supply of SDRAM controller	-	
48	VCCIO_SD	PG	Voltage supply of SDRAM controller	-	
49	VCCIO_SD	PG	Voltage supply of SDRAM controller	-	
50	VCCIO_SD	PG	Voltage supply of SDRAM controller	-	
51	VCCIO_SD	PG	Voltage supply of SDRAM controller	-	
52	GNDIO_SD	PG	Ground of SDRAM controller	-	
53	GNDIO_SD	PG	Ground of SDRAM controller	-	
54	GNDIO_SD	PG	Ground of SDRAM controller	-	
55	GNDIO_SD	PG	Ground of SDRAM controller	-	
56	GNDIO_SD	PG	Ground of SDRAM controller	-	
57	VCC12A_PLL	PG	Voltage supply of PLL	-	
58	GNDA_PLL	PG	Ground of PLL	-	
59	VCC12A_SDPLL	PG	Voltage supply of SDRAM PLL	-	
60	GNDA_SDPLL	PG	Ground of SDRAM PLL	-	
61	VCC12A_ADC	PG	Voltage supply of internal ADC	-	
62	GNDA_ADC	PG	Ground of internal ADC	-	
63	VCC3A_DAC	PG	Voltage supply of internal DAC	-	
64	GNDA_DAC	PG	Ground of internal DAC	-	
65	VCC3A_DACHP	PG	Voltage supply of Headphone DAC	-	
66	GNDA_DACHP	PG	Ground of Headphone DAC	-	

Note: (*1) “I” Only input pin; “O” Only output pin; “B” bidirectional pin; “A” Analog pin; “PG” Power or Ground pin.

(*2) “FUNC” means power on to functional mode; “IN” means power on to input GPIO mode;

(*3) TBD

5.2 IO-Trap Setting

MV6601C can be set to different configurations when powered on. The configuration setting is configure by connect pull-up or pull-down resistors to some pins.

Pin	Name	Description	Note
B_NOR_D[0:1]	Xtal[0:1]	Crystal frequency selection Xtal[2], Xtal[1], Xtal[0] 3'b000: 24.576 MHz 3'b001: 19.2 MHz 3'b010: 16.384 MHz 3'b011: 13 MHz 3'b100: 48 MHz 3'b101: 36 MHz 3'b110: 30 MHz 3'b111: 26 MHz	IO_Trap[0:1]
B_NOR_D[2:3]	SpiMode[0:1]	SPI Mode setting, SpiMode[1], SpiMode[0] 2'b00: Mode 0 2'b01: Mode 1 2'b10: Mode 2 2'b11: Mode 3	IO_Trap[2:3]
B_NOR_D4	BootSource	1'b0: Boot from extern NOR Flash 1'b1: Boot from SDRAM	IO_Trap[4]
B_NOR_D5	I2CAddress	HIF I2C device address setting 1'b0: 0x56 1'b1: 0x65	IO_Trap[5]
B_NOR_D6	Xtal[2]	The another crystal selection pin	IO_Trap[6]
B_NOR_D7	PllBypass	1'b0: Bypass PLL use oscillator clock as PLL output clock 1'b1: No Bypass	IO_Trap[7]
I_OSC_Z	OscType	1'b0: Use internal oscillator with Crystal 1'b1: Use external oscillator clock input	OSC_Trap[0]
I_OSC_F	OscFreq	Frequency selection if use internal oscillator with Crystal, 1'b0: 12 ~ 24MHz 1'b1: 24 ~ 42MHz	OSC_Trap[1]

5.3 Boot-up Sequence

The MV6601C supports two types of boot source.

- **Host-Boot**: The host processor initiated and downloading code from host, then booting from SDRAM.
- **Flash-Boot**: It will auto boot from Flash.

Both boot-up sequences need some pre-strap setup, such as select crystal or oscillator as clock input, PLL configuration, Host interface configuration, and configure MV6601C RISC processor as auto run mode or no-auto run mode. Refer to IO-Trap Setting for detail.

5.3.1 Host-Boot Sequence

The IO-Trap option should be configured as no-auto run mode.

After MV6601C power on and reset have been done. The Host should program the necessary clock register, and initiate the setting of SDRAM. Then SDRAM is ready for access, host can download the firmware into SDRAM via the burst access mode through the host interface (I2C, SPI, LCM, etc.). It is the software's responsibility to ensure the program data integrity after the download (Looking for HW checksum logic or at least word count logic). Once the download is verified, the host processor should soft reset MV6601C RISC to run the firmware, then check response from MV6601C to ensure firmware running correctly. Now MV6601C is ready for work.

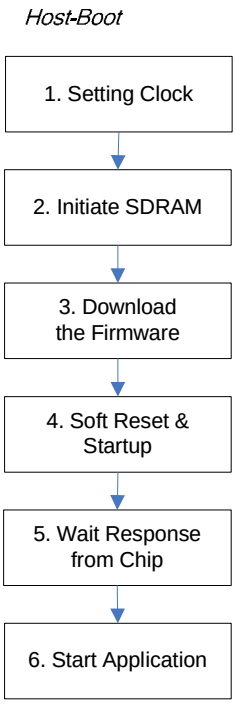


Figure 28 Host-boot sequence

5.3.2 Flash-Boot Sequence

The IO-Trap option should be configured as auto run mode.

After power-on-reset been done, the MV6601C will auto run from flash in default. Then the host processor must check response from MV6601C to ensure firmware running correctly,. Now MV6601C is ready for work.

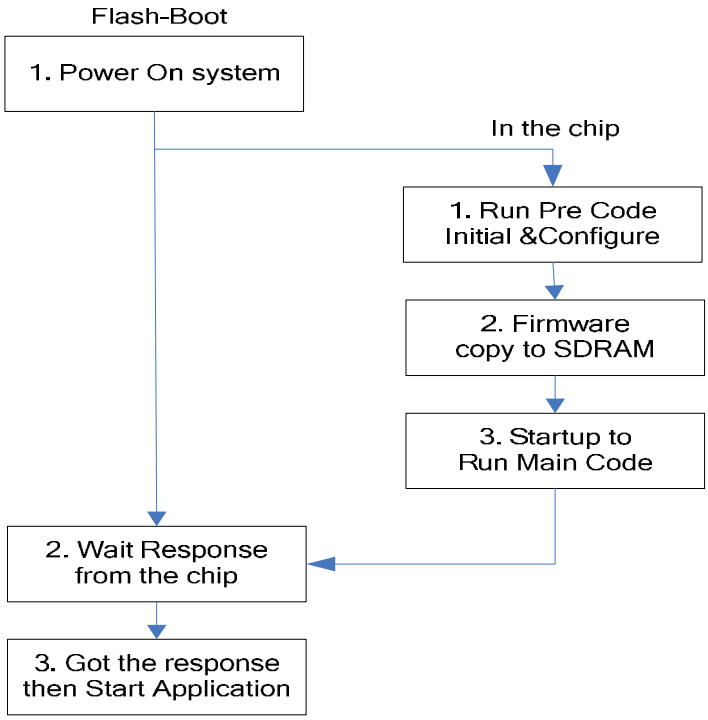


Figure 29 Flash-boot sequence

6. Electrical Characteristic

6.1 Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	VT	-0.5 to 4.6	V
Supply Voltage relative to VSS	VDD	-0.5 to 4.6	V
Operating Temperature	TOPT	-10 to +70	℃
Storage Temperature	TSTG	-55 to +125	℃

6.2 Operating Condition

	Min.	Typ.	Max.	Unit
Internal	1.1	1.2	1.3	V
PLL	1.1	1.2	1.3	V
SDRAM	2.3	2.5	2.7	V
Host Interface	1.8	3.0	3.3	V
GPIO	1.8	3.0	3.3	V
Analog (Interval DAC)	2.7	3.0	3.6	V
Internal core	-	96	160	MHz
Integrated RISC core	-	96	250	MHz

6.3 DC Characteristic

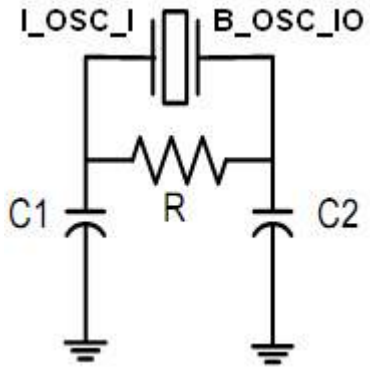
TA=25℃

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCK	Core operating voltage	1.1	1.2	1.3	V
VCC3IO VCCIO_BB VCCIO_SPI VCCIO_CLK VCCIO_C VCCIO_PWM VCCIO_NOR VCCIO_LCD	I/O operation voltage	1.8	3.0	3.3	V
VCCIO_SD	SDRAM controller operation voltage	2.3	2.5	2.7	V
VCC12A_PLL VCC12A_SDPLL	PLL operation voltage	1.1	1.2	1.3	V
VCC12A_ADC	Internal ADC operation voltage	1.1	1.2	1.3	V
VCC3A_DAC VCC3A_DACHP	Internal DAC operation voltage	2.7	3.0	3.6	V
IDD	II/O (Standby)	-	TBD	TBD	mA
	ICore (Standby)	-	TBD	TBD	mA
IDD	II/O (Bypass)	-	TBD	TBD	mA
	ICore (Bypass)	-	TBD	TBD	mA
IDD	II/O (Idle)	-	TBD	TBD	mA
	ICore (Idle)	-	TBD	TBD	mA
IDD	II/O (Play AVI)	-	TBD	TBD	mA
	ICore (Play AVI)	-	TBD	TBD	mA
IDD	II/O (Play RMVB)	-	TBD	TBD	mA
	ICore (Play RMVB)	-	TBD	TBD	mA

Note: 1. The current is average value, and connect to 16.384MHz Crystal as clock input.
2. The operation power: II/O: The IO current; ICore: The Core logic current
3. The maximum condition is measure by 1.2V core power, 3.0V IO power, 3.3V DAC power, and 25℃ temperature.
5. Standby mode: The clock inputs of all modules are stopped and all voltage supply of most modules is power on.
6. Bypass mode: Base on standby mode, enable all bypass functions.
7. Idle mode: CPU works in low frequency and other modules do nothing.
8. Play mode: Display output QVGA (320*240) size.

6.4 Crystal Input Timing

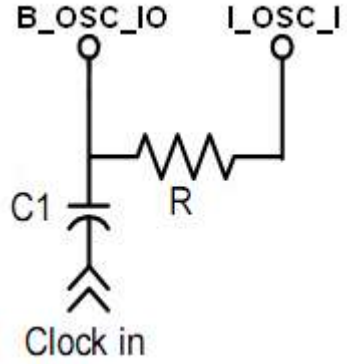
6.4.1 Crystal Oscillation



Parameter	Min.	Typ.	Max.	Unit
Resistor (R)	-	NC	-	MΩ
Capacitor (C1)	-	12	-	pF
Capacitor (C2)	-	12	-	pF

Note: Typical value is suitable for 16.384MHz crystal input.

6.4.2 External Clock



Parameter	Min.	Typ.	Max.	Unit
Resistor (R)	-	NC	-	MΩ
Capacitor (C1)	-	1000	-	pF
Frequency (clock in)	12	16.384	48	MHz
Clock in amplitude (peak to peak)	-	1.8	3.3	V

6.5 AC Characteristic

6.5.1 HIF Timing

I I2C Slave Interface Timing

<TBD>

II SPI Slave Interface Timing

<TBD>

III UART Interface Timing

<TBD>

IV LCM Interface Timing

<TBD>

6.5.2 LCD Controller Timing

<TBD>

6.5.3 Camera Emulation Timing

<TBD>

6.5.4 I2S Interface Timing

<TBD>

6.5.5 NOR Flash Controller Timing

<TBD>

6.6 I/O Pad Characteristic

Most pins on the MV6601C board can act as GPIO. There are 105 GPIO pins.
All GPIO-able pins power on to GPIO functional mode, except those GPIO pins that are shared with the host interfaces, JTAG, EJAG, and FLASH, which are powered on to functional mode,

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIL	Input low voltage	-0.3	-	0.3 VCCIO	V
VIH	Input high voltage	0.7 VCCIO	-	VCCIO+10%	V
IOL	Output low current	-	8	20	mA
IOH	Output high current	-	8	20	mA
IIL	Input leakage current	-	-	1	μA
Rd－	Pull down resistor	10K	-	150K	Ohm
Rd＋	Pull up resistor	10K	-	150K	Ohm

7. Physical Information

7.1 Package Dimension

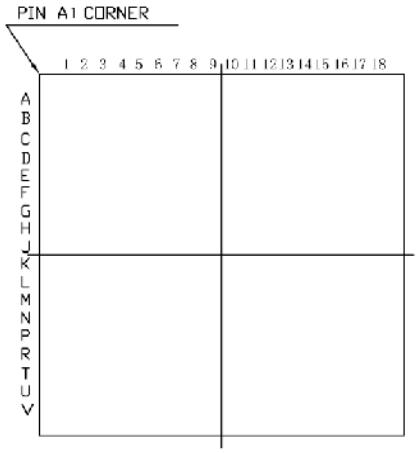


Figure 30 MV6601C package top view

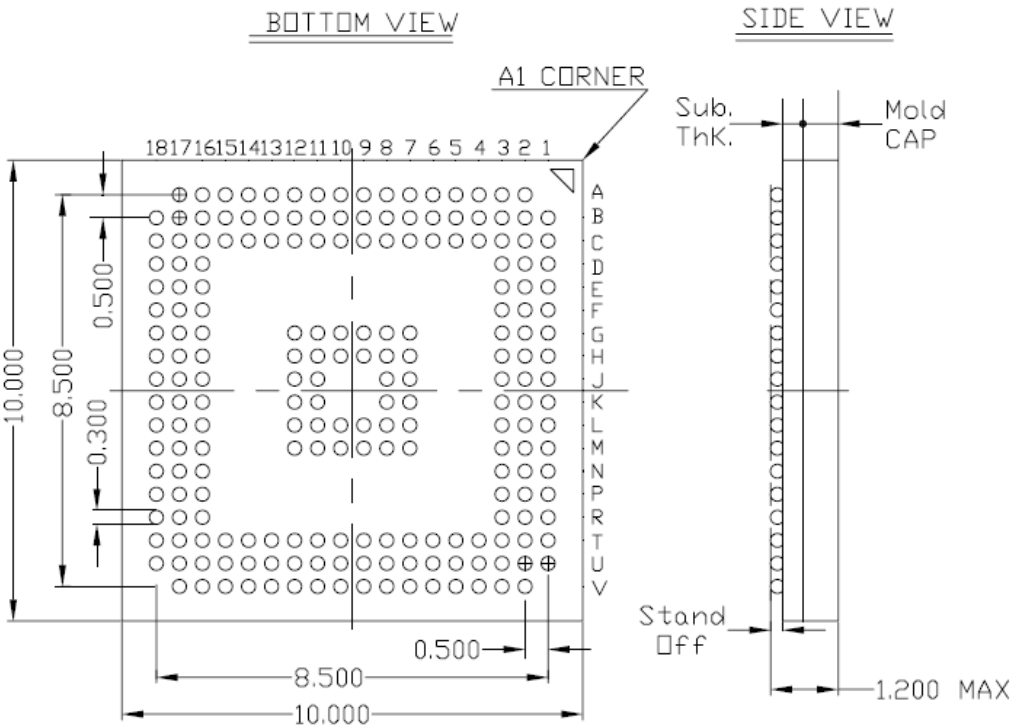


Figure 31 MV6601C package bottom and side view

7.2 Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
A		GPIO96 B_CLK_RST	I_OSC_F	GPIO14 B_LCM_WR_N	GPIO12 B_LCM_A0	GPIO16 B_LCM_D1	GPIO18 B_LCM_D3	GPIO20 B_LCM_D5	GPIO22 B_LCM_D7	I_OSC_I	B_OSC_IO	GPIO79 B_NOR_CE_N	B_NOR_RST_N	GPIO48 B_NOR_A1	GPIO50 B_NOR_A3	GPIO52 B_NOR_A5	GPIO54 B_NOR_A7		A
B	I_ADC_QP	GPIO97 B_CLK_PWDN	I_OSC_Z	GPIO11 B_LCM_CS_N	GPIO13 B_LCM_RD_N	GPIO15 B_LCM_D0	GPIO17 B_LCM_D2	GPIO19 B_LCM_D4	GPIO21 B_LCM_D6	GND3IO	GPIO80 B_NOR_OE_N	GPIO78 B_NOR_WE_N	GPIO47 B_NOR_A0	GPIO49 B_NOR_A2	GPIO51 B_NOR_A4	GPIO53 B_NOR_A6	GPIO56 B_NOR_A9	GPIO55 B_NOR_A8	B
C	I_ADC_QN	GPIO81 B_I2C_M_SCL	VCCIO_CLK	GNDIO	VCCIO_BB	GNDIO	VCCIO_BB	GNDIO_SD	VCCIO_SD	VCC3IO	VCCK	VCC12A_PLL	GNDK	GNDA_PLL	GNDIO	VCCIO_NOR	GPIO58 B_NOR_A11	GPIO57 B_NOR_A10	C
D	I_ADC_IN	GPIO82 B_I2C_M_SDA	GNDIO													GNDIO	GPIO60 B_NOR_A13	GPIO59 B_NOR_A12	D
E	I_ADC_IP	O_ADC_VREF	GPIO9 B_TXD													VCCIO_NOR	GPIO62 B_NOR_A15	GPIO61 B_NOR_A14	E
F	O_ADC_VRN	O_ADC_VCM	GPIO10 B_RXD													GPIO70 B_NOR_D0	GPIO64 B_NOR_A17	GPIO63 B_NOR_A16	F
G	O_ADC_VRP	GPIO90 B_SPI_S_CE_N	O_CLK_OUT				VCC12A_ADC	GNDA_ADC	VCCK	VCCK	VCCIO_SD	VCCIO_SD				GPIO71 B_NOR_D1	GPIO66 B_NOR_A19	GPIO65 B_NOR_A18	G
H	GPIO94 B_I2C_S_SCL	GPIO91 B_SPI_S_SCLK	VCCIO_BB				VCCK	GNDK	GNDK	GNDK	GNDIO_SD	GNDIO_SD				GPIO72 B_NOR_D2	GPIO68 B_NOR_A21	GPIO67 B_NOR_A20	H
J	GPIO95 B_I2C_S_SDA	GPIO92 B_SPI_S_MISO	GNDIO				VCCK	GNDK			GNDK	VCCK				GPIO73 B_NOR_D3	GPIO46 B_LCD_DE	GPIO69 B_NOR_A22	J
K	GPIO0 GPIO0	GPIO93 B_SPI_S_MOSI	I_RST_N				VCCK	GNDK			GNDK	VCCK				GPIO74 B_NOR_D4	I_LCD_MCLK	O_LCD_PCLK	K
L	GPIO1 GPIO1	GPIO102 B_GPIO_0	I_TEST				GNDIO_SD	GNDIO_SD	GNDK	GNDK	GNDK	VCCK				GPIO75 B_NOR_D5	O_LCD_VS	O_LCD_HS	L
M	GPIO2 GPIO2	GPIO103 B_GPIO_1	GPIO98 B_PWM0				VCCIO_SD	VCCIO_SD	VCCK	VCCK	VCC12A_SDPLL	GNDA_SDPLL				GPIO76 B_NOR_D6	O_LCD_D1	O_LCD_D0	M
N	GPIO3 GPIO3	GPIO104 B_I2S_MCLK	VCCIO_PWM													GPIO77 B_NOR_D7	O_LCD_D3	O_LCD_D2	N
P	GPIO83 B_SPI_M_CE_N	VCCIO_SPI	GNDIO													GNDIO_LCD	O_LCD_D5	O_LCD_D4	P
R	GPIO84 B_SPI_M_SCLK	GNDIO	GPIO99 B_PWM1													VCCIO_LCD	O_LCD_D7	O_LCD_D6	R
T	GPIO85 B_SPI_M_MISO	GPIO100 B_PWM2	GPIO101 B_PWM3	VCCIO_C	GNDIO	GPIO4 GPIO4	GPIO5 GPIO5	GPIO6 GPIO6	GPIO7 GPIO7	GPIO8 GPIO8	VCC3A_DACHP	GNDA_DACHP	VCC3A_DAC	GNDA_DAC	GNDIO_LCD	VCCIO_LCD	GPIO27 B_LCD_D9	GPIO26 B_LCD_D8	T
U	GPIO86 B_SPI_M_MOSI	O_C_MCLK	GPIO36 B_C_HS	GPIO38 B_C_YUV0	GPIO40 B_C_YUV2	GPIO42 B_C_YUV4	GPIO44 B_C_YUV6	GPIO87 B_I2S_I_CLK	GPIO89 B_I2S_I_DATA	GPIO24 B_I2S_O_LRCK	I_DAC_VREFN	O_DAC_VCM	I_DAC_VREFP	GPIO35 B_LCD_D17	GPIO33 B_LCD_D15	GPIO31 B_LCD_D13	GPIO29 B_LCD_D11	GPIO28 B_LCD_D10	U
V		O_C_PCLK	GPIO37 B_C_VS	GPIO39 B_C_YUV1	GPIO41 B_C_YUV3	GPIO43 B_C_YUV5	GPIO45 B_C_YUV7	GPIO88 B_I2S_I_LRCK	GPIO23 B_I2S_O_CLK	GPIO25 B_I2S_O_DATA	O_DAC_LHP	O_DAC_RHP	O_DAC_R	O_DAC_L	GPIO34 B_LCD_D16	GPIO32 B_LCD_D14	GPIO30 B_LCD_D12		V
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

7.3 Ordering Information

Product Number	Package Type	Memo
MV6601C	TFBGA 208 balls 10*10*1.2	0.13um CMOS

7.4 Storage Condition and Period for Package

Package	Moisture Sensitivity Level	Max. Reflow Temperature	Floor Life Storage Condition	Dry Pack
BGA	LEVEL 3	220 +5/-0 ℃	168Hrs@ ≤30℃/60% R.H.	Yes

Note: Please refer to IP/JEDEC standard J-STD-020C or refer to the “CAUTION Note” on dry pack bag.

7.5 Recommended SMT Temperature Profile

This “Recommended” temperature profile is a rough guideline for SMT process reference. The Mavrix MV600 follows the JEDEC standard for reflow profile J-STD-020C July 2004.

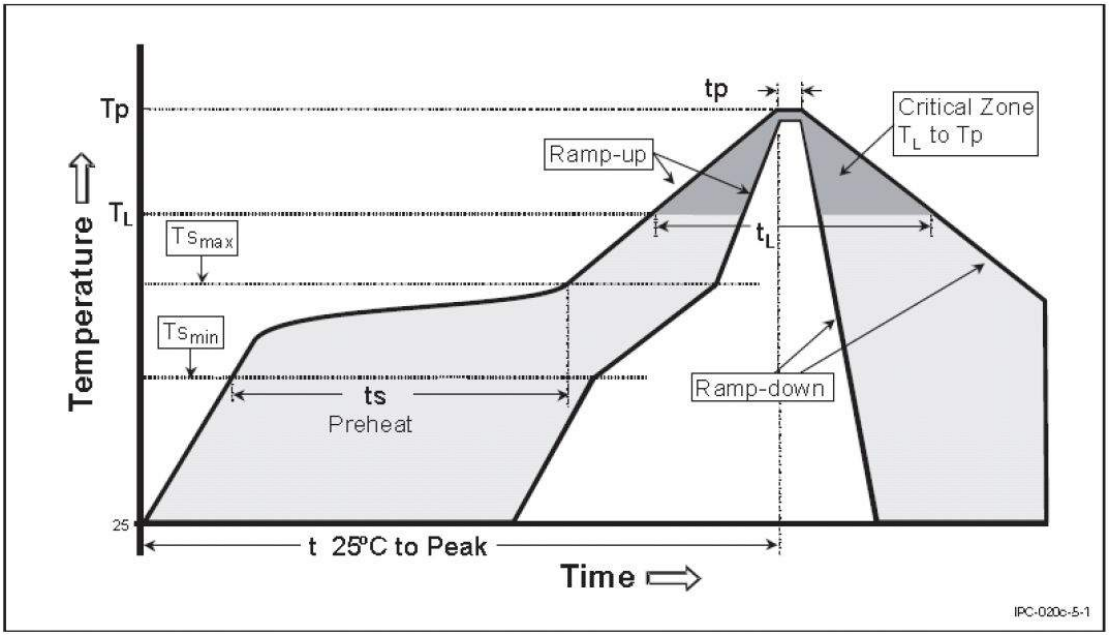
Process	Volume mm^3 <350	Volume mm^3 350 - 2000	Volume mm^3 >2000
SnPb Eutectic	240 +0/-5 ℃	225 +0/-5 ℃	225 +0/-5 ℃
Pb-Free Process	260 +0 ℃	260 +0 ℃	260 +0 ℃

IPC/JEDEC J-STD-020C July 2004

Table 5-2 Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3 °C/second max.	3° C/second max.
Preheat – Temperature Min (Ts_{min}) – Temperature Max (Ts_{max}) – Time (ts_{min} to ts_{max})	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: – Temperature (T_L) – Time (t_L)	 183 °C 60-150 seconds	 217 °C 60-150 seconds
Peak/Classification Temperature (Tp)	See Table 4.1	See Table 4.2
Time within 5 °C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/second max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Note 1: All temperatures refer to topside of the package, measured on the package body surface.



Appendix

Group Connection Diagram

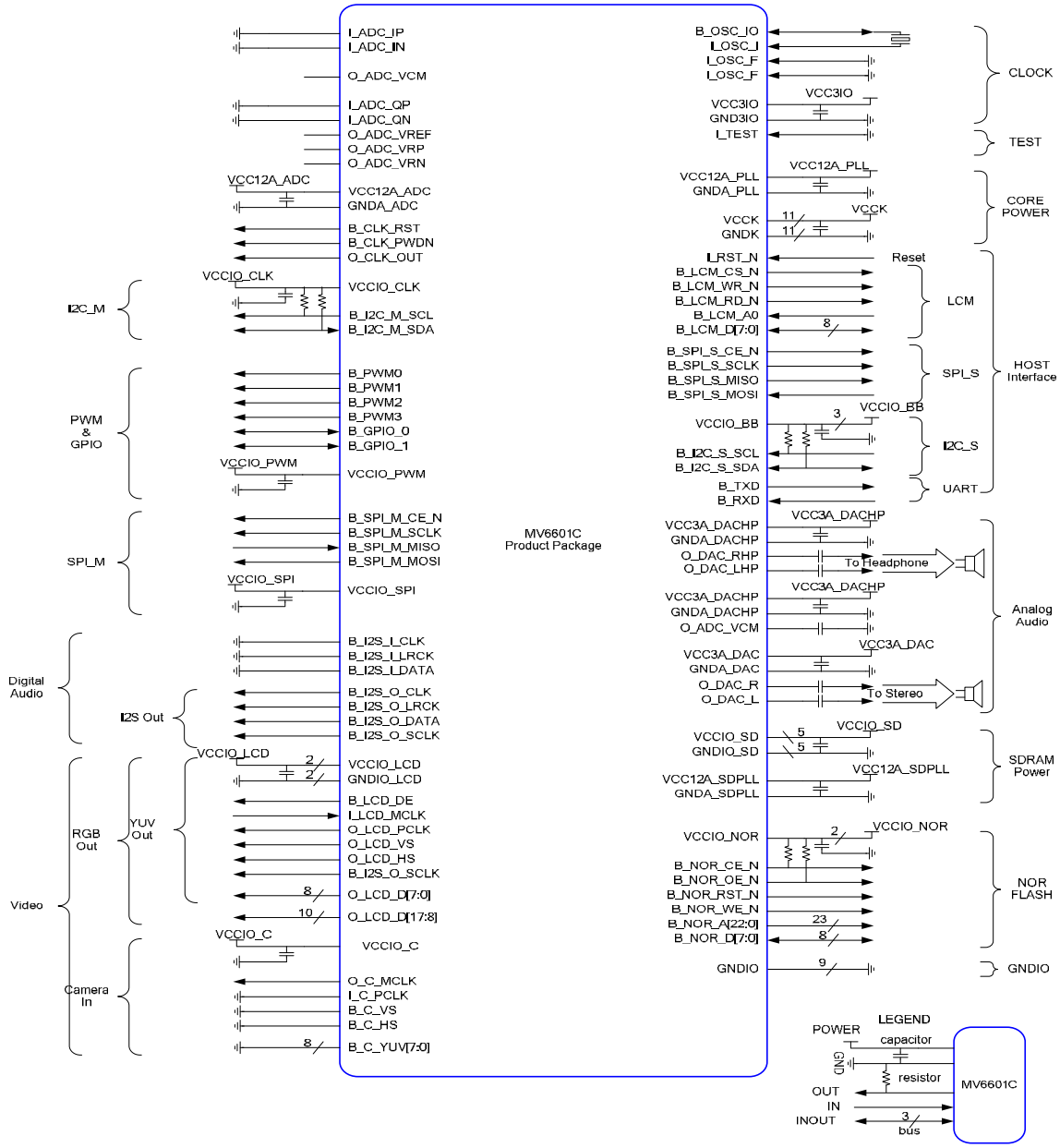


Figure 32 MV6601C group connection diagram

Acronym and Abbreviation

Acronym and Abbreviation	Full Name
IO	Input/Output
B	Bi-Directional
S	Slave
M	Master
SCLK	Signal Clock
MCLK	Master Clock
PCLK	Pixel Clock
TXD	Transfer Data
RXD	Receive Data
LRC	Left-Right Clock
HS, VS	Horizontal Synchronization, Vertical Synchronization
MISO	Master In Slave Out
MOSI	Master Out Slave In
CE, CS	Chip Enable, Chip Select
DAC	Digital-to-analog converters

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