

MU1503V LDMOS TRANSISTOR

Document Number: MU1503V
Preliminary Datasheet V1.0

30W, 50V High Power RF LDMOS FETs

Description

The MU1503V is a 30-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.5 GHz.

- Typical Performance (On Innogration narrow band fixture with device soldered):

$V_{DD} = 50$ Volts, $I_{DQ} = 100$ mA, CW.

Frequency	Gp (dB)	P_{out} (W)	$\eta_D @ P_{out}$ (%)
915 MHz	24	36	60

MU1503V



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 1200-1400MHz(L band)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)
- 960-1215MHz(Avionics)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	120	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ\text{C}$, $P_{out} = 30\text{W}$	$R_{\theta JC}$	2.9	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22—A114)	Class 2

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Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V _{GS} =0, I _{DS} =1.0Ma	V _{(BR)DSS}		122		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 50V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Gate—Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 50V, I _D = 600 μA)	V _{GS(th)}	—	2.73	—	V
Gate Quiescent Voltage (V _{DD} = 50 V, I _D = 100 mA, Measured in Functional Test)	V _{GS(Q)}	—	3.57	—	V
Drain source on state resistance (V _{DS} = 0.1V, V _{GS} = 10 V)	R _{ds(on)}		900		mΩ
Common Source Input Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz)	C _{ISS}		28.3		pF
Common Source Output Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz)	C _{OSS}		11.9		pF
Common Source Feedback Capacitance (V _{GS} = 0V, V _{DS} =50 V, f = 1 MHz)	C _{RSS}		0.38		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 100mA, f = 915 MHz, CW Signal Measurements, Pin=21.5dBm

Power Gain@Pout	Gp	—	24	—	dB
Output Power	Pout	30	36		W
Drain Efficiency@Pout	η _D	—	60	—	%
Input Return Loss	IRL	—	-7	—	dB
Ruggedness at all phase angle	VSWR		10:1		

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Package Outline

Flanged ceramic package; 2 leads

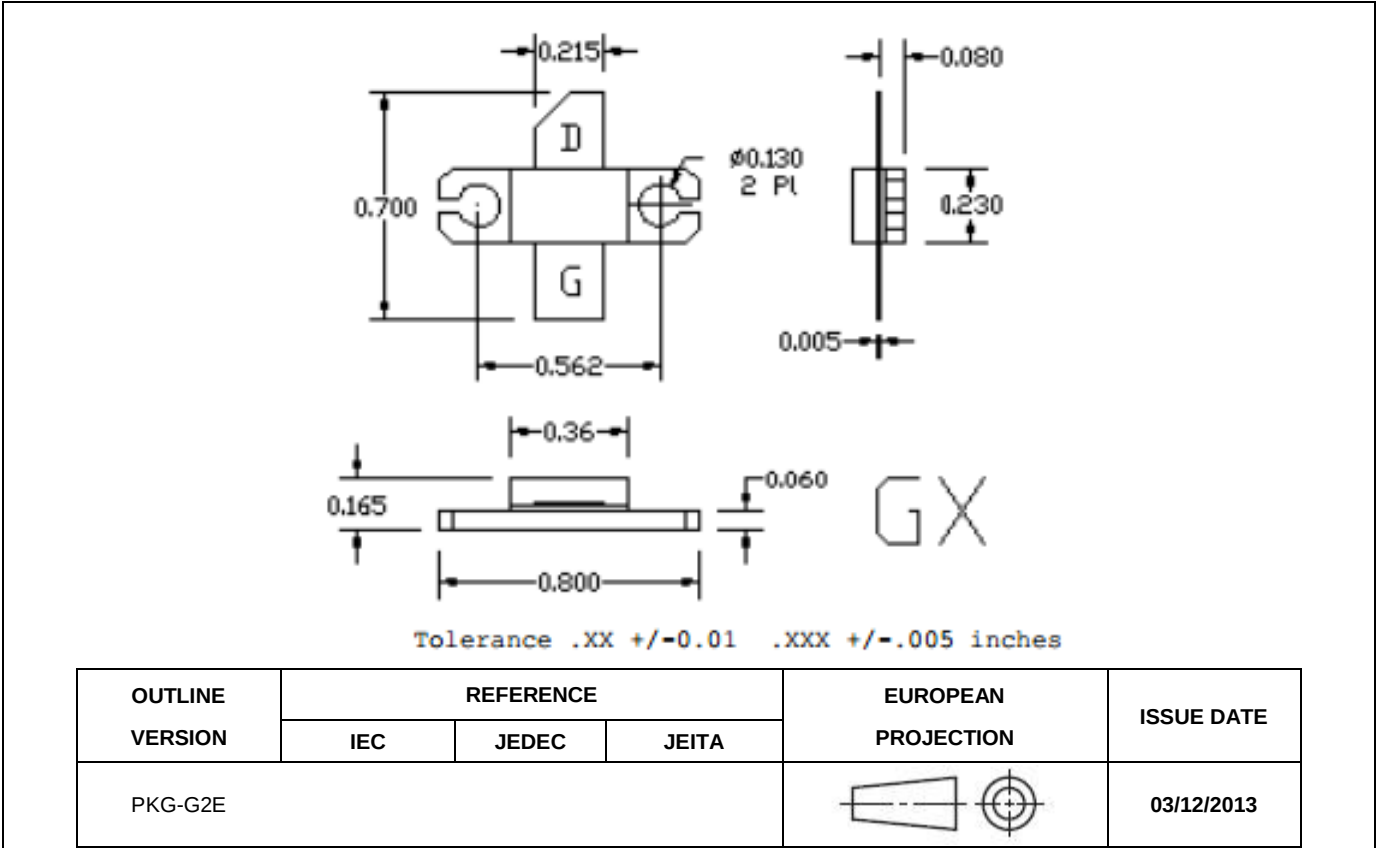


Figure 1. Package Outline PKG-G2E

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/7/18	V1.0	Preliminary Datasheet Creation

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