

MU1502 LDMOS TRANSISTOR

Document Number: MU1502
Product Datasheet V4.0

1500MHz, 25W, 28V High Power RF LDMOS FETs

Description

The MU1502 is a 25-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.5 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

- Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 150$ mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	$\eta_D @ P_{-1}$ (%)
1000 MHz	20	25	60

- Typical Performance (In Demo Fixture): $V_{DD} = 24$ Volts, $I_{DQ} = 50$ mA, CW.

Frequency	Gp (dB)	P_{OUT} (W)	η_D (%)	2nd Harmonic (dBc)	3rd Harmonic (dBc)
1300 MHz	14.5	21	50	-18	-29

MU1502



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	1.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
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Human Body Model (per JESD22--A114)	Class 2
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Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V _{GS} =0, I _{DS} =1.0mA	V _{(BR)DSS}	95	97		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 75V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 V, V _{GS} = 0 V)	I _{DSS}	—	—	1	μA
Gate--Source Leakage Current (V _{GS} = 10 V, V _{DS} = 0 V)	I _{GSS}	—	—	1	μA
Gate Threshold Voltage (V _{DS} = 28V, I _D = 150 μA)	V _{GS(th)}	—	2.11	—	V
Gate Quiescent Voltage (V _{DD} = 28 V, I _D = 150 mA, Measured in Functional Test)	V _{GS(Q)}	—	3.0	—	V
Common Source Input Capacitance (V _{GS} = 0V, V _{DS} =28 V, f = 1 MHz)	C _{ISS}		31.5		pF
Common Source Output Capacitance (V _{GS} = 0V, V _{DS} =28 V, f = 1 MHz)	C _{OSS}		12.8		pF
Common Source Feedback Capacitance (V _{GS} = 0V, V _{DS} =28 V, f = 1 MHz)	C _{RSS}		0.7		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 150mA, f = 1000 MHz, CW Signal Measurements.

Power Gain	G _p	—	20	—	dB
Drain Efficiency@P1dB	η _D	—	60	—	%
1 dB Compression Point	P _{-1dB}	—	25	—	W
Input Return Loss	IRL	—	-7	—	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 150 mA, f = 1000 MHz

VSWR 20:1 at 25W pulse CW Output Power	No Device Degradation
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Package Outline

Flanged ceramic package; 2 leads

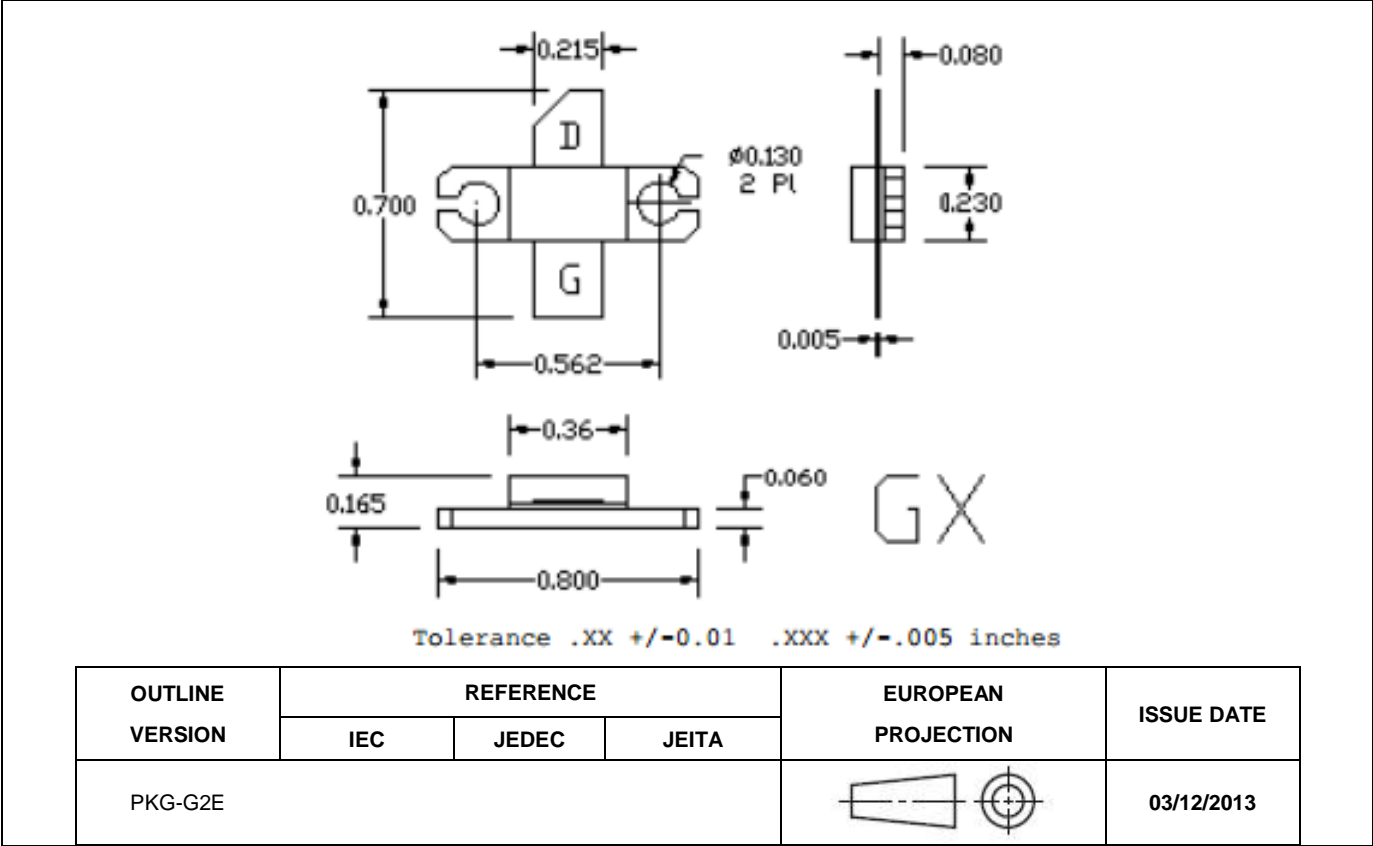


Figure 1. Package Outline PKG-G2E

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2016/3/28	Rev 1.0	Preliminary Datasheet
2016/8/8	Rev 2.0	Preliminary Datasheet
2016/8/22	Rev 2.1	Preliminary Datasheet
		Add Package Name
2016/12/2	Rev 3.0	Preliminary Datasheet
		Add Higher supply voltage performance
2017/2/22	Rev 4.0	Product Datasheet
		Add CV parameter

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