MYSON
TECHNOLOGY

MTV212M64
(Rev. 1.2)

8051 Embedded Monitor Controller MTP Type

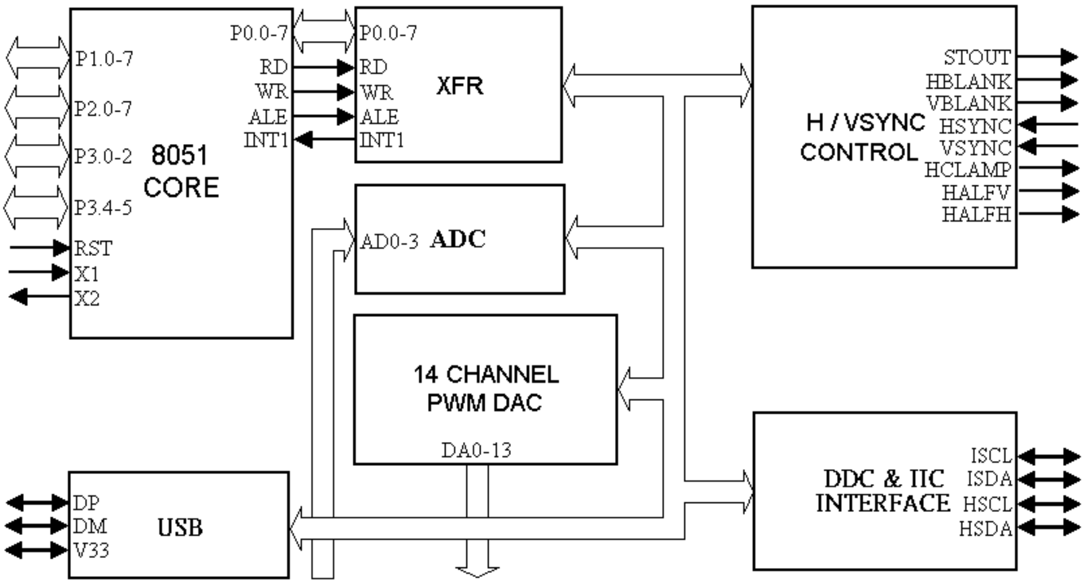
FEATURES

- 8051 core, 12MHz operating frequency.
- 1024-byte RAM, 64K-byte program Flash-ROM.•
- Maximum 14 channels of 9V open-drain PWM DAC.
- Maximum 32 bi-directional I/O pins.
- SYNC processor for composite separation/insertion, H/V polarity/frequency check, polarity adjustment and programmable clamp pulse output.
- Built-in self-test pattern generator with three free-running timings.
- Built-in low power reset circuit.
- Compliant with VESA DDC1/2B/2Bi/2B+ standard.
- Dual slave IIC addresses.
- Single master IIC interface for internal device communication.
- 4-channel 6-bit ADC.
- Watchdog timer with programmable interval.
- Compliant with Low Speed USB Spec.1.1 including 2 Endpoints: one is Control endpoint (8-byte IN & 8-byte OUT FIFOs), the other one is Interrupt endpoint (8-byte IN FIFO).
- Built-in 3.3V regulator for USB Interface.
- 40-pin DIP, 42-pin SDIP or 44-pin PLCC package.

GENERAL DESCRIPTIONS

The MTV212M micro-controller is an 8051 CPU core embedded device specially tailored to Monitor applications. It includes an 8051 CPU core, 1024-byte SRAM, SYNC processor, 14 built-in PWM DACs, VESA DDC interface, 4-channel A/D converter, Low Speed USB Interface and a 64K-byte internal program Flash-ROM.

BLOCK DIAGRAM



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DEVICE SUMMARY

The MTV212M is the MTP (Multi-Time Programming) type device for all of MTV212A mask ROM derivatives, the memory size and package differences please see the table below:

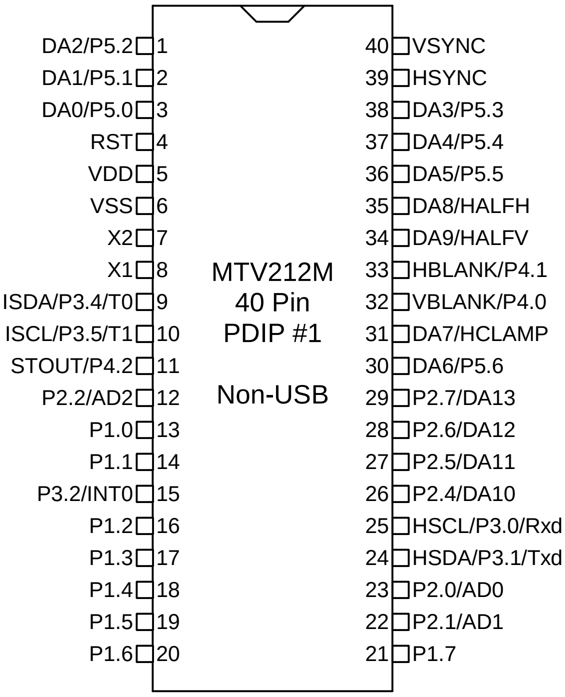
Part Number	USB	ROM	RAM	Package
MTV212A16	No	16K	256	PDIP40, SDIP42, PLCC44
MTV212A24	No	24K	512	PDIP40, SDIP42, PLCC44
MTV212A32	No	32K	512	PDIP40, SDIP42, PLCC44
MTV212A32U	Yes	32K	768	PDIP40, SDIP42, PLCC44
MTV212A48U	Yes	48K	768	PDIP40, SDIP42, PLCC44
MTV212A64U	Yes	64K	1024	PDIP40, SDIP42, PLCC44

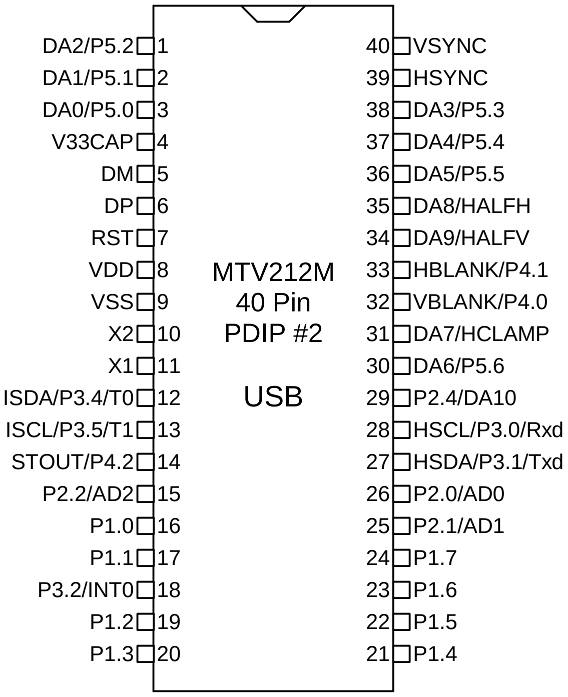
The use of Auxiliary RAM (AUXRAM) is limited for targeted mask ROM, the allowable XBANK (35h) bank selection is defined as the table below:

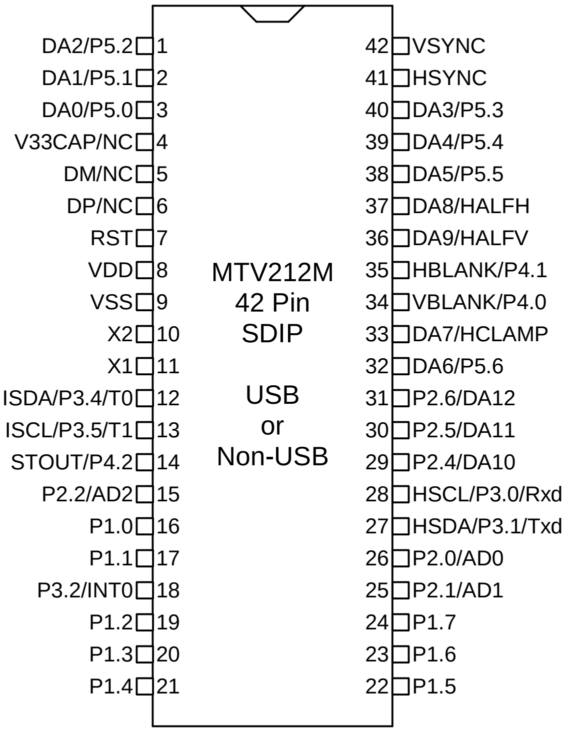
Part Number	RAM	Xbnk2	Xbnk1	Xbnk0
MTV212A16	256	-	-	-
MTV212A24	512	0 0	0 0	0 1
MTV212A32	512	0 0	0 0	0 1
MTV212A32U	768	0 0 0 0	0 0 1 1	0 1 0 1
MTV212A48U	768	0 0 0 0	0 0 1 1	0 1 0 1
MTV212A64U	1024	0 0 0 0 1 1	0 0 1 1 0 0	0 1 0 1 0 1

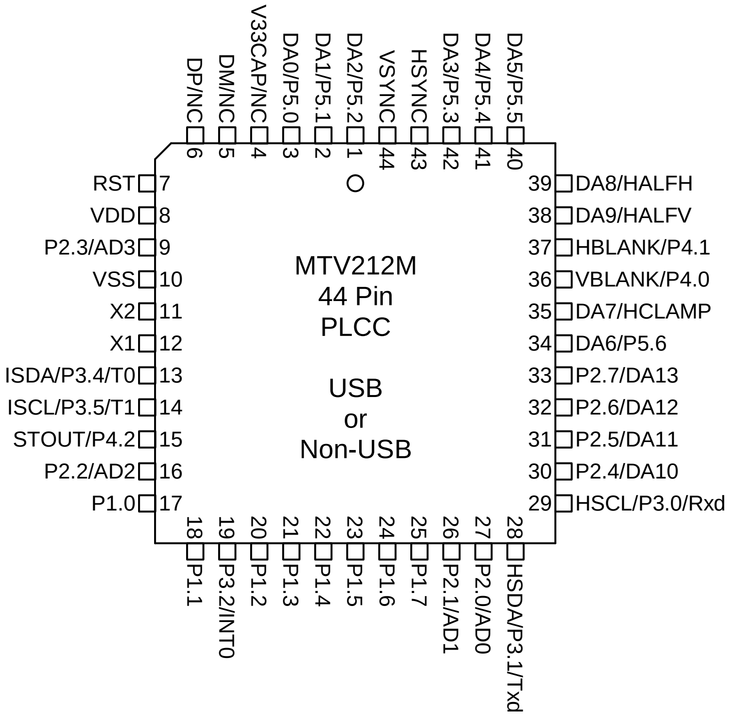
Remark:
The major pin connection differences between USB (MTV212M64U) and non-USB (MTV212M64) types are pin# 4, #5 and #6 for SDIP42 and PLCC44. The pin name of USB device is V33CAP(#4), VM(#5) and VP(#6), while NC (No Connection) for non-USB device.

PIN CONNECTION









PIN DESCRIPTION

Name	Type	Pin#				Description
		40	40	42	44	
DA2/P5.2	I/O	1	1	1	1	PWM DAC output / General purpose I/O (open drain).
DA1/P5.1	I/O	2	2	2	2	PWM DAC output / General purpose I/O (open drain).
DA0/P5.0	I/O	3	3	3	3	PWM DAC output / General purpose I/O (open drain).
V33CAP/NC	I/O	-	4	4	4	3.3V Regulator Capacitor connection or NC.
DM/NC	I/O	-	5	5	5	USB DM or NC.
DP/NC	I/O	-	6	6	6	USB DP or NC.
RST	I	4	7	7	7	Active high reset.
VDD	-	5	8	8	8	Positive Power Supply.
P2.3/AD3	I/O	-	-	-	9	General purpose I/O / ADC Input.
VSS	-	6	9	9	10	Ground.
X2	O	7	10	10	11	Oscillator output.
X1	I	8	11	11	12	Oscillator input.
ISDA/P3.4/T0	I/O	9	12	12	13	Master IIC data / General purpose I/O / T0.
ISCL/P3.5/T1	I/O	10	13	13	14	Master IIC clock / General purpose I/O / T1.
STOUT/P4.2	O	11	14	14	15	Self-test video output / General purpose Output.
P2.2/AD2	I/O	12	15	15	16	General purpose I/O / ADC Input.
P1.0	I/O	13	16	16	17	General purpose I/O.
P1.1	I/O	14	17	17	18	General purpose I/O.
P3.2/INT0	I	15	18	18	19	General purpose Input / INT0.
P1.2	I/O	16	19	19	20	General purpose I/O.
P1.3	I/O	17	20	20	21	General purpose I/O.
P1.4	I/O	18	21	21	22	General purpose I/O.
P1.5	I/O	19	22	22	23	General purpose I/O.
P1.6	I/O	20	23	23	24	General purpose I/O.
P1.7	I/O	21	24	24	25	General purpose I/O.
P2.1/AD1	I/O	22	25	25	26	General purpose I/O / ADC Input.
P2.0/AD0	I/O	23	26	26	27	General purpose I/O / ADC Input.
HSDA/P3.1/Txd	I/O	24	27	27	28	Slave IIC data / General purpose I/O / Txd.
HSCL/P3.0/Rxd	I/O	25	28	28	29	Slave IIC clock / General purpose I/O / Rxd.
P2.4/DA10	I/O	26	29	29	30	General purpose I/O / PWM DAC output (open drain).
P2.5/DA11	I/O	27	-	30	31	General purpose I/O / PWM DAC output (open drain).
P2.6/DA12	I/O	28	-	31	32	General purpose I/O / PWM DAC output (open drain).
P2.7/DA13	I/O	29	-	-	33	General purpose I/O / PWM DAC output (open drain).
DA6/P5.6	I/O	30	30	32	34	PWM DAC output / General purpose I/O (open drain).
DA7/HCLAMP	O	31	31	33	35	PWM DAC output / Hsync clamp pulse output (open drain).
VBLANK/P4.0	O	32	32	34	36	Vertical blank / General purpose Output.
HBLANK/P4.1	O	33	33	35	37	Horizontal blank / General purpose Output.
DA9/HALFV	O	34	34	36	38	PWM DAC output / Vsync half freq. output (open drain).
DA8/HALFH	O	35	35	37	39	PWM DAC output / Hsync half freq. output (open drain).
DA5/P5.5	I/O	36	36	38	40	PWM DAC output / General purpose I/O (open drain).
DA4/P5.4	O	37	37	39	41	PWM DAC output / General purpose I/O (open drain).
DA3/P5.3	O	38	38	40	42	PWM DAC output / General purpose I/O (open drain).
HSYNC	I	39	39	41	43	Horizontal SYNC or Composite SYNC Input.
VSYNC	I	40	40	42	44	Vertical SYNC input.

FUNCTIONAL DESCRIPTIONS

1. 8051 CPU Core

MTV212M includes all 8051 functions with the following exceptions:

1.1 PSEN, ALE, RD and WR pins are disabled. The external RAM access is restricted to XFRs within the MTV212M.
1.2 Port0, port3.3, port3.6 and port3.7 are not general-purpose I/O ports. They are dedicated to monitor special application.
1.3 INT1 input pin is not provided, it is connected to special interrupt sources.
1.4 Port2 are shared with special function pins.

In addition, there are 2 timers, 5 interrupt sources and serial interface compatible with the standard 8051.

Note: All registers listed in this document reside in external RAM area (XFR). For internal RAM memory map please refer to 8051 spec.

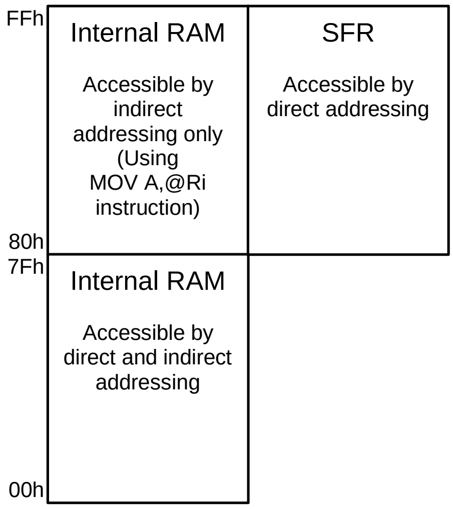
2. Memory Allocation

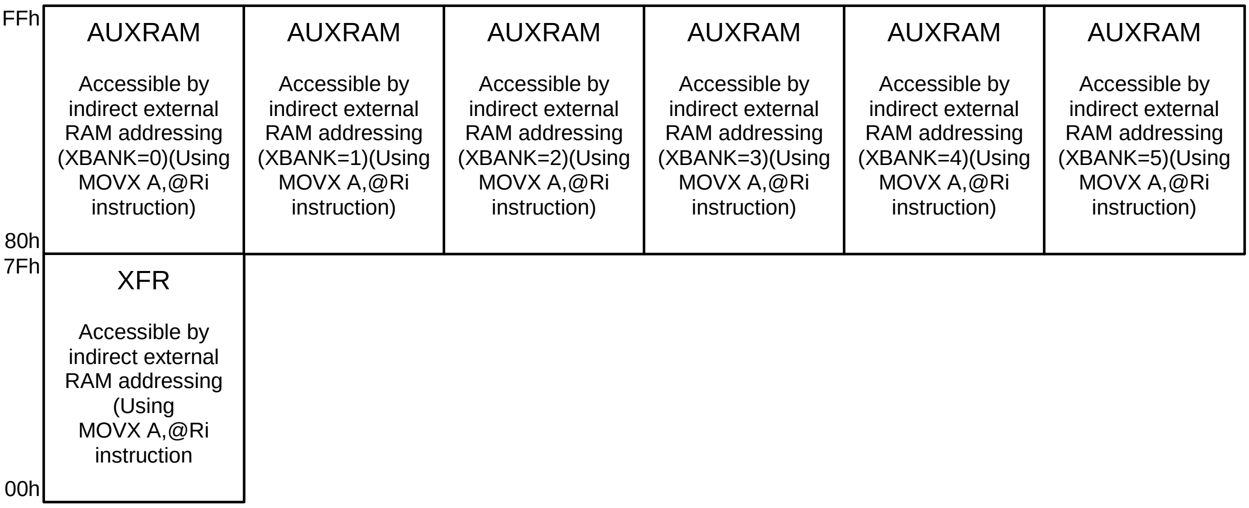
2.1 Internal Special Function Registers (SFR)
The SFR is a group of registers that are the same as standard 8051.

2.2 Internal RAM
There are total 256 bytes internal RAM in MTV212M, same as standard 8052.

2.3 External Special Function Registers (XFR)
The XFR is a group of registers allocated in the 8051 external RAM area 00h - 7Fh. Most of the registers are used for monitor control or PWM DAC. Program can initialize Ri value and use "MOVX" instruction to access these registers.

2.4 Auxiliary RAM (AUXRAM)
There are total 768 bytes auxiliary RAM allocated in the 8051 external RAM area 80h - FFh. The AUXRAM is divided into six banks, selected by XBANK register. Program can initialize Ri value and use "MOVX" instruction to access the AUXRAM.


FFh
Internal RAM
Accessible by indirect addressing only (Using MOV A,@Ri instruction)
SFR
Accessible by direct addressing
80h
7Fh
Internal RAM
Accessible by direct and indirect addressing
00h


FFh
AUXRAM
Accessible by indirect external RAM addressing (XBANK=0)(Using MOVX A,@Ri instruction)
AUXRAM
Accessible by indirect external RAM addressing (XBANK=1)(Using MOVX A,@Ri instruction)
AUXRAM
Accessible by indirect external RAM addressing (XBANK=2)(Using MOVX A,@Ri instruction)
AUXRAM
Accessible by indirect external RAM addressing (XBANK=3)(Using MOVX A,@Ri instruction)
AUXRAM
Accessible by indirect external RAM addressing (XBANK=4)(Using MOVX A,@Ri instruction)
AUXRAM
Accessible by indirect external RAM addressing (XBANK=5)(Using MOVX A,@Ri instruction)
80h
7Fh
XFR
Accessible by indirect external RAM addressing (Using MOVX A,@Ri instruction
00h

3. Chip Configuration

The Chip Configuration registers define the chip pins function, as well as the functional blocks' connection, configuration and frequency.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PADMOD	30h (w)	DA13E	DA12E	DA11E	DA10E	AD3E	AD2E	AD1E	AD0E
PADMOD	31h (w)		P56E	P55E	P54E	P53E	P52E	P51E	P50E
PADMOD	32h (w)	HIICE	IIICE	HLFVE	HLFHE	HCLPE	P42E	P41E	P40E
OPTION	33h (w)	PWMF	DIV253	FclkE	IICpass	ENSCL	Msel	MIICF1	MIICF0
OPTION	34h (w)							SlvAbs1	SlvAbs0
XBANK	35h (r/w)						Xbnk2	Xbnk1	Xbnk0

PADMOD (w) : Pad mode control registers. (All are "0" in Chip Reset)

DA13E = 1 → pin “P2.7/DA13” is DA13.
= 0 → pin “P2.7/DA13” is P2.7.
DA12E = 1 → pin “P2.6/DA12” is DA12.
= 0 → pin “P2.6/DA12” is P2.6.
DA11E = 1 → pin “P2.5/DA11” is DA11.
= 0 → pin “P2.5/DA11” is P2.5.
DA10E = 1 → pin “P2.4/DA10” is DA10.
= 0 → pin “P2.4/DA10” is P2.4.
AD3E = 1 → pin “P2.3/AD3” is AD3.
= 0 → pin “P2.3/AD3” is P2.3.
AD2E = 1 → pin “P2.2/AD2” is AD2.
= 0 → pin “P2.2/AD2” is P2.2.
AD1E = 1 → pin “P2.1/AD1” is AD1.
= 0 → pin “P2.1/AD1” is P2.1.
AD0E = 1 → pin “P2.0/AD0” is AD0.
= 0 → pin “P2.0/AD0” is P2.0.
P56E = 1 → pin “DA6/P5.6” is P5.6.
= 0 → pin “DA6/P5.6” is DA6.
P55E = 1 → pin “DA5/P5.5” is P5.5.
= 0 → pin “DA5/P5.5” is DA5.

P54E	= 1	→ pin “DA4/P5.4” is P5.4.	
	= 0	→ pin “DA4/P5.4” is DA4.	
P53E	= 1	→ pin “DA3/P5.3” is P5.3.	
	= 0	→ pin “DA3/P5.3” is DA3.	
P52E	= 1	→ pin “DA2/P5.2” is P5.2.	
	= 0	→ pin “DA2/P5.2” is DA2.	
P51E	= 1	→ pin “DA1/P5.1” is P5.1.	
	= 0	→ pin “DA1/P5.1” is DA1.	
P50E	= 1	→ pin “DA0/P5.0” is P5.0.	
	= 0	→ pin “DA0/P5.0” is DA0.	
HIICE	= 1	→ pin “HSCL/P3.0/Rxd” is HSCL;	pin “HSDA/P3.1/Txd” is HSDA.
	= 0	→ pin “HSCL/P3.0/Rxd” is P3.0/Rxd;	pin “HSDA/P3.1/Txd” is P3.1/Txd.
IIICE	= 1	→ pin “ISDA/P3.4/T0” is ISDA;	pin “ISCL/P3.5/T1” is ISCL.
	= 0	→ pin “ISDA/P3.4/T0” is P3.4/T0;	pin “ISCL/P3.5/T1” is P3.5/T1.
HLFVE	= 1	→ pin “DA9/HALFV” is VSYNC half frequency output.	
	= 0	→ pin “DA9/HALFV” is DA9.	
HLFHE	= 1	→ pin “DA8/HALFH” is HSYNC half frequency output.	
	= 0	→ pin “DA8/HALFH” is DA8.	
HCLPE	= 1	→ pin “DA7/HCLAMP” is HSYNC clamp pulse output.	
	= 0	→ pin “DA7/HCLAMP” is DA7.	
P42E	= 1	→ pin “STOUT/P4.2” is P4.2.	
	= 0	→ pin “STOUT/P4.2” is STOUT.	
P41E	= 1	→ pin “HBLANK/P4.1” is P4.1.	
	= 0	→ pin “HBLANK/P4.1” is HBLANK.	
P40E	= 1	→ pin “VBLANK/P4.0” is P4.0.	
	= 0	→ pin “VBLANK/P4.0” is VBLANK.	

OPTION (w) : Chip option configuration (All are "0" in Chip Reset).

PWMF	= 1	→ select 94KHz PWM frequency.
	= 0	→ select 47KHz PWM frequency.
DIV253	= 1	→ PWM pulse width is 253 step resolution.
	= 0	→ PWM pulse width is 256 step resolution.
FclkE	= 1	→ Double CPU clock freq.
IICpass	= 1	→ HSCL/HSDA pin bypass to ISCL/ISDA pin in DDC2 mode.
	= 0	→ Separate Master and Slave IIC block.
ENSCL	= 1	→ Enable slave IIC block to hold HSCL pin low while MTV212M can't catch-up the external master's speed.
Msel	= 1	→ Master IIC block connect to HSCL/HSDA pins.
	= 0	→ Master IIC block connect to ISCL/ISDA pins.
MIICF1,MIICF0	= 1,1	→ select 400KHz Master IIC frequency.
	= 1,0	→ select 200KHz Master IIC frequency.
	= 0,1	→ select 50KHz Master IIC frequency.
	= 0,0	→ select 100KHz Master IIC frequency.

SlvAbs1,SlvAbs0 : Slave IIC block A's slave address length.

= 1,0	→ 5-bits slave address.
= 0,1	→ 6-bits slave address.
= 0,0	→ 7-bits slave address.

XBANK (r/w) : Auxiliary RAM bank switch.

Xbnk[2:0]	= 0	→ Select AUXRAM bank 0.
	= 1	→ Select AUXRAM bank 1.
	= 2	→ Select AUXRAM bank 2.
	= 3	→ Select AUXRAM bank 3.

= 4 → Select AUXRAM bank 4.
= 5 → Select AUXRAM bank 5.

4. Extra I/O

The extra I/O is a group of I/O pins located in XFR area. Port4 is output mode only. Port5 can be used as both output and input, because Port5's pin is open drain type, user must write Port5's corresponding bit to "1" in input mode.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PORT4	38h (w)						P42	P41	P40
PORT5	39h (r/w)		P56	P55	P54	P53	P52	P51	P50

PORT4 (w) : Port 4 data output value.

PORT5 (r/w) : Port 5 data input/output value.

5. PWM DAC

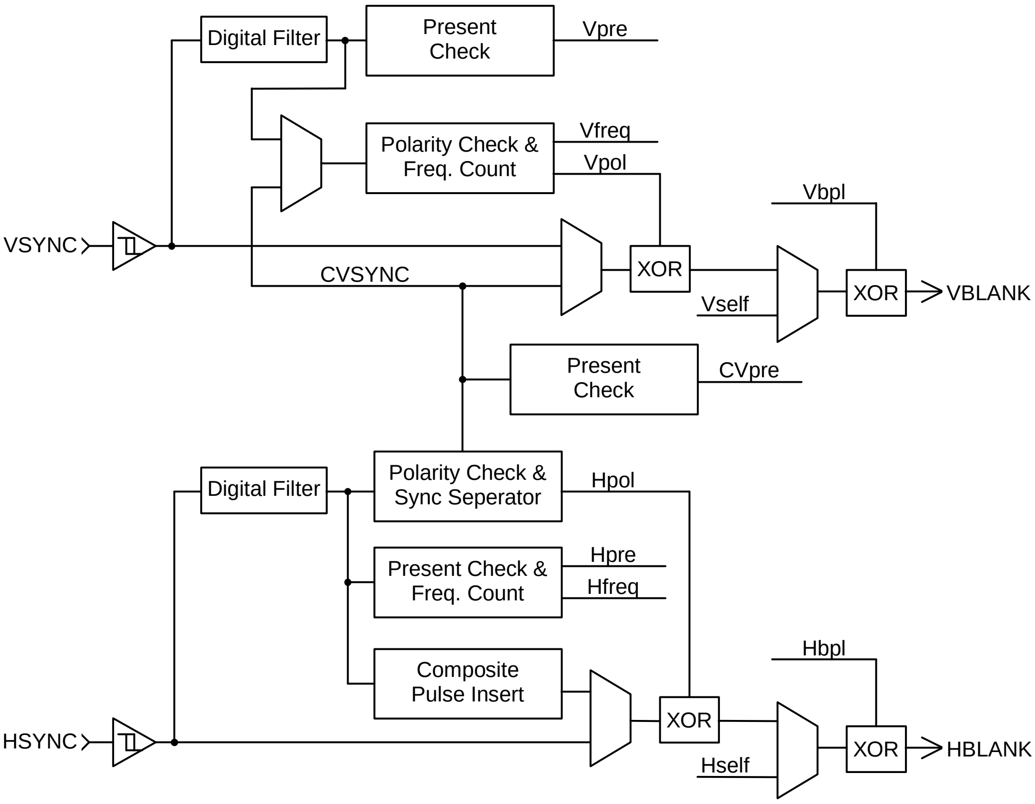
Each PWM DAC converter's output pulse width is controlled by an 8-bit register in XFR. The frequency of PWM clk is 47KHz or 94KHz, selected by PWMF. And the total duty cycle step of these DAC outputs is 253 or 256, selected by DIV253. If DIV253=1, writing FDH/FEH/FFH to DAC register generates stable high output. If DIV253=0, the output will pulse low at least once even if the DAC register's content is FFH. Writing 00H to DAC register generates stable low output.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DA0	20h (r/w)	Pulse width of PWM DAC 0							
DA1	21h (r/w)	Pulse width of PWM DAC 1							
DA2	22h (r/w)	Pulse width of PWM DAC 2							
DA3	23h (r/w)	Pulse width of PWM DAC 3							
DA4	24h (r/w)	Pulse width of PWM DAC 4							
DA5	25h (r/w)	Pulse width of PWM DAC 5							
DA6	26h (r/w)	Pulse width of PWM DAC 6							
DA7	27h (r/w)	Pulse width of PWM DAC 7							
DA8	28h (r/w)	Pulse width of PWM DAC 8							
DA9	29h (r/w)	Pulse width of PWM DAC 9							
DA10	2Ah (r/w)	Pulse width of PWM DAC 10							
DA11	2Bh (r/w)	Pulse width of PWM DAC 11							
DA12	2Ch (r/w)	Pulse width of PWM DAC 12							
DA13	2Dh (r/w)	Pulse width of PWM DAC 13							

DA0-13 (r/w) : The output pulse width control for DA0-13.
* All of PWM DAC converters are centered with value 80h after power on.

6. H/V SYNC Processing

The H/V SYNC processing block performs the functions of composite signal separation/insertion, SYNC inputs presence check, frequency counting, polarity detection and control, as well as the protection of VBLANK output while VSYNC speed up in high DDC communication clock rate. The present and frequency function block treat any pulse shorter than one OSC period as noise.



H/V SYNC Processor Block Diagram

6.1 Composite SYNC separation/insertion

The MTV212M continuously monitors the input HSYNC, if the vertical SYNC pulse can be extracted from the input, a CVpre flag is set and user can select the extracted "CVSYNC" for the source of polarity check, frequency count, and VBLANK output. The CVSYNC will have 8us delay compared to the original signal. The MTV212M can also insert pulse to HBLANK output during composite VSYNC's active time. The insert pulse's width is 1/8 HSYNC period and the insertion frequency can adapt to original HSYNC.

6.2 H/V Frequency Counter

MTV212M can discriminate HSYNC/VSYNC frequency and saves the information in XFRs. The 14 bits Hcounter counts the time of 64xHSYNC period, then load the result into the HCNTH/HCNTL latch. The output value will be [(128000000/H-Freq) - 1], updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is non-present. The 12 bits Vcounter counts the time between two VSYNC pulses, then load the result into the VCNTH/VCNTL latch. The output value will be (62500/V-Freq), updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of H/V counter overflow. The VFchg/HFchg interrupt is set when VCNT/HCNT value changes or overflow. Table 4.2.1 and table 4.2.2 shows the HCNT/VCNT value under the operations of 12MHz.

6.2.1 H-Freq Table

H-Freq(KHZ)		Output Value (14 bits)
		12MHz OSC (hex / dec)
1	31.5	0FDEh / 4062
2	37.5	0D54h / 3412
3	43.3	0B8Bh / 2955
4	46.9	0AA8h / 2728
5	53.7	094Fh / 2383
6	60.0	0854h / 2132
7	68.7	0746h / 1862
8	75.0	06AAh / 1706
9	80.0	063Fh / 1599
10	85.9	05D1h / 1489
11	93.8	0554h / 1364
12	106.3	04B3h / 1203

6.2.2 V-Freq Table

V-Freq(Hz)		Output value (12bits)
		12MHz OSC (hex / dec)
1	56	45Ch / 1116
2	60	411h / 1041
3	70	37Ch / 892
4	72	364h / 868
5	75	341h / 833
6	85	2DFh / 735

6.3 H/V Present Check

The Hpresent function checks the input HSYNC pulse, Hpre flag is set when HSYNC is over 10KHz or cleared when HSYNC is under 10Hz. The Vpresent function checks the input VSYNC pulse, the Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz. The HPRchg interrupt is set when the Hpre value changes. The VPRchg interrupt is set when the Vpre/CVpre value change. However, the CVpre flag interrupt may be disabled when S/W disable the composite function.

6.4 H/V Polarity Detect

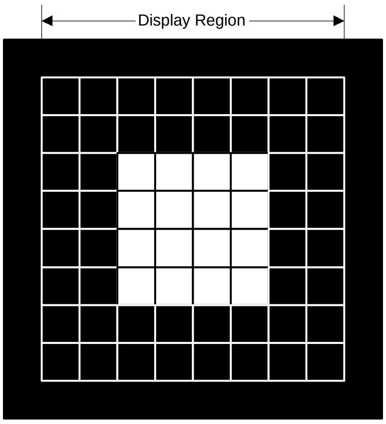
The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The HPLchg interrupt is set when the Hpol value changes. The VPLchg interrupt is set when the Vpol value changes.

6.5 Output HBLANK/VBLANK Control and Polarity Adjust

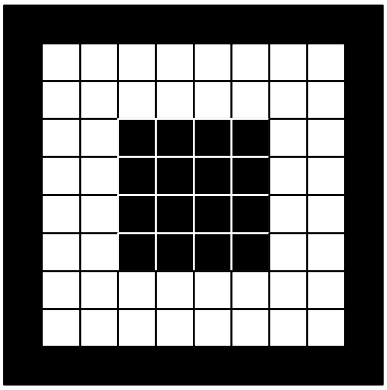
The HBLANK is the mux output of HSYNC, composite Hpulse and self-test horizontal pattern. The VBLANK is the mux output of VSYNC, CVSYNC and self-test vertical pattern. The mux selection and output polarity are S/W controllable. The VBLANK output is cut off when VSYNC frequency is over 200Hz. The HBLANK/VBLANK shares the output pin with P4.1/ P4.0.

6.6 Self Test Pattern Generator

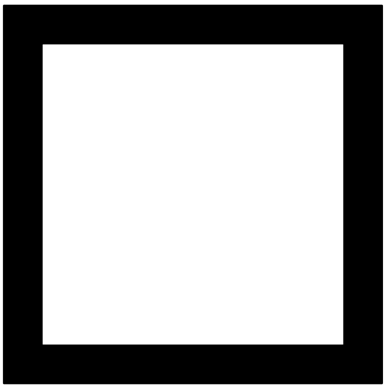
This generator can generate 4 display patterns for testing purpose, which are positive cross-hatch, negative cross-hatch, full white, and full black (showed as following figure). The HBLANK output frequency of the pattern can be chosen to 63.5KHz, 47.6KHz and 31.75KHz. The VBLANK output frequency of the pattern is 60Hz. It is originally designed to support monitor manufacturer to do burn-in test, or offer end-user a reference to check the monitor. The generator's output STOUT shares the output pin with P4.2.



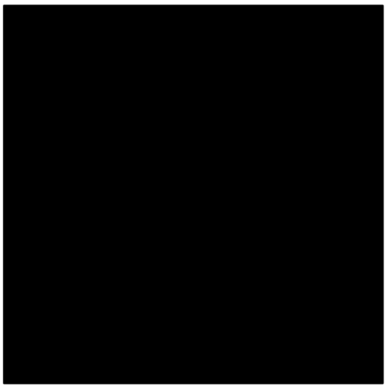
Positive cross-hatch



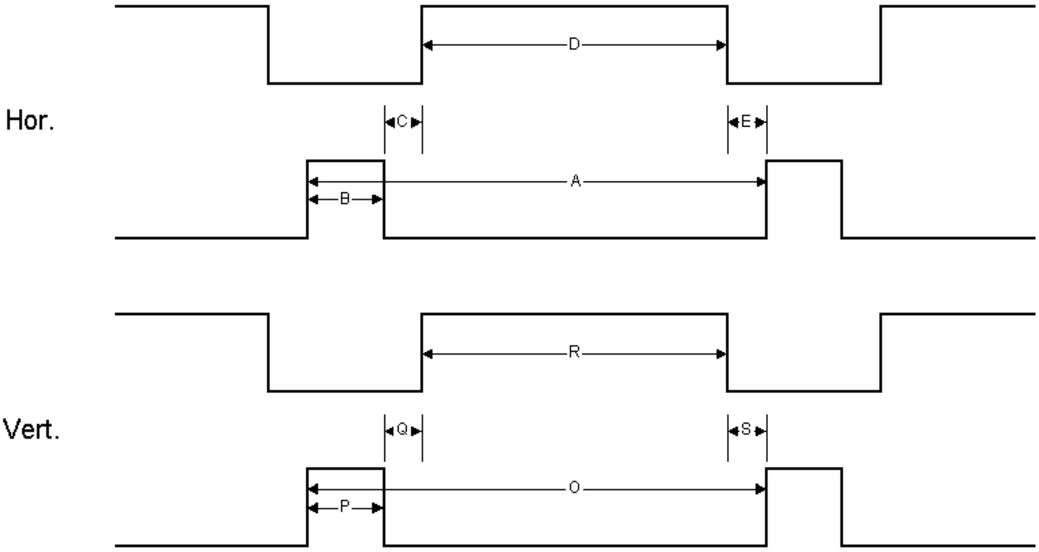
Negative cross-hatch



Full white



Full black



MTV212M Self-Test pattern timing

	63.5KHz, 60Hz		47.6KHz, 60Hz		31.7KHz, 60Hz	
	Absolute time	H dots	Absolute time	H dots	Absolute time	H dots
Hor. Total time (A)	15.75us	1280	21.0us	1024	31.5us	640
Hor. Active time (D)	12.05us	979.3	16.07us	783.2	24.05us	488.6
Hor. F. P. (E)	0.2us	16.25	0.28us	12	0.45us	9
SYNC pulse width (B)	1.5us	122	2us	90	3us	61
Hor. B. P. (C)	2us	162.54	2.67us	110	4us	81.27

	Absolute time	V lines	Absolute time	V lines	Absolute time	V lines
Vert. Total time (O)	16.663ms	1024	16.663ms	768	16.663ms	480
Vert. Active time (R)	15.655ms	962	15.655ms	721.5	15.655ms	451
Vert. F. P. (S)	0.063ms	3.87	0.063ms	2.9	0.063ms	1.82
SYNC pulse width (P)	0.063ms	3.87	0.063ms	2.9	0.063ms	1.82
Vert. B. P. (Q)	0.882ms	54.2	0.882ms	40.5	0.882ms	25.4

* 8 x 8 blocks of cross hatch pattern in display region.

6.7 HSYNC Clamp Pulse Output

The HCLAMP output is active by setting “HCLPE” control bit. The HCLAMP’s leading edge position, pulse width and polarity is S/W controllable.

6.8 VSYNC Interrupt

The MTV212M check the VSYNC input pulse and generate an interrupt at its leading edge. The VSYNC flag is set each time when MTV212M detects a VSYNC pulse. The flag is cleared by S/W writing a "0".

6.9 H/V SYNC Processor Register

Reg name	**addr**	**bit7**	**bit6**	**bit5**	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**
HVSTUS	40h (r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	41h (r)	Hovf		HF13	HF12	HF11	HF10	HF9	HF8
HCNTL	42h (r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	43h (r)	Vovf				VF11	VF10	VF9	VF8
VCNTL	44h (r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR0	40h (w)	C1	C0	NoHins				HBpl	VBpl
HVCTR2	42h (w)			Selft	STF1	STF0	Rt1	Rt0	STE
HVCTR3	43h (w)		CLPEG	CLPPO	CLPW2	CLPW1	CLPW0		
INTFLG	48h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg		Vsync
INTEN	49h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF		EVsync

HVSTUS (r) : The status of polarity, present and static level for HSYNC and VSYNC.

CVpre = 1 → The extracted CVSYNC is present.
= 0 → The extracted CVSYNC is not present.
Hpol = 1 → HSYNC input is positive polarity.
= 0 → HSYNC input is negative polarity.
Vpol = 1 → VSYNC (CVSYNC) is positive polarity.
= 0 → VSYNC (CVSYNC) is negative polarity.
Hpre = 1 → HSYNC input is present.
= 0 → HSYNC input is not present.
Vpre = 1 → VSYNC input is present.
= 0 → VSYNC input is not present.
Hoff* = 1 → HSYNC input's off level is high.

= 0 → HSYNC input's off level is low.
Voff* = 1 → VSYNC input's off level is high.
= 0 → VSYNC input's off level is low.
*Hoff and Voff are valid when Hpre=0 or Vpre=0.

HCNTH (r) : H-Freq counter's high bits.
Hovf = 1 → H-Freq counter is overflow, this bit is clear by H/W when condition removed.
HF13 - HF8 : 6 high bits of H-Freq counter.

HCNTL (r) : H-Freq counter's low byte.

VCNTH (r) : V-Freq counter's high bits.
Vovf = 1 → V-Freq counter is overflow, this bit is clear by H/W when condition removed.
VF11 - 8 : 4 high bits of V-Freq counter.

VCNTL (r) : V-Freq counter's low byte.

HVCTR0 (w) : H/V SYNC processor control register 0.
C1, C0 = 1,1 → Select CVSYNC as the polarity, freq and VBLANK source.
= 1,0 → Select VSYNC as the polarity, freq and VBLANK source.
= 0,0 → Disable composite function.
= 0,1 → H/W auto switch to CVSYNC when CVpre=1 and VSpre=0.
NoHins = 1 → HBLANK has no insert pulse in composite mode.
= 0 → HBLANK has insert pulse in composite mode.
HBpl = 1 → negative polarity HBLANK output.
= 0 → positive polarity HBLANK output.
VBpl = 1 → negative polarity VBLANK output.
= 0 → positive polarity VBLANK output.

HVCTR2 (w) : Self-test pattern generator control.
Selft = 1 → enable generator.
= 0 → disable generator.
STF1,STF0 = 1,1 → 63.5KHz(horizontal) output selected.
= 1,0 → 47.6KHz(horizontal) output selected.
= 0,0 → 31.75KHz(horizontal) output selected.
Rt1, Rt0= 0,0 → positive cross-hatch pattern output.
= 0,1 → negative cross-hatch pattern output.
= 1,0 → full white pattern output.
= 1,1 → full black pattern output.
STE = 1 → enable STOUT output.
= 0 → disable STOUT output.

HVCTR3 (w) : HSYNC clamp pulse control register.
CLPEG = 1 → Clamp pulse follows HSYNC leading edge.
= 0 → Clamp pulse follows HSYNC trailing edge.
CLPPO = 1 → Positive polarity clamp pulse output.
= 0 → Negative polarity clamp pulse output.
CLPW2 : CLPW0 : Pulse width of clamp pulse is
[(CLPW2:CLPW0) + 1] x 0.167 μs for 12MHz X'tal selection.

INTFLG (w) : Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 core's INT1 source will be driven by a zero level. Software MUST clear this register while serve the interrupt routine.

HPRchg= 1 → No action.
= 0 → Clear HSYNC presence change flag.
VPRchg= 1 → No action.
= 0 → Clear VSYNC presence change flag.
HPLchg= 1 → No action.
= 0 → Clear HSYNC polarity change flag.
VPLchg= 1 → No action.
= 0 → Clear VSYNC polarity change flag.
HFchg = 1 → No action.
= 0 → Clear HSYNC frequency change flag.
VFchg = 1 → No action.
= 0 → Clear VSYNC frequency change flag.
Vsync = 1 → No action.
= 0 → Clear VSYNC interrupt flag.

INTFLG (r) : Interrupt flag.
HPRchg= 1 → Indicates a HSYNC presence change.
VPRchg= 1 → Indicates a VSYNC presence change.
HPLchg= 1 → Indicates a HSYNC polarity change.
VPLchg= 1 → Indicates a VSYNC polarity change.
HFchg = 1 → Indicates a HSYNC frequency change or counter overflow.
VFchg = 1 → Indicates a VSYNC frequency change or counter overflow.
Vsync = 1 → Indicates a VSYNC interrupt.

INTEN (w) : Interrupt enable.
EHPR = 1 → Enable HSYNC presence change interrupt.
EVPR = 1 → Enable VSYNC presence change interrupt.
EHPL = 1 → Enable HSYNC polarity change interrupt.
EVPL = 1 → Enable VSYNC polarity change interrupt.
EHF = 1 → Enable HSYNC frequency change / counter overflow interrupt.
EVF = 1 → Enable VSYNC frequency change / counter overflow interrupt.
EVsync = 1 → Enable VSYNC interrupt.

7. DDC & IIC Interface

7.1 DDC1 Mode

The MTV212M enters DDC1 mode after Reset. In this mode, VSYNC is used as data clock. The HSCL pin should remain at high. The data output to the HSDA pin is taken from a shift register in MTV212M. The shift register fetch data byte from the DDC1 data buffer (DBUF) then send it in 9 bits packet formats which includes a null bit (=1) as packet separator. The DBUF set the DbufI interrupt flag when the shift register read out the data byte from DBUF. Software needs to write EDID data to DBUF as soon as the DbufI is set. The DbufI interrupt is automatically cleared when Software writes a new data byte to DBUF. The DbufI interrupt can be mask or enable by EDbufI control bit.

7.2 DDC2B Mode

The MTV212M switches to DDC2B mode when it detects a high to low transition on the HSCL pin. Once MTV212M enters DDC2B mode, S/W can set IICpass control bit to allow HOST access EEPROM directly. Under such condition, the HSDA and HSCL are directly bypassed to ISDA and ISCL pins. The other way to perform DDC2 function is to clear IICpass and config the Slave A IIC block to act as EEPROM behavior. The Slave A block's slave address can be chosen by S/W as 5-bits, 6-bits or 7-bits. For example, if S/W choose 5-bits slave address as 10100b, the slave IIC block A will respond to slave address 10100xxb and save the 2 LSB "xx" in XFR. This feature enables MTV212M to meet PC99 requirement.
The MTV212M will return to DDC1 mode if HSCL is kept high for 128 VSYNC clock period. However, it will

lock in DDC2B mode if a valid IIC address (1010xxxb) has been detected on HSCL/HSDA bus. The DDC2 flag reflects the current DDC status, S/W may clear it by writing a "0" to it.

7.3 Slave Mode IIC function Block

The slave mode IIC block is connected to HSDA and HSCL pins. This block can receive/transmit data using IIC protocol. There are 2 slave addresses MTV212M can respond to. S/W may write the SLVAADR/SLVBADR register to determine the slave addresses. The SlaveA address can be configured to 5-bits, 6-bits or 7-bits by S/W setting the SlvAbs1 and SlvAbs0 control bits.
In receive mode, the block first detects IIC slave address match condition then issues a SlvAMI/SlvBMI interrupt. If the matched address is slave A, MTV212M will save the matched address's 2 LSB bits to SlvAlsb1 and SlvAlsb0 register. The data from HSDA is shifted into shift register then written to RCABUF/RCBBUF register when a data byte is received. The first byte loaded is word address (slave address is dropped). This block also generates a RCAI/RCBI (receive buffer full interrupt) every time when the RCABUF/RCBBUF is loaded. If S/W can't read out the RCABUF/RCBBUF in time, the next byte in shift register will not be written to RCABUF/RCBBUF and the slave block return NACK to the master. This feature guarantees the data integrity of communication. The WadrA/WadrB flag can tell S/W that if the data in RCABUF/RCBBUF is a word address.
In transmit mode, the block first detects IIC slave address match condition then issues a SlvAMI/SlvBMI interrupt. In the mean time, the SlvAlsb1/SlvAlsb0 is also updated if the matched address is slave A, and the data pre-stored in the TXABUF/TXBBUF is loaded into shift register, result in TXABUF/TXBBUF empty and generates a TXAI/TXBI (transmit buffer empty interrupt). S/W should write the TXABUF/TXBBUF a new byte for next transfer before shift register empty. Fail to do this will cause data corrupt. The TXAI/TXBI occurs every time when shift register reads out the data from TXABUF/TXBBUF.
The SlvAMI/SlvBMI is cleared by writing "0" to corresponding bit in INTFLG register. The RCAI/RCBI is cleared by reading RCABUF/RCBBUF. The TXAI/TXBI is cleared by writing TXABUF/TXBBUF. If the control bit ENSCL is set, the block will hold HSCL low until the RCAI/RCBI/TXAI/TXBI is cleared.

*Please see the attachments about "Slave IIC Block Timing".

7.4 Master Mode IIC Function Block

The master mode IIC block can be connected to the ISDA /ISCL pins or the HSDA/HSCL pins, select by Msel control bit. Its speed can be selected to 50KHz-400KHz by S/W setting the MIICF1/MIICF0 control bit. The software program can access the external IIC device through this interface. Since the EDID/VDIF data and the display information share the common EEPROM, precaution must be taken to avoid bus conflicting while Msel=0. In DDC1 mode or IICpass=0, the ISCL/ISDA is controlled by MTV212M only. In DDC2 mode and IICpass flag is set, the host may access the EEPROM directly. Software can test the HSCL condition by reading the Hbusy flag, which is set in case of HSCL=0, and keeps high for 100uS after the HSCL's rising edge. S/W can launch the master IIC transmit/receive by clearing the P bit. Once P=0, MTV212M will hold HSCL low to isolate the host's access to EEPROM. A summary of master IIC access is illustrated as follows.

7.4.1. To write IIC Device
1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV212M transmit this byte, a MbufI interrupt will be triggered.
4. Program can write MBUF to transfer next byte or set P bit to stop.
* Please see the attachments about "Master IIC Transmit Timing".

7.4.2. To read IIC Device
1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV212M transmit this byte, a MbufI interrupt will be triggered.
4. Set or reset the MAckO flag according to the IIC protocol.
5. Read out MBUF the useless byte to continue the data transfer.
6. After the MTV212M receives a new byte, the MbufI interrupt is triggered again.
7. Read MBUF also trigger the next receive operation, but set P bit before read can terminate the operation.

* Please see the attachments about "Master IIC Receive Timing".

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IICCTR	00h (r/w)	DDC2					MAckO	P	S
IICSTUS	01h (r)	WadrB	WadrA	SlvRWB	SAckIn	SLVS		SlvAlsb1	SlvAlsb0
IICSTUS	02h (r)	MAckIn	Hifreq	Hbusy					
INTFLG	03h (r)	TXBI	RCBI	SlvBMI	TXAI	RCAI	SlvAMI	DbufI	MbufI
INTFLG	03h (w)			SlvBMI			SlvAMI		MbufI
INTEN	04h (w)	ETXBI	ERCBI	ESlvBMI	ETXAI	ERCAI	ESlvAMI	EDbufI	EMbufI
MBUF	05h (r/w)	Master IIC receive/transmit data buffer							
RCABUF	06h (r)	Slave A IIC receive buffer							
TXABUF	06h (w)	Slave A IIC transmit buffer							
SLVAADR	07h (w)	ENSlvA	Slave A IIC address						
RCBBUF	08h (r)	Slave B IIC receive buffer							
TXBBUF	08h (w)	Slave B IIC transmit buffer							
SLVBADR	09h (w)	ENSlvB	Slave B IIC address						
DBUF	0Ah (w)	DDC1 transmit data buffer							

IICCTR (r/w) : IIC interface control register.

DDC2 = 1 → MTV212M is in DDC2 mode, write "0" can clear it.

= 0 → MTV212M is in DDC1 mode.

MAckO = 1 → In master receive mode, NACK is returned by MTV212M.

= 0 → In master receive mode, ACK is returned by MTV212M.

S, P = ↑, 0 → Start condition when Master IIC is not during transfer.

= X, ↑ → Stop condition when Master IIC is not during transfer.

= 1, X → Will resume transfer after a read/write MBUF operation.

= X, 0 → Force HSCL low and occupy the master IIC bus.

* A write/read MBUF operation can be recognized only after 10us of the MbufI flag's rising edge.

IICSTUS (r) : IIC interface status register.

WadrB = 1 → The data in RCBBUF is word address.

WadrA = 1 → The data in RCABUF is word address.

SlvRWB = 1 → Current transfer is slave transmit

= 0 → Current transfer is slave receive

SAckIn = 1 → The external IIC host respond NACK.

SLVS = 1 → The slave block has detected a START, cleared when STOP detected.

SlvAlsb1,SlvAlsb0 : The 2 LSB which host send to Slave A block.

MAckIn = 1 → Master IIC bus error, no ACK received from the slave IIC device.

= 0 → ACK received from the slave IIC device.

Hifreq = 1 → MTV212M has detected a higher than 200Hz clock on the VSYNC pin.

Hbusy = 1 → Host drives the HSCL pin to low.

INTFLG (w) : Interrupt flag. A interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serve the interrupt routine.

SlvBMI = 1 → No action.

= 0 → Clear SlvBMI flag.

SlvAMI = 1 → No action.

= 0 → Clear SlvAMI flag.

MbufI = 1 → No action.

= 0 → Clear Master IIC bus interrupt flag (MbufI).

INTFLG (r) : Interrupt flag.

TXBI = 1 → Indicates the TXBBUF need a new data byte, clear by writing TXBBUF.
RCBI = 1 → Indicates the RCBBUF has received a new data byte, clear by reading RCBBUF.
SlvBMI = 1 → Indicates the slave IIC address B match condition.
TXAI = 1 → Indicates the TXABUF need a new data byte, clear by writing TXABUF.
RCAI = 1 → Indicates the RCABUF has received a new data byte, clear by reading RCABUF.
SlvAMI = 1 → Indicates the slave IIC address A match condition.
DbufI = 1 → Indicates the DDC1 data buffer need a new data byte, clear by writing DBUF.
MbufI = 1 → Indicates a byte is sent/received to/from the master IIC bus.

INTEN (w) : Interrupt enable.
ETXBI = 1 → Enable TXBBUF interrupt.
ERCBI = 1 → Enable RCBBUF interrupt.
ESlvBMI = 1 → Enable slave address B match interrupt.
ETXAI = 1 → Enable TXABUF interrupt.
ERCAI = 1 → Enable RCABUF interrupt.
ESlvAMI = 1 → Enable slave address A match interrupt.
EDbufI = 1 → Enable DDC1 data buffer interrupt.
EMbufI = 1 → Enable Master IIC bus interrupt.

Mbuf (w) : Master IIC data shift register, after START and before STOP condition, write this register will resume MTV212M's transmission to the IIC bus.

Mbuf (r) : Master IIC data shift register, after START and before STOP condition, read this register will resume MTV212M's receiving from the IIC bus.

RCABUF (r) : Slave IIC block A receive data buffer.

TXABUF (w) : Slave IIC block A transmit data buffer.

SLVAADR (w) : Slave IIC block A's enable and address.
ENslvA = 1 → Enable slave IIC block A.
= 0 → Disable slave IIC block A.
bit6-0 : Slave IIC address A to which the slave block should respond.

RCBBUF (r) : Slave IIC block B receive data buffer.

TXBBUF (w) : Slave IIC block B transmit data buffer.

SLVBADR (w) : Slave IIC block B's enable and address.
ENslvB = 1 → Enable slave IIC block B.
= 0 → Disable slave IIC block B.
bit6-0 : Slave IIC address B to which the slave block should respond.

8. Low Power Reset (LVR) & Watchdog Timer

When the voltage level of power supply is below 4.0V for a specific time, the LVR will generate a chip reset signal. After the power supply is above 4.0V, LVR maintain in reset state for 144 Xtal cycle to guarantee the chip exit reset condition with a stable X'tal oscillation.

The WatchDog Timer automatically generates a device reset when it is overflow. The interval of overflow is 0.25 sec x N, where N is a number from 1 to 8, and can be programmed via register WDT(2:0). The timer function is disabled after power on reset, user can activate this function by setting WEN, and clear the timer by set WCLR.

9. A/D converter

The MTV212M is equipped with four 6-bit A/D converters, S/W can select the current convert channel by setting the SADC1/SADC0 bit. The refresh rate for the ADC is OSC freq./12288. The ADC compare the input pin voltage with internal VDD*N/64 voltage (where N = 0 - 63). The ADC output value is N when pin voltage is greater than VDD*N/64 and smaller than VDD*(N+1)/64.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ADC	10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	10h (r)			ADC convert Result					
WDT	18h (w)	WEN	WCLR				WDT2	WDT1	WDT0

WDT (w) : Watchdog Timer control register.

WEN	= 1	→ Enable WatchDog Timer.
WCLR	= 1	→ Clear WatchDog Timer.
WDT2: WDT0	= 0	→ overflow interval = 8 x 0.25 sec.
	= 1	→ overflow interval = 1 x 0.25 sec.
	= 2	→ overflow interval = 2 x 0.25 sec.
	= 3	→ overflow interval = 3 x 0.25 sec.
	= 4	→ overflow interval = 4 x 0.25 sec.
	= 5	→ overflow interval = 5 x 0.25 sec.
	= 6	→ overflow interval = 6 x 0.25 sec.
	= 7	→ overflow interval = 7 x 0.25 sec.

ADC (w) : ADC control.

ENADC	= 1	→ Enable ADC.
SADC0	= 1	→ Select ADC0 pin input.
SADC1	= 1	→ Select ADC1 pin input.
SADC2	= 1	→ Select ADC2 pin input.
SADC3	= 1	→ Select ADC3 pin input.

ADC (r) : ADC convert result.

10. USB Engine

The USB engine includes the Serial Interface Engine (SIE), the low-speed USB I/O transceiver and the 3.3 Volt Regulator. The SIE block performs most of the USB interface function with only minimum support from S/W. Two endpoints are supported. Endpoint 0 is used to receive and transmit control (including SETUP) packets while Endpoint 1 is only used to transmit data packets.
The USB SIE handles the following USB bus activity independently:

1. Bitstuffing/unstuffing
2. CRC generation/checking
3. ACK/NAK
4. TOKEN type identification
5. Address checking

S/W handles the following tasks:

1. Coordinate enumeration by responding to SETUP packets
2. Fill and empty the FIFOs
3. Suspend/Resume coordination
4. Verify and select DATA toggle values

<u>10.1 USB Device Address</u>
The USBADR register stores the device address. This register is reset to all 0 after chip reset or USB bus

reset. S/W must write this register a valid value after the USB enumeration process.

10.2 Endpoint 0 receive

After receiving a packet and placing the data into the Endpoint 0 receive FIFO (RC0FIFO), MTV212M updates the Endpoint 0 status register (EP0STUS) to record the receive status and then generates an Endpoint 0 receive interrupt (RC0I). S/W can read the EP0STUS register for the recent transfer information, which includes the data byte count (RC0cnt), data direction (EP0dir), SETUP token flag (EP0set) and data valid flag (RC0err). The received data is always stored into RC0FIFO and the RC0cnt is always updated for DATA packets following SETUP tokens. The data following an OUT token is written into the RC0FIFO, and the RC0cnt is updated unless Endpoint 0 STALL (EP0stall) or Endpoint 0 receive NAK (RC0nak) is set. The RC0I interrupt will happen in case where the RC0cnt/RC0FIFO is updated.

10.3 Endpoint 0 transmit

After detecting a valid Endpoint 0 IN token, MTV212M automatically transmit the data pre-stored in the Endpoint 0 transmit FIFO (TX0FIFO) to the USB bus if the Endpoint 0 transmit ready flag (TX0rdy) is set and the EP0stall is cleared. The number of byte to be transmitted is base on the Endpoint 0 transmit byte count register (TX0cnt). The DATA0/1 token to be transmitted is base on the Endpoint 0 transmit toggle control bit (TX0tgl). After the TX0FIFO is updated, TX0rdy should be set to 1. This enables the MTV212M to respond to an Endpoint 0 IN packet. TX0rdy is cleared and an Endpoint 0 transmit interrupt (TX0I) is generated once the USB host acknowledges the data transmission. The interrupt service routine can check TX0rdy to confirm that the data transfer was successful.

10.4 Endpoint 1 transmit

Endpoint 1 is capable of transmit only. This endpoint is enable when the Endpoint1 configured control bit (EP1Cfgd) is set. After detecting a valid Endpoint 1 IN token, MTV212M automatically transmit the data pre-stored in the Endpoint 1 transmit FIFO (TX1FIFO) to the USB bus if the Endpoint 1 transmit ready flag (TX1rdy) is set and the EP1stall is cleared. The number of byte to be transmitted is base on the Endpoint 1 transmit byte count register (TX1cnt). The DATA0/1 token to be transmitted is base on the Endpoint 1 transmit toggle control bit (TX1tgl). After the TX1FIFO is updated, TX1rdy should be set to 1. This enables the MTV212M to respond to an Endpoint 1 IN packet. TX1rdy is cleared and an Endpoint 1 transmit interrupt (TX1I) is generated once the USB host acknowledges the data transmission. The interrupt service routine can check TX0rdy to confirm that the data transfer was successful.

10.5 USB Control and Status

Other USB control bits include the USB enable (ENUSB), SUSPEND (Susp), RESUME (RsmO), Control Read (CtrRD), and corresponding interrupt enable bits. The CtrRD should be set when program detects the current transfer is an Endpoint0 Control Read Transfer. Once this bit is set, the MTV212M will stall an Endpoint0 OUT packet with DATA toggle 0 or byte count other than 0. Other USB status flag includes the USB reset interrupt (USBrstI), RESUME interrupt (RsmI), and USB bus active flag (USBactv). The USBactv flag is set once the MTV212M detect the USB bus activity. S/W should read and clear it every 3 ms to identify the suspend condition. Writing a "1" to the USBactv flag will not change its value.

10.6 Suspend and Resume

Once the Suspend condition is asserted, S/W can set the Susp bit to stop the USBSIE's clock. In the mean time, the 3.3V Regulator is operating in low power mode. S/W can further save the device power by force the 8051 CPU core into the Power Down or Idle mode by setting the PCON register in SFR area. In the Idel mode, the X'tal keeps oscillating and CPU can be waken-up by the trigger of any enabled interrupt. In the Power Down mode, the X'tal is stop, but CPU can be waken-up by the trigger of enabled INT1's source. In short, S/W can keep the RsmI alive before enter the suspend mode.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
USBADR	60h (r/w)	ENUSB	USBadr						
INTFLG	61h (r/w)	USBrstI	RC0I	TX1I	TX0I	RsmI			
INTEN	62h (w)	EUrstI	ERC0I	ETX1I	ETX0I	ERsmI			
EP0STUS	63h (r)	RC0tgl	RC0err	EP0dir	EP0set	RC0cnt			

USBCTR	64h (r/w)	Susp	RsmO	EP1cfgd	RC0nak	CtrRD			USBactv
TX0CTR	65h (w)	TX0rdy	TX0tgl	EP0stall		TX0cnt			
TX0CTR	65h (r)	TX0rdy	TX0tgl	EP0stall					
TX1CTR	66h (w)	TX1rdy	TX1tgl	EP1stall		TX1cnt			
TX1CTR	66h (r)	TX1rdy	TX1tgl	EP1stall					
RC0FIFO	68h (r)	Endpoint 0 receive FIFO 1st byte							
RC0FIFO	69h (r)	Endpoint 0 receive FIFO 2nd byte							
RC0FIFO	6Ah (r)	Endpoint 0 receive FIFO 3rd byte							
RC0FIFO	6Bh (r)	Endpoint 0 receive FIFO 4th byte							
RC0FIFO	6Ch (r)	Endpoint 0 receive FIFO 5th byte							
RC0FIFO	6Dh (r)	Endpoint 0 receive FIFO 6th byte							
RC0FIFO	6Eh (r)	Endpoint 0 receive FIFO 7th byte							
RC0FIFO	6Fh (r)	Endpoint 0 receive FIFO 8th byte							
TX0FIFO	70h (w)	Endpoint 0 transmit FIFO 1st byte							
TX0FIFO	71h (w)	Endpoint 0 transmit FIFO 2nd byte							
TX0FIFO	72h (w)	Endpoint 0 transmit FIFO 3rd byte							
TX0FIFO	73h (w)	Endpoint 0 transmit FIFO 4th byte							
TX0FIFO	74h (w)	Endpoint 0 transmit FIFO 5th byte							
TX0FIFO	75h (w)	Endpoint 0 transmit FIFO 6th byte							
TX0FIFO	76h (w)	Endpoint 0 transmit FIFO 7th byte							
TX0FIFO	77h (w)	Endpoint 0 transmit FIFO 8th byte							
TX1FIFO	78h (w)	Endpoint 1 transmit FIFO 1st byte							
TX1FIFO	79h (w)	Endpoint 1 transmit FIFO 2nd byte							
TX1FIFO	7Ah (w)	Endpoint 1 transmit FIFO 3rd byte							
TX1FIFO	7Bh (w)	Endpoint 1 transmit FIFO 4th byte							
TX1FIFO	7Ch (w)	Endpoint 1 transmit FIFO 5th byte							
TX1FIFO	7Dh (w)	Endpoint 1 transmit FIFO 6th byte							
TX1FIFO	7Eh (w)	Endpoint 1 transmit FIFO 7th byte							
TX1FIFO	7Fh (w)	Endpoint 1 transmit FIFO 8th byte							

USBADR (r/w) : USB device address and enable.

ENUSB	= 1	→ Enable USB function, clear while chip reset.
USBadr :		USB device address, clear while chip reset or USB bus reset.

INTFLG (w) : Interrupt flag. A interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serve the interrupt routine.

USBrstI	= 1	→ No action.
	= 0	→ Clear USBrstI flag.
RC0I	= 1	→ No action.
	= 0	→ Clear RC0I flag.
TX1I	= 1	→ No action.
	= 0	→ Clear TX1I flag.
TX0I	= 1	→ No action.
	= 0	→ Clear TX0I flag.
RsmI	= 1	→ No action.
	= 0	→ Clear RsmI flag.

INTFLG (r) : Interrupt flag.

USBrstI	= 1	→ Indicates the USB bus reset condition.
RC0I	= 1	→ Endpoint 0 has completed a receive transfer and save the data in RC0FIFO.
TX1I	= 1	→ Endpoint 1 has completed a transmit transfer and empty TX1FIFO.

TX0I = 1 → Endpoint 0 has completed a transmit transfer and empty TX0FIFO.
RsmI = 1 → Indicates the USB bus RESUME condition in suspend mode.

INTEN (w) : Interrupt enable.
EUrstI = 1 → Enable USBrstI interrupt.
ERC0I = 1 → Enable RC0I interrupt.
ETX1I = 1 → Enable TX1I interrupt.
ETX0I = 1 → Enable TX0I interrupt.
ERsmI = 1 → Enable RsmI interrupt.

EP0STUS (r) : Endpoint 0 status.
RC0tgl = 1 → Receive a DATA1 packet.
= 0 → Receive a DATA0 packet.
RC0err = 1 → Receive DATA packet error.
= 0 → Receive DATA packet good.
EP0dir = 1 → Last transfer is transmit direction (IN).
= 0 → Last transfer is receive direction (OUT, SETUP).
EP0set = 1 → Last transfer is a SETUP.
= 0 → Last transfer is not a SETUP.
RC0cnt : Last transfer's receive byte count.

USBCTR (r/w) : USB control register.
Susp = 1 → S/W force USB interface into suspend mode.
RsmO = 1 → S/W force USB interface into send RESUME signal in suspend mode.
EP1cfgd = 1 → Endpoint 1 is configed.
RC0nak = 1 → Endpoint 0 will respond NAK to OUT token.
CtrRD = 1 → MTV212M will stall a invalid OUT token during Control Read transfer.
USBactv = 1 → MTV212M detects USB bus activity, clear by S/W writing "0".

TX0CTR (r/w) : Endpoint 0 transmit control register.
TX0rdy = 1 → Enable the Endpoint 0 to respond to IN token.
= 0 → Endpoint 0 will respond NAK to IN token.
This bit can be set or cleared by S/W, clear by H/W while Host acknowledge the transfer.
TX0tgl = 1 → Endpoint 0 will transmit DATA1 packet.
= 0 → Endpoint 0 will transmit DATA0 packet.
EP0stall = 1 → Endpoint 0 will stall OUT/IN packet.
TX0cnt : Endpoint 0 transmit byte count, write only.

TX1CTR (r/w) : Endpoint 1 transmit control register.
TX1rdy = 1 → Enable the Endpoint 1 to respond to IN token.
= 0 → Endpoint 1 will respond NAK to IN token.
This bit can be set or cleared by S/W, clear by H/W while Host acknowledge the transfer.
TX1tgl = 1 → Endpoint 1 will transmit DATA1 packet.
= 0 → Endpoint 1 will transmit DATA0 packet.
EP1stall = 1 → Endpoint 1 will stall IN packet.
TX1cnt : Endpoint 1 transmit byte count, write only.

RC0FIFO (r) : Endpoint 0 receive FIFO registers.

TX0FIFO (w) : Endpoint 0 transmit FIFO registers.

TX1FIFO (w) : Endpoint 1 transmit FIFO registers.

Memory Map of XFR

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IICCTR	00h (r/w)	DDC2					MAckO	P	S
IICSTUS	01h (r)	WadrB	WadrA	SlvRWB	SAckIn	SLVS		SlvAlsb1	SlvAlsb0
IICSTUS	02h (r)	MAckIn	Hifreq	Hbusy					
INTFLG	03h (r)	TXBI	RCBI	SlvBMI	TXAI	RCAI	SlvAMI	DbufI	MbufI
INTFLG	03h (w)			SlvBMI			SlvAMI		MbufI
INTEN	04h (w)	ETXBI	ERCBI	ESlvBMI	ETXAI	ERCAI	ESlvAMI	EDbufI	EMbufI
MBUF	05h (r/w)	Master IIC receive/transmit data buffer							
RCABUF	06h (r)	Slave A IIC receive buffer							
TXABUF	06h (w)	Slave A IIC transmit buffer							
SLVAADR	07h (w)	ENSlvA	Slave A IIC address						
RCBBUF	08h (r)	Slave B IIC receive buffer							
TXBBUF	08h (w)	Slave B IIC transmit buffer							
SLVBADR	09h (w)	ENSlvB	Slave B IIC address						
DBUF	0Ah (w)	DDC1 transmit data buffer							
ADC	10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	10h (r)			ADC convert Result					
WDT	18h (w)	WEN	WCLR				WDT2	WDT1	WDT0
DA0	20h (r/w)	Pulse width of PWM DAC 0							
DA1	21h (r/w)	Pulse width of PWM DAC 1							
DA2	22h (r/w)	Pulse width of PWM DAC 2							
DA3	23h (r/w)	Pulse width of PWM DAC 3							
DA4	24h (r/w)	Pulse width of PWM DAC 4							
DA5	25h (r/w)	Pulse width of PWM DAC 5							
DA6	26h (r/w)	Pulse width of PWM DAC 6							
DA7	27h (r/w)	Pulse width of PWM DAC 7							
DA8	28h (r/w)	Pulse width of PWM DAC 8							
DA9	29h (r/w)	Pulse width of PWM DAC 9							
DA10	2Ah (r/w)	Pulse width of PWM DAC 10							
DA11	2Bh (r/w)	Pulse width of PWM DAC 11							
DA12	2Ch (r/w)	Pulse width of PWM DAC 12							
DA13	2Dh (r/w)	Pulse width of PWM DAC 13							
PADMOD	30h (w)	DA13E	DA12E	DA11E	DA10E	AD3E	AD2E	AD1E	AD0E
PADMOD	31h (w)		P56E	P55E	P54E	P53E	P52E	P51E	P50E
PADMOD	32h (w)	HIICE	IIICE	HLFVE	HLFHE	HCLPE	P42E	P41E	P40E
OPTION	33h (w)	PWMF	DIV253	FclkE	IICpass	ENSCL	Msel	MIICF1	MIICF0
OPTION	34h (w)							SlvAbs1	SlvAbs0
XBANK	35h (r/w)						Xbnk2	Xbnk1	Xbnk0
PORT4	38h (w)						P42	P41	P40
PORT5	39h (r/w)		P56	P55	P54	P53	P52	P51	P50
HVSTUS	40h (r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	41h (r)	Hovf		HF13	HF12	HF11	HF10	HF9	HF8
HCNTL	42h (r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	43h (r)	Vovf				VF11	VF10	VF9	VF8
VCNTL	44h (r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR0	40h (w)	C1	C0	NoHins				HBpl	VBpl
HVCTR2	42h (w)			Selft	STF1	STF0	Rt1	Rt0	STE
HVCTR3	43h (w)		CLPEG	CLPPO	CLPW2	CLPW1	CLPW0		
INTFLG	48h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg		Vsync
INTEN	49h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF		EVsync

USBADR	60h (r/w)	ENUSB	USBadr						
INTFLG	61h (r/w)	USBrstI	RC0I	TX1I	TX0I	RsmI			
INTEN	62h (w)	EUrstI	ERC0I	ETX1I	ETX0I	ERsmI			
EP0STUS	63h (r)	RC0tgl	RC0err	EP0dir	EP0set	RC0cnt			
USBCTR	64h (r/w)	Susp	RsmO	EP1cfgd	RC0nak	CtrRD			USBactv
TX0CTR	65h (w)	TX0rdy	TX0tgl	EP0stall		TX0cnt			
TX0CTR	65h (r)	TX0rdy	TX0tgl	EP0stall					
TX1CTR	66h (w)	TX1rdy	TX1tgl	EP1stall		TX1cnt			
TX1CTR	66h (r)	TX1rdy	TX1tgl	EP1stall					
RC0FIFO	68h (r)	Endpoint 0 receive FIFO 1st byte							
RC0FIFO	69h (r)	Endpoint 0 receive FIFO 2nd byte							
RC0FIFO	6Ah (r)	Endpoint 0 receive FIFO 3rd byte							
RC0FIFO	6Bh (r)	Endpoint 0 receive FIFO 4th byte							
RC0FIFO	6Ch (r)	Endpoint 0 receive FIFO 5th byte							
RC0FIFO	6Dh (r)	Endpoint 0 receive FIFO 6th byte							
RC0FIFO	6Eh (r)	Endpoint 0 receive FIFO 7th byte							
RC0FIFO	6Fh (r)	Endpoint 0 receive FIFO 8th byte							
TX0FIFO	70h (w)	Endpoint 0 transmit FIFO 1st byte							
TX0FIFO	71h (w)	Endpoint 0 transmit FIFO 2nd byte							
TX0FIFO	72h (w)	Endpoint 0 transmit FIFO 3rd byte							
TX0FIFO	73h (w)	Endpoint 0 transmit FIFO 4th byte							
TX0FIFO	74h (w)	Endpoint 0 transmit FIFO 5th byte							
TX0FIFO	75h (w)	Endpoint 0 transmit FIFO 6th byte							
TX0FIFO	76h (w)	Endpoint 0 transmit FIFO 7th byte							
TX0FIFO	77h (w)	Endpoint 0 transmit FIFO 8th byte							
TX1FIFO	78h (w)	Endpoint 1 transmit FIFO 1st byte							
TX1FIFO	79h (w)	Endpoint 1 transmit FIFO 2nd byte							
TX1FIFO	7Ah (w)	Endpoint 1 transmit FIFO 3rd byte							
TX1FIFO	7Bh (w)	Endpoint 1 transmit FIFO 4th byte							
TX1FIFO	7Ch (w)	Endpoint 1 transmit FIFO 5th byte							
TX1FIFO	7Dh (w)	Endpoint 1 transmit FIFO 6th byte							
TX1FIFO	7Eh (w)	Endpoint 1 transmit FIFO 7th byte							
TX1FIFO	7Fh (w)	Endpoint 1 transmit FIFO 8th byte							

Test Mode Condition

In normal application, users should avoid the MTV212M entering its test/program mode, outlined as follow:
Test Mode A: RESET=1 & DA9=1 & DA8=0 & STO=0
Test Mode B: RESET's falling edge & DA9=1 & DA8=0 & STO=1
Program Mode: RESET=1 & DA9=0 & DA8=1

ELECTRICAL PARAMETERS

1. Absolute Maximum Ratings

at: Ta= 0 to 70 °C, VSS=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to +6.0	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum Output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	0 to +70	°C
Maximum Storage Temperature	Tstg	-25 to +125	°C

2. Allowable Operating Conditions

at: Ta= 0 to 70 °C, VSS=0V

Name	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	4.5	5.5	V
Input "H" Voltage	Vih1	0.4 x VDD	VDD +0.3	V
Input "L" Voltage	Vil1	-0.3	0.2 x VDD	V
Operating Freq.	Fopg	-	15	MHz

3. DC Characteristics

at: Ta=0 to 70 °C, VDD=5.0V, VSS=0V

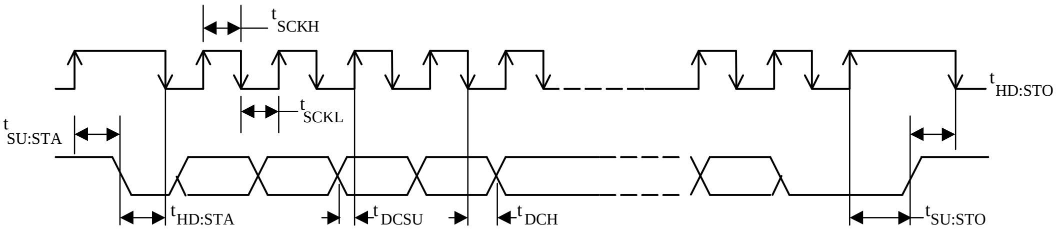
Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Output "H" Voltage, open drain pin	Voh1	Ioh=0uA	4			V
Output "H" Voltage, 8051 I/O port pin	Voh2	Ioh=-50uA	4			V
Output "H" Voltage, pin HBLANK, VBLANK, STOUT	Voh3	Ioh=-2mA	4			V
Output "L" Voltage	Vol	Iol=6mA			0.45	V
Power Supply Current	Idd	Active		18	24	mA
		Idle		1.3	4.0	mA
		Power-Down		50	80	uA
RST Pull-Down Resistor	Rrst	VDD=5V	50		150	Kohm
Pin Capacitance	Cio				15	pF

4. AC Characteristics

at: Ta=0 to 70 °C, VDD=5.0V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal Frequency	fXtal			12		MHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		94.86	KHz
HS input pulse Width	tHIPW	fXtal=12MHz	0.3		8	uS
VS input pulse Width	tVIPW	fXtal=12MHz	3			uS
HSYNC to Hblank output jitter	tHHBJ				5	nS
H+V to Vblank output delay	tVVBD	fXtal=12MHz		10		uS
VS pulse width in H+V signal	tVCPW	FXtal=12MHz	20			uS
SDA to SCL setup time	tDCSU		200			ns

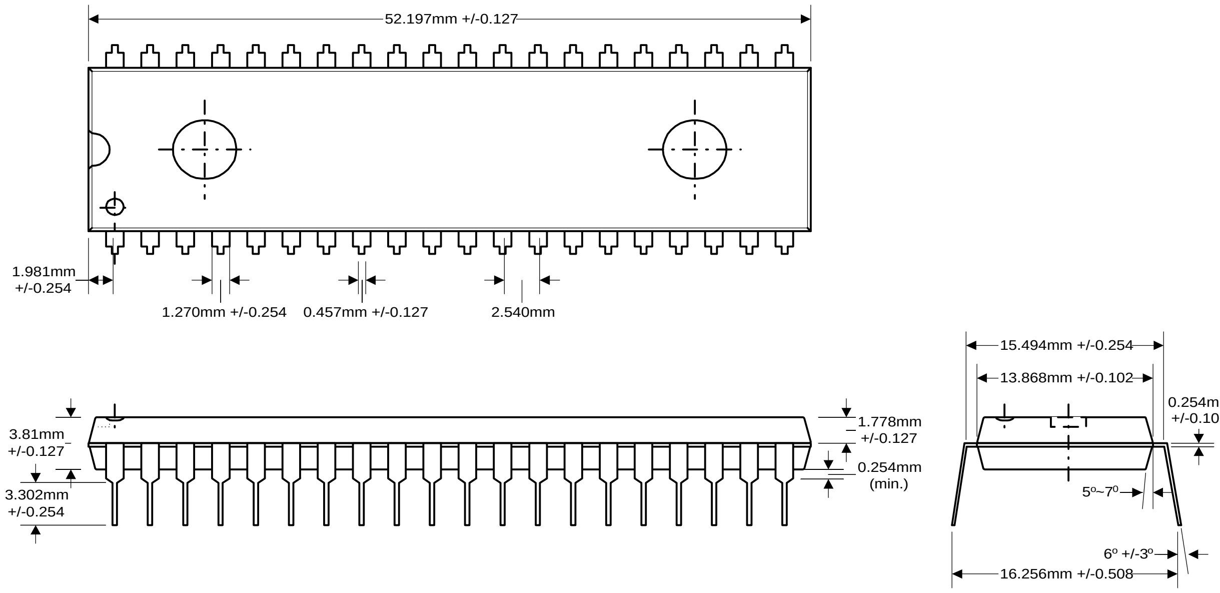
SDA to SCL hold time	tDCH		100			ns
SCL high time	tSCLH		500			ns
SCL low time	tSCLL		500			ns
START condition setup time	tSU:STA		500			ns
START condition hold time	tHD:STA		500			ns
STOP condition setup time	tSU:STO		500			ns
STOP condition hold time	tHD:STO		500			ns



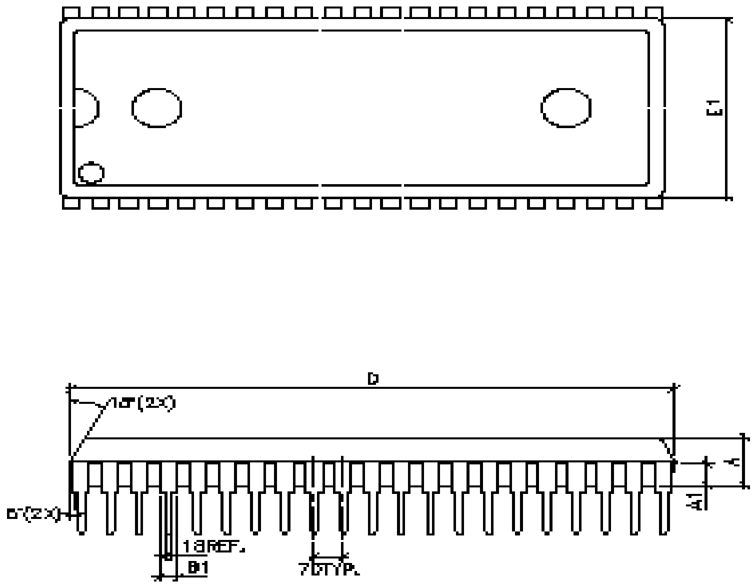
Data interface timing (I^2C)

PACKAGE DIMENSION

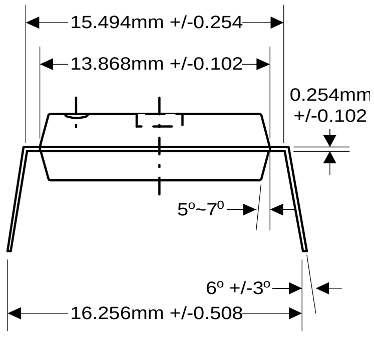
1. 40-pin PDIP 600 mil



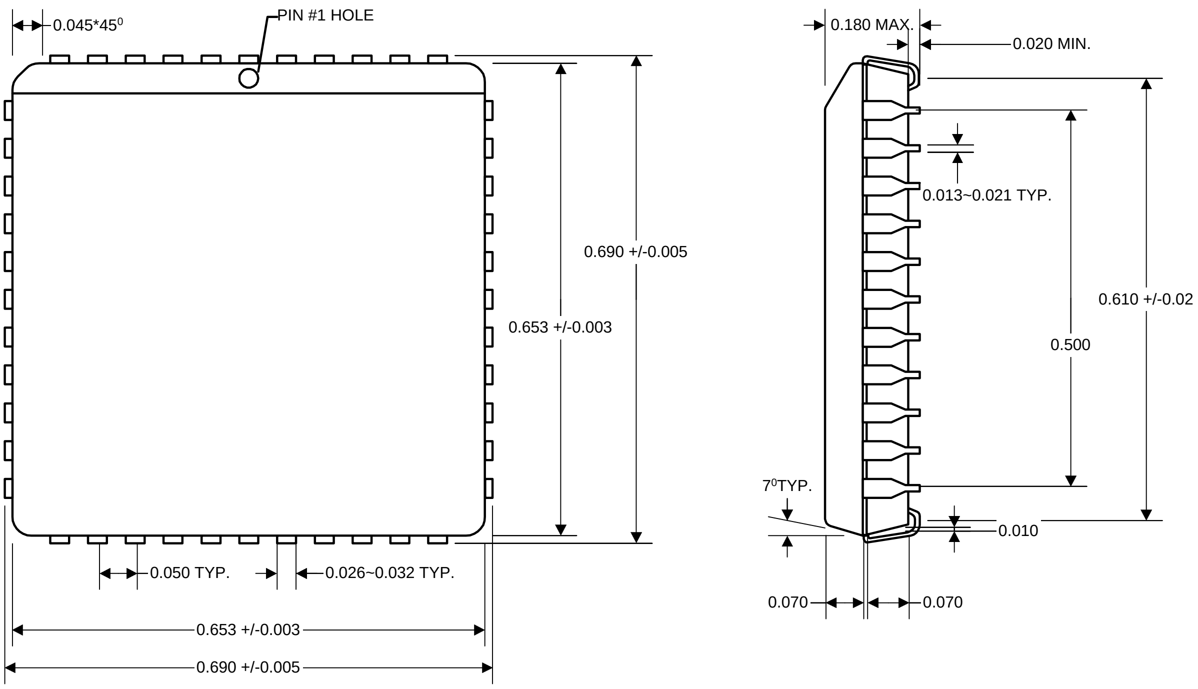
2. 42 pin SDIP Unit: mm



Symbol	Dimension in mm		
	Min	Nom	Max
A	3.937	4.064	4.2
A1	1.78	1.842	1.88
B1	0.914	1.270	1.118
D	36.78	36.83	36.88
E1	13.945	13.970	13.995
F	15.19	15.240	15.29
eB	15.24	16.510	17.78
θ	0°	7.5°	15°



3. 44 pin PLCC Unit:



Ordering Information

Standard configurations:

Prefix	Part Type	Package Type	ROM Size (K)	USB Option
MTV	212M	N: PDIP S:SDIP V: PLCC	64	Non-USB: N/A USB: U

Part Numbers:

Prefix	Part Type	Package Type	ROM Size (K)	USB Option
MTV	212M	N	64	
MTV	212M	S	64	
MTV	212M	V	64	
MTV	212M	N	64	U
MTV	212M	S	64	U
MTV	212M	V	64	U