MTE125N20E

Motorola Preferred Device

Designer's™ Data Sheet

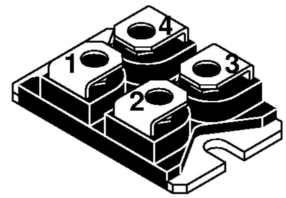
ISOTOP™ TMOS E-FET™ Power Field Effect Transistor

N–Channel Enhancement–Mode Silicon Gate

TMOS POWER FET
125 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.015 OHM

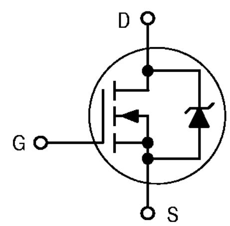
This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- 2500 V RMS Isolated Isotop Package
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- Very Low Internal Parasitic Inductance
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- U.L. Recognized, File #E69369



SOT–227B

1. Source
2. Gate
3. Drain
4. Source 2



MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10\ \mu s$)	I_D I_D I_{DM}	125 79 500	Adc
Total Power Dissipation Derate above 25°C	P_D	460 3.70	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–40 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, I_L = 125 Apk, L = 0.05mH, R_G = 25 Ω)	E_{AS}	400	mJ
RMS Isolation Voltage	V_{ISO}	2500	Vac
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.28 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8 from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

E–FET is a trademark of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.
ISOTOP is a trademark of SGS–THOMSON Microelectronics.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	200	215	—	Vdc
Temperature Coefficient (Positive)			—	250	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	200	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	—	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 62.5 Adc)		$R_{DS(on)}$	—	12	15	mOhm
Drain–Source On–Voltage (V_{GS} = Vdc) (I_D = 125 Adc)		$V_{DS(on)}$	—	—	2.1	Vdc
(I_D = 62.5 Adc, T_J = 125°C)			—	—	1.9	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 62.5 Adc)		g_{FS}	50	80	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	14400	—	pF
Output Capacitance		C_{oss}	—	3600	—	
Reverse Transfer Capacitance		C_{rss}	—	920	—	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 125 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	72	—	ns
Rise Time		t_r	—	574	—	
Turn–Off Delay Time		$t_{d(off)}$	—	327	—	
Fall Time		t_f	—	376	—	
Gate Charge	(V_{DS} = 160 Vdc, I_D = 125 Adc, V_{GS} =10 Vdc)	Q_T	—	510	—	nC
		Q_1	—	100	—	
		Q_2	—	245	—	
		Q_3	—	158	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 125 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.00	1.5	Vdc
	(I_S = 125 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.00	—	
Reverse Recovery Time	(I_S = 125 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	310	—	ns
		t_a	—	220	—	
		t_b	—	90	—	
Reverse Recovery Stored Charge		Q_{RR}	—	9.2	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25 from package to center of die)			—	5.0	—	
Internal Source Inductance (Measured from the source lead 0.25 from package to source bond pad)		L_S	—	5.0	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

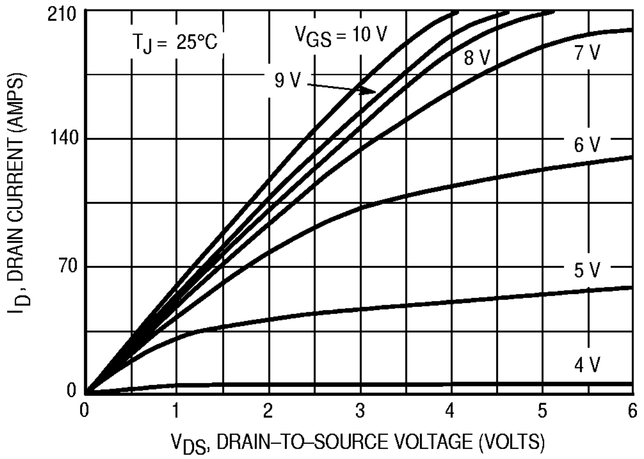


Figure 1. On–Region Characteristics

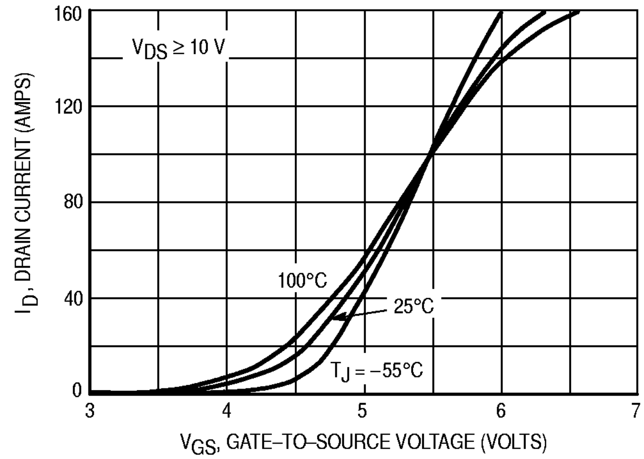


Figure 2. Transfer Characteristics

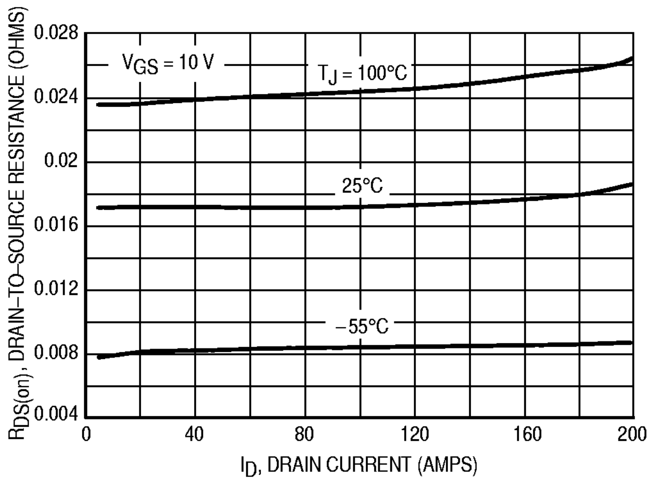


Figure 3. On–Resistance versus Drain Current and Temperature

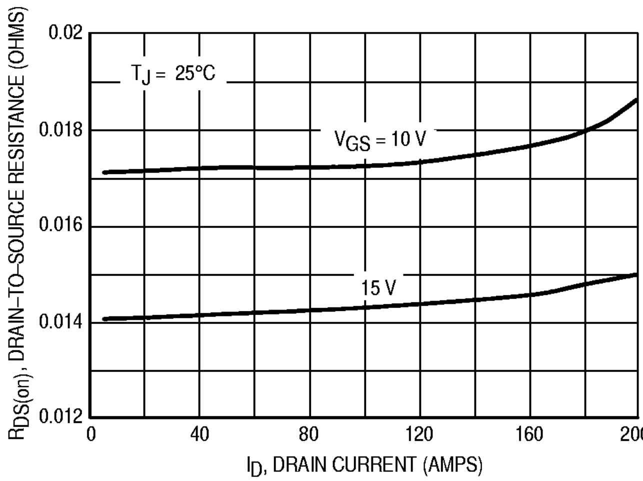


Figure 4. On–Resistance versus Drain Current and Gate Voltage

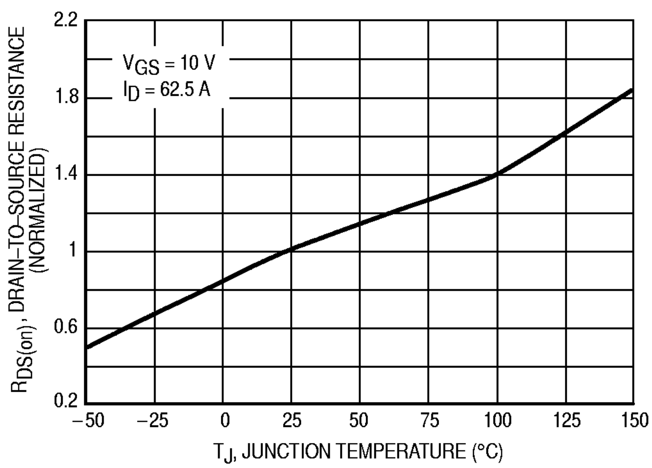


Figure 5. On–Resistance Variation with Temperature

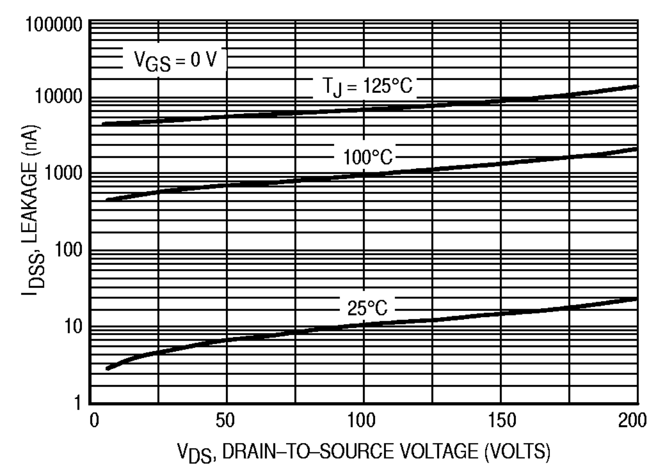


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \ln\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \ln\ (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

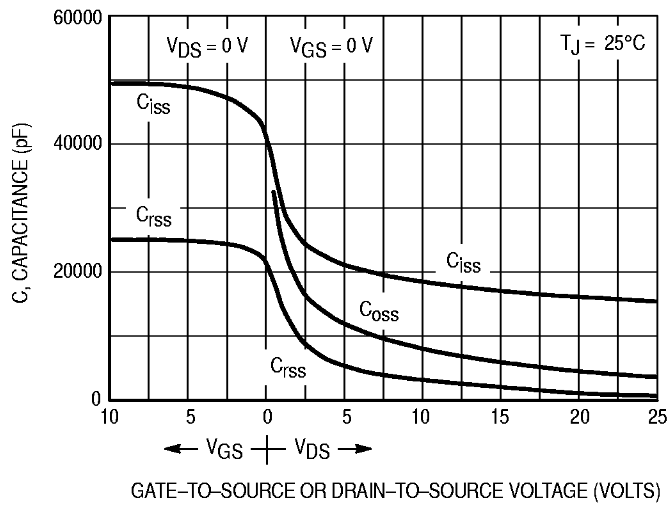


Figure 7. Capacitance Variation

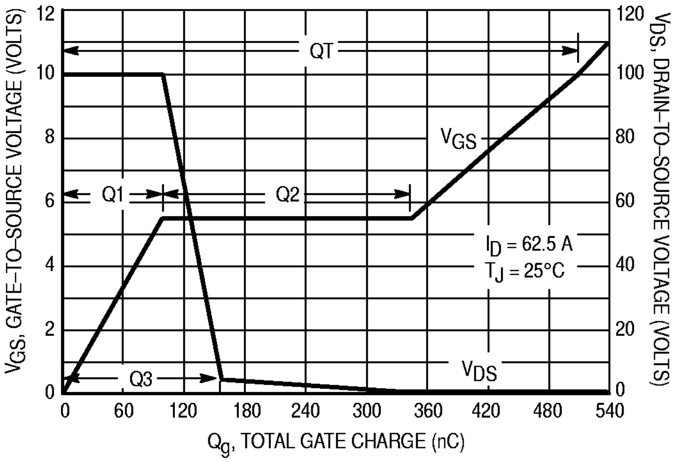


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

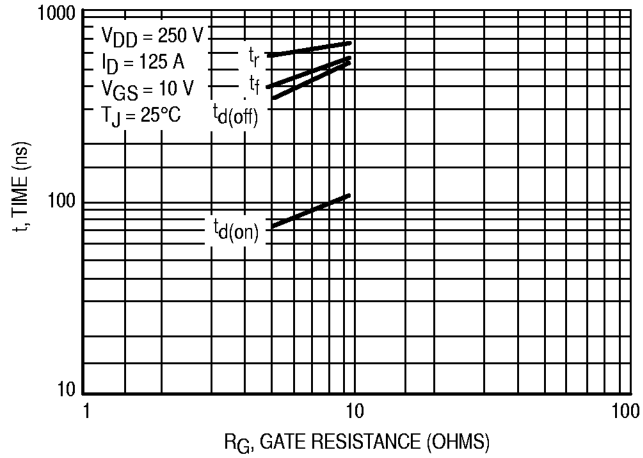


Figure 9. Resistive Switching Time Variation versus Gate Resistance

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

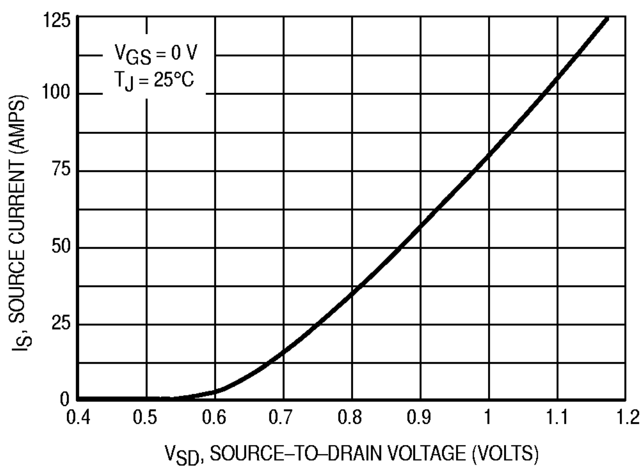


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

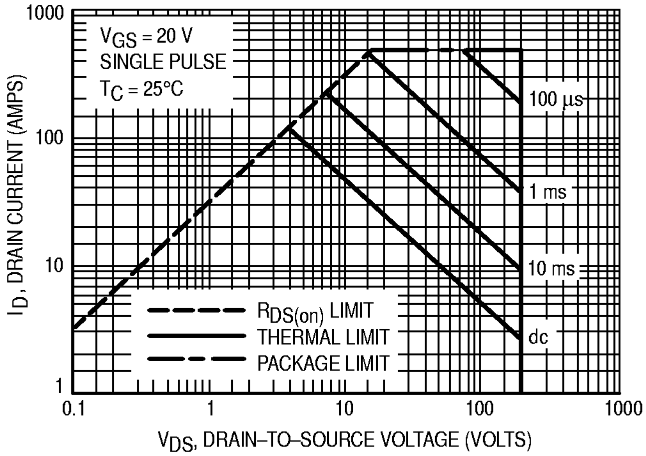


Figure 11. Maximum Rated Forward Biased Safe Operating Area

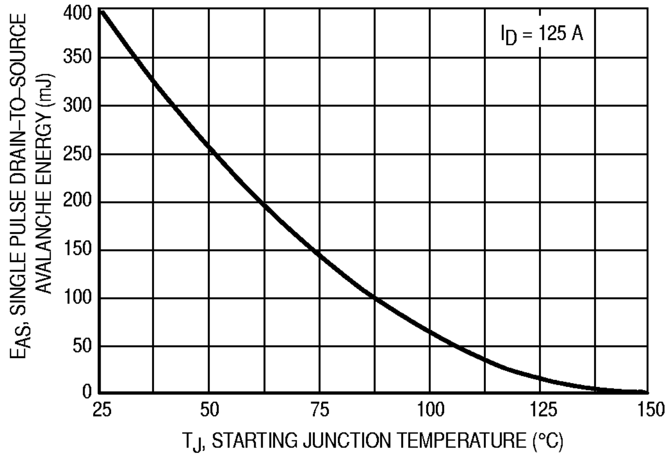


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

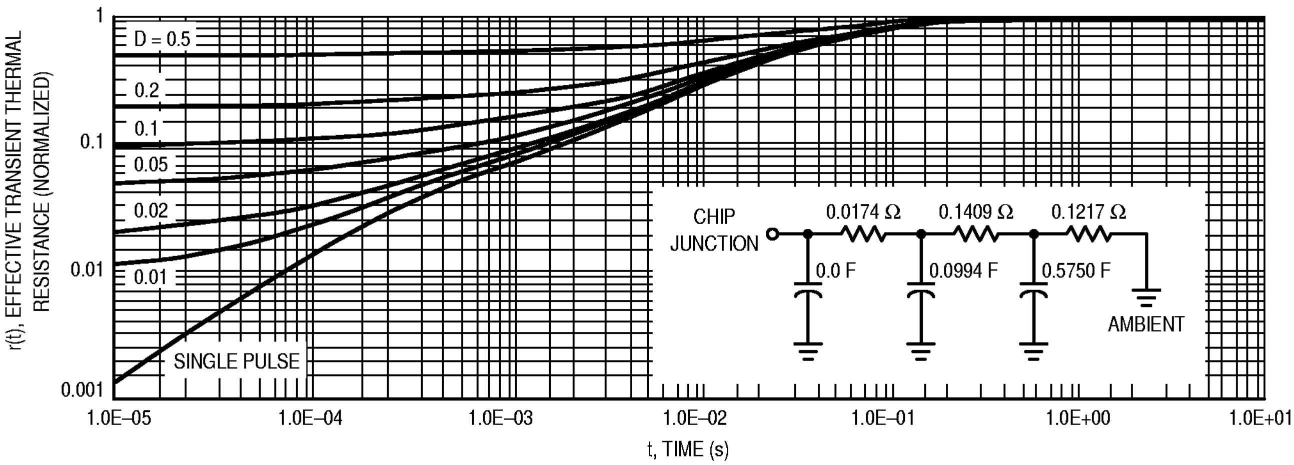


Figure 13. Thermal Response

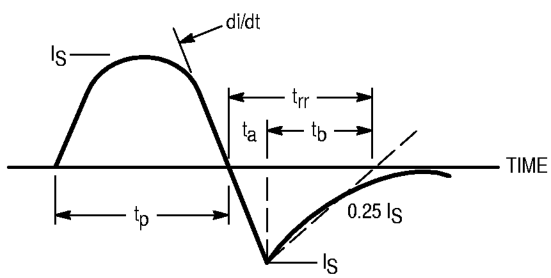
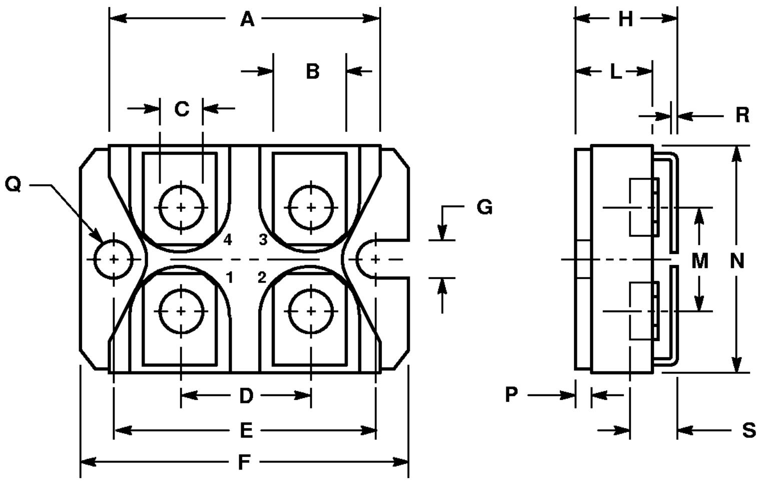


Figure 14. Diode Reverse Recovery Waveform

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	31.70	1.240	1.248
B	7.80	8.20	0.307	0.322
C	4.10	4.30	0.161	0.169
D	14.90	15.10	0.586	0.590
E	30.10	30.30	1.185	1.193
F	38.00	38.20	1.496	1.503
G	4.00	—	0.157	—
H	11.80	12.20	0.464	0.480
L	8.90	9.10	0.350	0.358
M	12.60	12.80	0.496	0.503
N	25.20	25.40	0.992	1.000
P	1.95	2.05	0.076	0.080
Q	4.10	—	0.157	—
R	0.75	0.85	0.030	0.033
S	5.50	—	0.217	—

Recommended screw torque: 1.3 ± 0.2 Nm
Maximum screw torque: 1.5 Nm

STYLE 1:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SOURCE 2

SOT–227B

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MOTOROLA