1.0 Key Features

- Line Interface Circuit for Automotive Multiplex Systems
- Fully Integrated Support for the VAN Protocol (layer 1 of the OSI model)
- Integrates:
  - Interface protection
  - Line biasing
  - Transmitter
  - Receiver
  - Watchdog function
  - Power on reset
- Hardware Support for Bus Collision Detection
- Data Rates from 10k to 160kbits/second
- Multi-Master / Multi-Slave Configurations, as well as Master-Slave
- Integrated Protection against Automotive Interference Pulses, including Load-dump
- High-voltage BICMOS Technology

General Description

The chip is designed to be used in a car multiplexing system in bus collision mode, using the VAN protocol according to ISO standard 11519-3, at a maximum transmission speed of 160kHz. The circuit consists of the following blocks:

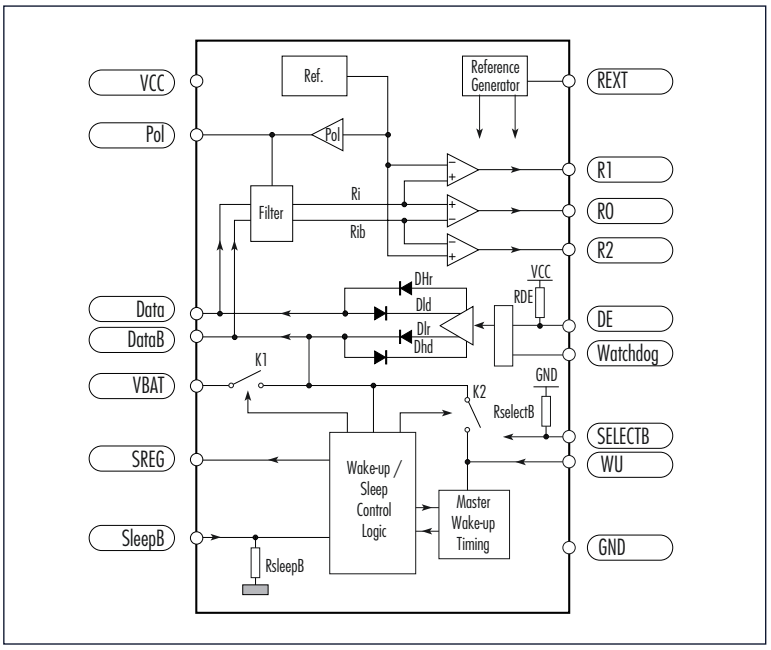
- differential line transmitter
- differential line receiver with built-in filtering and digital interface
- sleep and wake up system
- watchdog and power on reset

Normal Operation Mode

The network consists of several nodes connected to a two-wire bus. The chip acts as the interface between the bus wires and the digital parts controlling communication. The bus sees all nodes as physically identical. The difference between nodes is in the controlling part which defines whether a node is a master or a slave.
For this interface chip the difference

between master and slave only becomes important during sleep and wake up mode. This will be described further on. The interface chip is directly connected to the bus wires on the two pins called Data and DataB.

These two pins are the outputs of the line transmitter, and are also the inputs of the line receiver. Eventually an impedance balance can be added externally at these two pins.



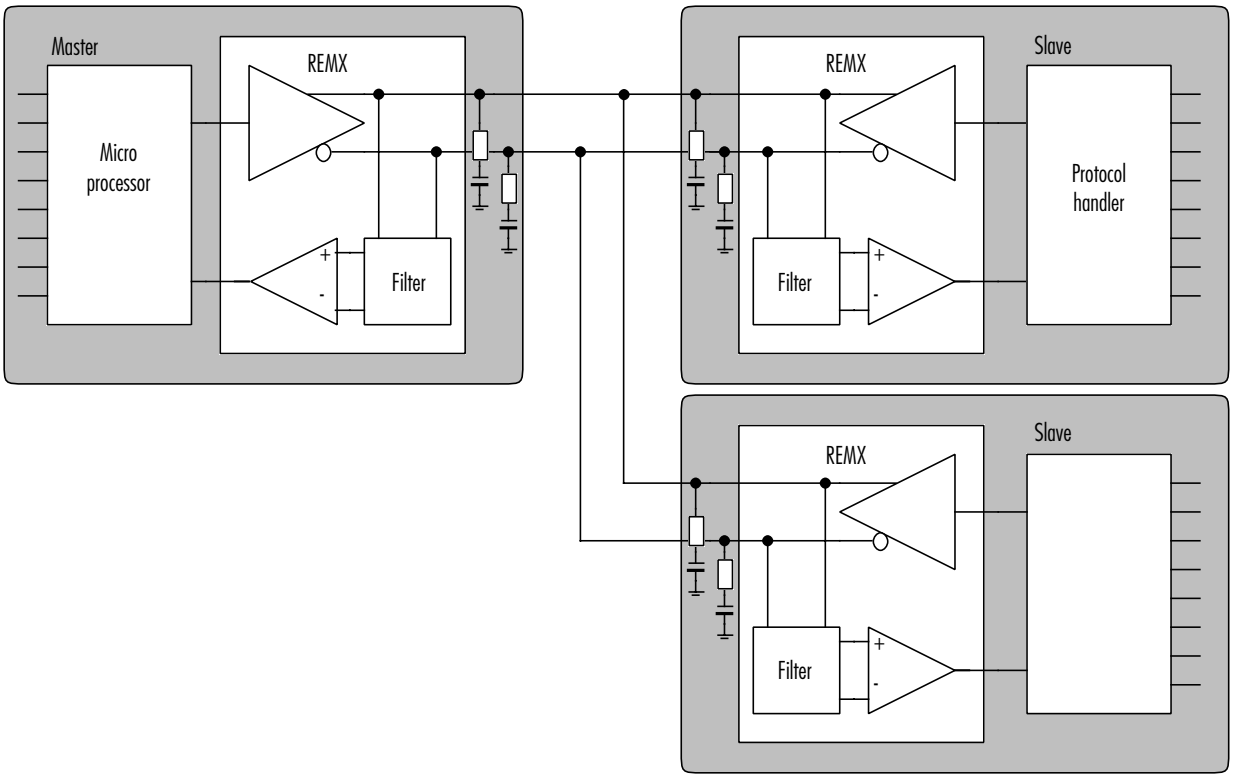


Fig.1: **Basic Configurations of the Network**

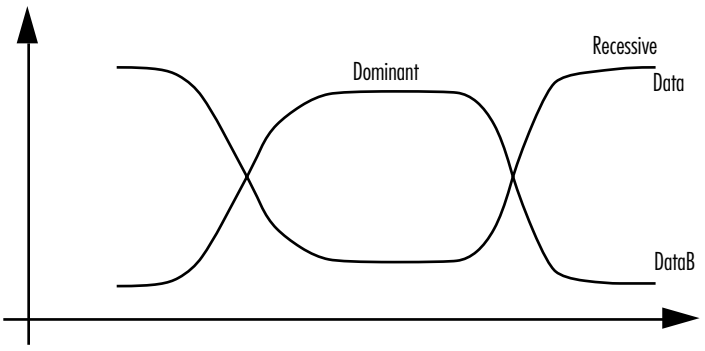


Fig.2: **Typical Bus Signals**

2.0 Transmitter Functional Description

A low level on TX0 and a low level on RX0 correspond to a dominant state on the bus lines. To provide an independent switch-off of the transceiver by a third device (e.g. the µC) an enable input is included.

In the disabled state the driving section behaves as in the recessive state and does not depend on the input voltage at TX0. The output of the receiving section is forced to the recessive state and does not depend on the bus voltage. RX0 still outputs the data corresponding to the input signal at TX0A or TX0B. This is realized by an internal logical connection.

In the enabled state the driving section behavior depends on the input voltage at TX0. The output of the receiving section depends on the bus voltage. RX0 only represents the data of the receiver output. The internal logical connection between TX0 and RX0 is interrupted.

The enable input has an internal pull up resistor to ensure a disabled state when the input is not connected.

Pin VS is an additional supply pin. This pin is used to supply the control stage of the bus driver with a voltage that is higher than the normal supply voltage. This is needed to guarantee proper functioning of the bus driver. The pin VS can be supplied with a DC voltage source, or with a voltage generated with a charge pump. For this purpose a square wave generator is integrated on chip. The output is a push pull cmos output stage at pin OSC. With the aid of two capacitors and two (external or internal) diodes a charge pump can be build to transform the supply voltage VCC to a higher level at VS.

SleepB	SELECTB	DE	DHr	DLd	DHd	DLr	R0	R1	R2
1	1	0	1.2mA	0mA	0mA	1.2mA	HI	HI	HI
1	1	1	1.2mA	0mA	0mA	1.2mA	HI	HI	HI
1	0	0	1.2mA	50mA	50mA	1.2mA	0	0	0
1	0	1	1.2mA	0mA	0mA	1.2mA	1	1	1
0	X	X	0mA	0mA	0mA	0mA	HI	HI	HI

HI = high impedant

Thermal-shut-down: When the Data pin is shorted to VBAT, the dominant-current can cause an extreme dissipation (worst-case: 64mA*1.2*16V = 1.2W).
To prevent that the internal junction temperature is exceeded an internal thermal-shut-down TSD is implemented. This condition is memorised as long as R1 stays high (short still exist). The memory is reset once R1 becomes 0. The TSD can also be activated by the testmode. In this way the functionality of the TSD can be tested in production. The implementation of the testmode is depicted in figure 6. Testmode will be activated when 2 rising edges on pin Watchdog occur while DE stays one (2 bit shift-register).

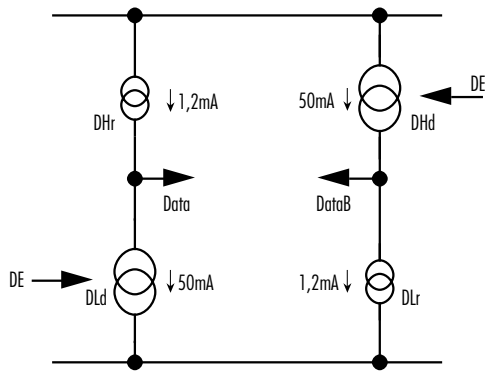


Fig.3: **Transmitter Current Sources**

Receiver

The line receiver is always active during normal operation, independent of the state of the transmitter. Basically the receiver part consists of an on-chip passive (first order) low pass filter, followed by three comparators in parallel. The outputs of these comparators pass to a small block of logic and are then transferred to the controller chip. The implemented filter is fully symmetrical, thus generating the internal signals Ri and Rib from the signals Data and DataB. Ri and RiB are fed to the inputs of the comparators. From these three comparators, one has its two inputs connected to Ri and RiB.

The two other comparators have only one input connected to either Ri or RiB, while the other input is connected to an on chip reference voltage, indicated as Vpol. The value of this voltage is about half the output voltage of the transmitter.
This ensures that, when the transmission is disturbed on one of the wires, the communication can still go on via the transmission on the other wire and one of the two supplementary comparators.

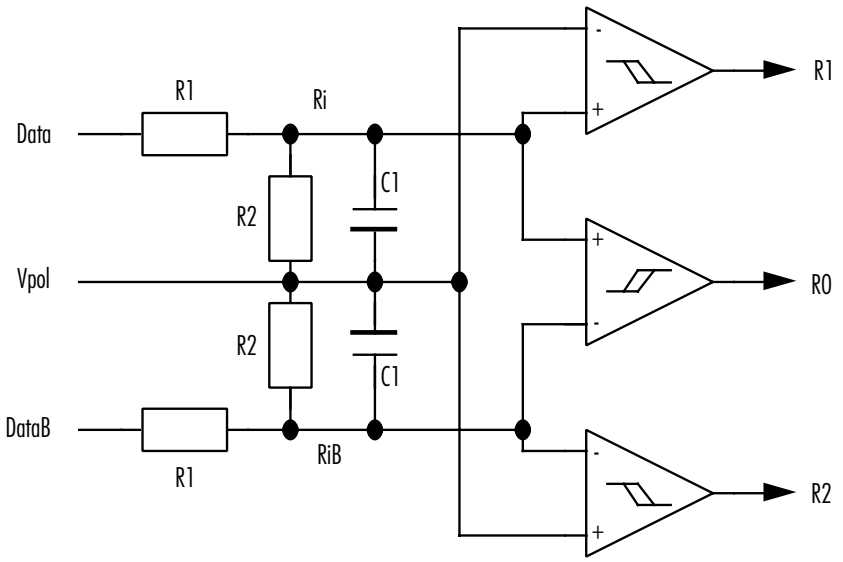


Fig.4: **Receiver Section**

4.0 Watchdog Functional Description

If the pin DE of one transmitter remains for some reason in the dominant state the communication is lost on the hole network. And further the localisation of the faulty module by the diagnostic system is impossible. To prevent this a system WA is interfaced between the DE command and the transmitter that forces a recessive state after some delay defined by an external capacitor C (Fig.5)

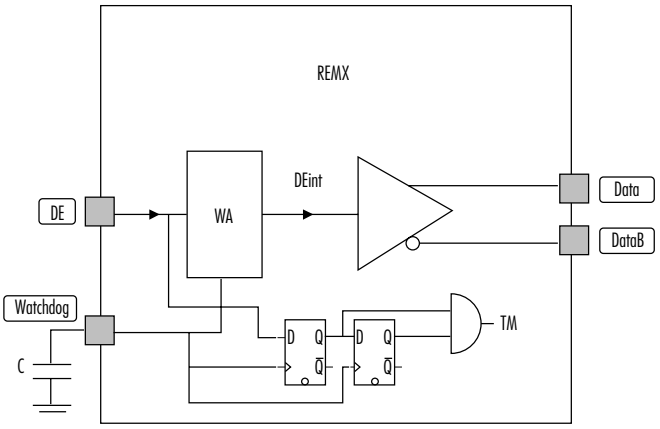


Fig.5

Receiver

The function of the watchdog interface is displayed in the diagram below. The time-delay tdom is generated by charging the external capacitor starting when DE has become low (recessive to dominant transition). The capacitor is discharged after DE has become high again (dominant to recessive transition). This has to occur in less than one time-slot to enable the watchdog for a next falling edge on DE (treset).

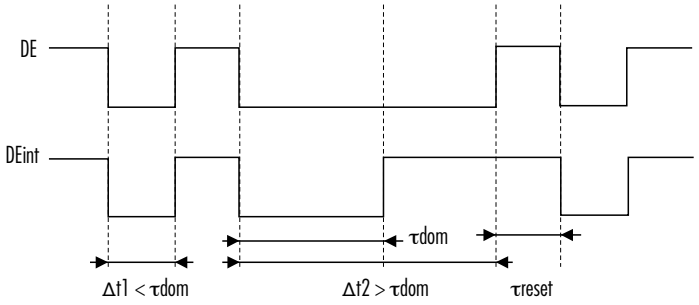


Fig.6

5.0 Power-on-reset Function

The POR-circuit monitors the voltage-levels for the supplies VCC and Vbat.
When Vcc becomes lower than PORLVcc then the device is put in power-down (POR-condition). It will stay in power-down until Vcc becomes higher than PORHVcc.
When Vbat becomes lower than PORVbat and Vcc stays high than the device is in sleep-mode. It will stay in sleep-mode until Vbat becomes higher than PORVbat.

The POR-condition is defined as follows:

- all internal circuits are switched in power-down(PD) to reduce the supply-currents
- the outputs R0,R1, R2 are put high-impedant
- the transmitter-outputs are put high-impedant
- the internal nodes Ri and RiB are shorted to Vcc (figure 14, paragraph "4.2.4. Filter Characteristics")
- the switches K1 and K2 are open (same as normal mode) (figure 8, paragraph "3.3 Sleep mode operation").

The implementation of this POR-function is important for the case of an open ground. In this case the voltage at the ground will increase referred to the external ground. The voltage between the gnd-pin and the Vcc pin will become lower than PORLVcc so that the outputs Data and DataB become high impedant. To avoid that the resistors of the filter will keep the GND-pin low the nodes Ri and RiB are connected to Vcc during POR.

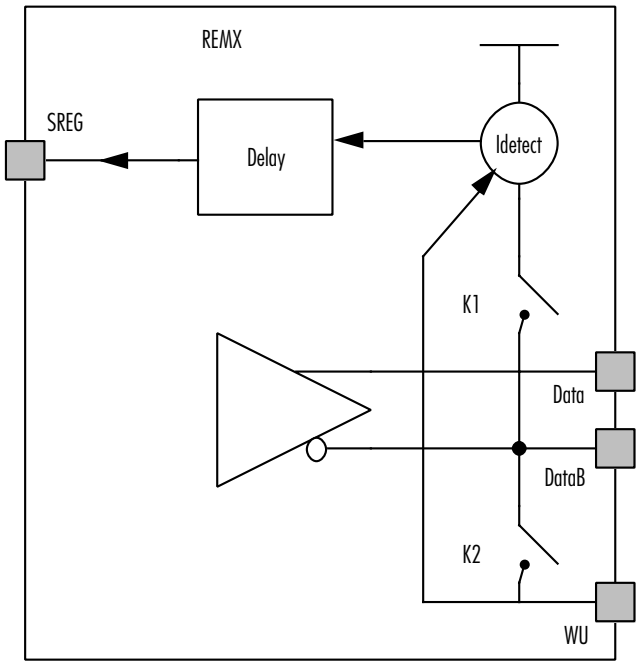


Fig.7: **Sleep Circuit during Normal Mode and POR**

6.0 Sleep Mode Operation

An important function of the multiplexing system is its ability to go into a sleep mode. At this moment the power consumption is reduced to the minimum. The system can wake up again in two different ways.
Although all interface chips are physically identical, the functionality of the chip is different for a master and a slave node. Figure 7 shows the most important circuits with regard to the sleep mode. On node DataB there are two switches, one to Vbat via a current sensor and one to the pin WU. Furthermore, the input SleepB is used to put the circuit in sleep mode, at which time the external regulator (SREG = tristate and pulled up by an external resistor) will be shut down. Following is a detailed description of the behavior of a master and a slave node. Figure 7 illustrates the state of all switches during normal operation; this is identical for a master and a slave node. Figure 8 shows a system during sleep mode. Figure 9 and 10 illustrate the possible sequences to go from sleep mode to normal mode and back. If the sleep/Wake-up function is not used (SleepB connected to Vbat), then it must be possible to connect Vbat to Vcc without disturbing the function of the transmitter and the receiver.

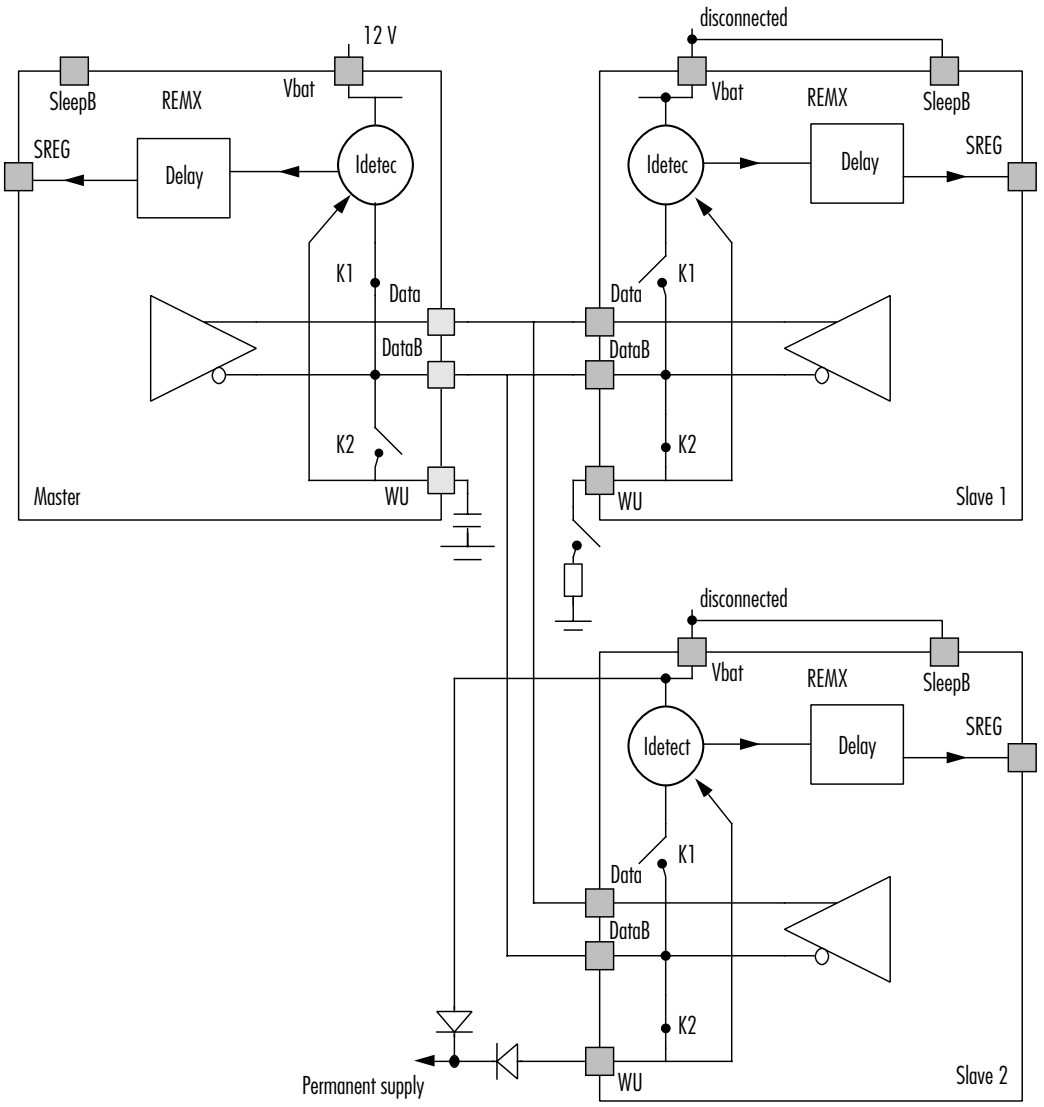


Fig.8: **System Configuration in Sleep Mode**

7.0 Entering Sleep Mode

Master node:
The interface chip in a master node is permanently connected to the supply Vbat. The system is put in sleep mode by pulling the pin SleepB of the master node to ground.

This disables the SREG-output which no longer pulls the DISABLE-input of the external regulator down. This condition will disable the external voltage regulator. The switch K1 which connects Vbat with the DataB wire in a master is closed. The transmitter is disabled and rendered highly impedant.

Slave node:
When the external regulator of the master is disabled, the Vbat of all slaves is disconnected from the supply by an external circuit (e.g. by a relay which is controlled by the regulator). From this moment on the slaves are only supplied via the pin DataB. This is the difference between a master and a slave.

Because the Vbat of the slaves is disconnected, the switch K2 closes, connecting DataB with the pin WU. The system is now in sleep mode.

Wake Up Through Current Detection

When, at a particular slave node, the pin WU is connected to ground (eventually via a resistor) a current will flow from Vbat at the master node, through the DataB wire, to ground. When this current is above a well defined value Idet, this will be detected in the master node. When this current is flowing for a period tds the pin SREG is pulled down and the external regulator is activated. The period tds is defined by the interface chip and an external capacitor connected to pin WU at the master node. When the regulator is active again, the microcontroller in the master node will pull high the pin SleepB. This will open the switch K1. The master is now in normal operation again. Since the regulator in the master-module is activated again, the pin Vbat in the slaves is reconnected to the supply. In all slaves the pin SleepB is connected to Vbat. Therefor, from the moment the Vbat is connected, the slave is in normal operation again. Switch K2 is therefor opened. Following is a table explaining the different states for both a master and a slave.

Master Node	Normal Mode	Sleep Mode
K1	open	closed
K2	open	open
WU	loaded with capacitor and discharged to ground	loaded with capacitor and discharged until I(DATAB)<Idet
SleepB	1	0
1Vbat	connected	connected
Slave Node	***Normal Mode***	***Sleep Mode***
K1	open	open
K2	open	closed
WU	contact to ground	contact to ground
SleepB	1	0
1Vbat	connected	disconnected

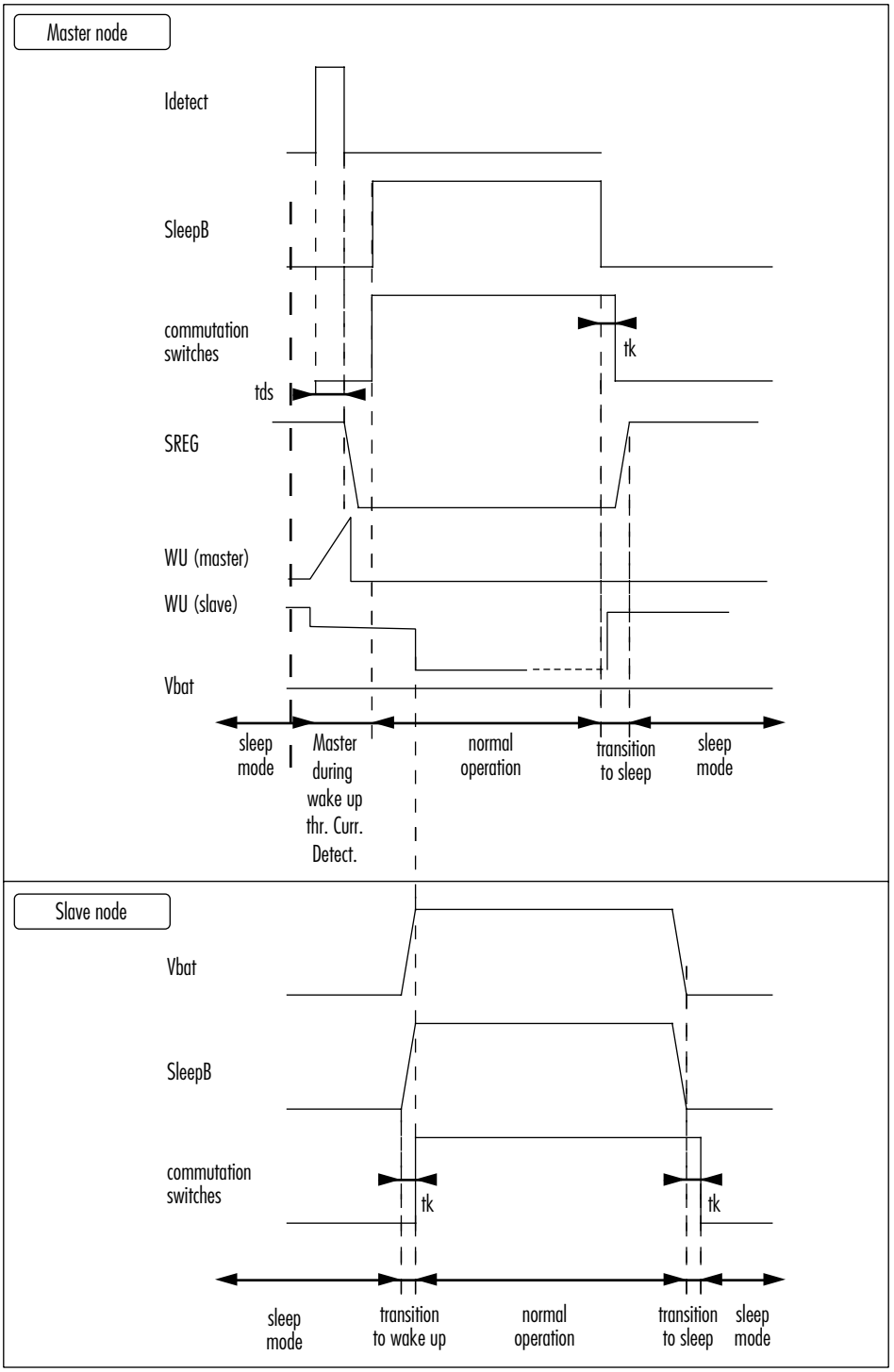


Fig.9: **Wake-up through Current Detection**

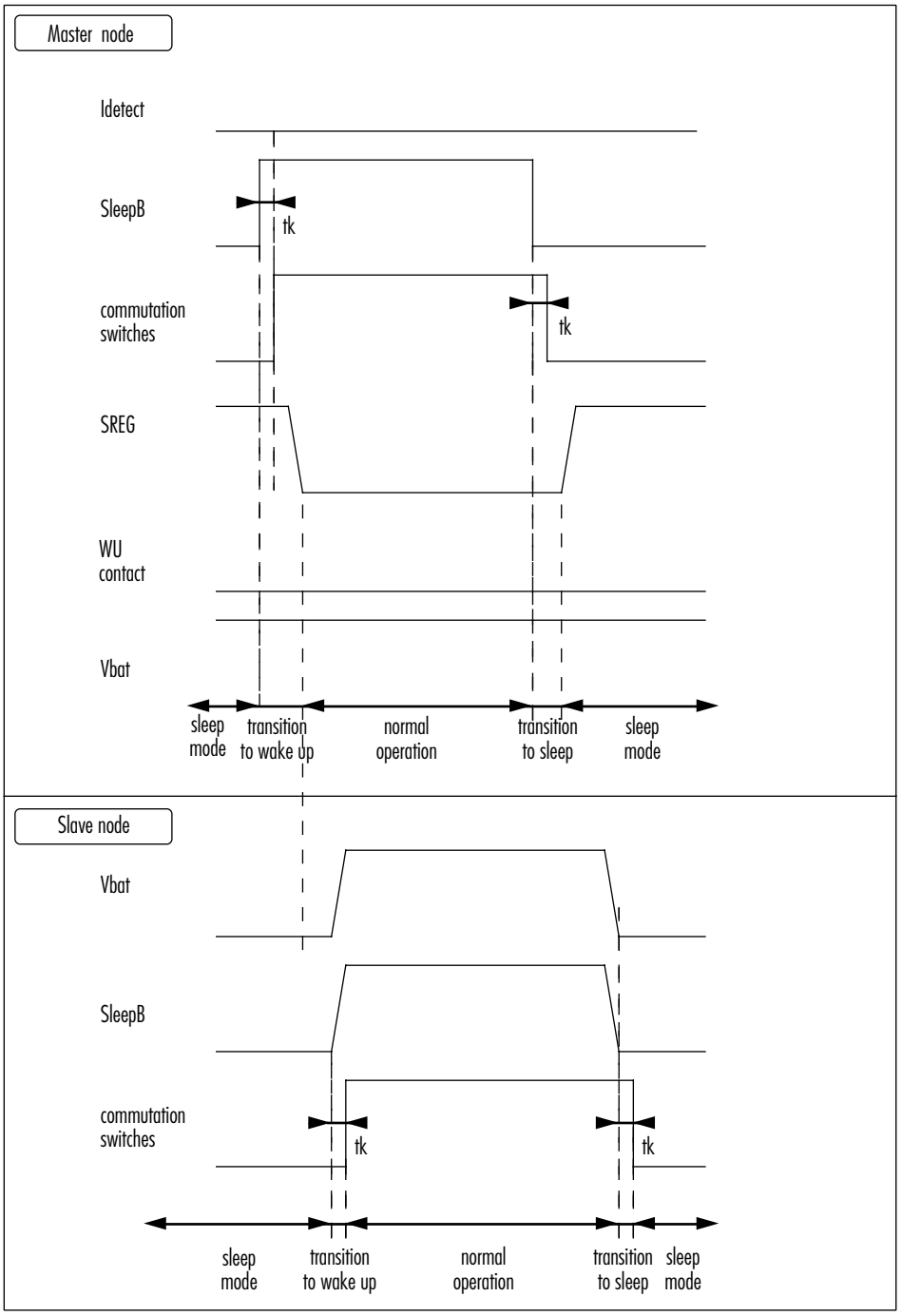


Fig.10: **Wake-up through SleepB Activation**

Permanent Supply at a Slave Node

Circuits located at a slave node and which need a permanent supply, even during sleep mode, can be connected as shown in figure 8. During normal mode the circuit is supplied through Vbat. During sleep-mode the circuit is supplied through DataB of the master. In this latest case, the current consumption of this circuit has to be low enough to avoid that the master will detect this as a current to restart the system.

Overvoltages on Pins Data, DataB and Vbat

The pins Data, DataB must be capable of being connected to:

- 18V during 2 hours
- 24V during 1 minute
- -12V during 5 seconds

without destroying the component, and this over the complete temperature range as long as the maximum junction temperature of REMX is not exceeded, with the circuit supplied or not, and whatever the status of the current generators.
(To calculate the junction temperature Tj of REMX: Tj = Dissipation(W) * Thermal-resistance of the package (Rth = 78dgc/W))
Parametrical characteristics will not be guaranteed under these conditions.

The pin Vbat must be capable of being connected to:
- 18V during 2 hours
- 24V during 1 minute
- -0.7V during 5 seconds

without destroying the component, and this over the complete temperature range as long as the maximum junction temperature of REMX is not exceeded, with the circuit supplied or not, and whatever the status of the current generators.
Parametrical characteristics will not be guaranteed under these conditions.

The outputs of the line transmitter have to be independent. When one is short circuited to ground, to the supply voltage, or is open, this should not influence the performance of the other output.

The pins Data and DataB must withstand the pulses 1 to 5 in according to ISO 7637 part 1.

The exact values are listed in the table below.

Parameter	Pulse 1	Pulse 2	Pulse 3a	Pulse 3b	Pulse 5 (fig 11)
Class	C	C	C	C	C
Vamp(V) (*)	-85	+73.5	-150	+100	50
Ri(Ω)	10	10	50	50	2
T	2 ms	50 µs	0.1 µs	0.1 µs	400 ms
Tr	≤ 1 µs	≤ 1 µs	≤ 5 ns	≤ 5 ns	5 to 10 ms
number	1	1	1	1	1

(*): Voltage Vamp of all pulses is referred to 0V.

The pin VBAT must withstand the pulses 1 to 5 in according to ISO 7637 part 1 with the external components depicted in figure 26: REMX Applications Diagram on page 29.

Parameter	Pulse 1	Pulse 2	Pulse 3a	Pulse 3b	Pulse 5 (fig 11)
Class	C	C	C	C	C
Vs(V) (*)	-100	+100	-150	+100	36.5
Ri(Ω)	10	10	50	50	2
T	2 ms	50 µs	0.1 µs	0.1 µs	400 ms
Tr	≤ 1 µs	≤ 1 µs	≤ 5 ns	≤ 5 ns	5 to 10 ms
number	34000	17000	36000	36000	5

(*): Voltage Vs is referred to 0V for pulse 1. Voltage Vs is referred to 13.5V for pulses 2, 3a, 3b and 5.

Pulse 5: Pulse defined for an alternator with internal protection.

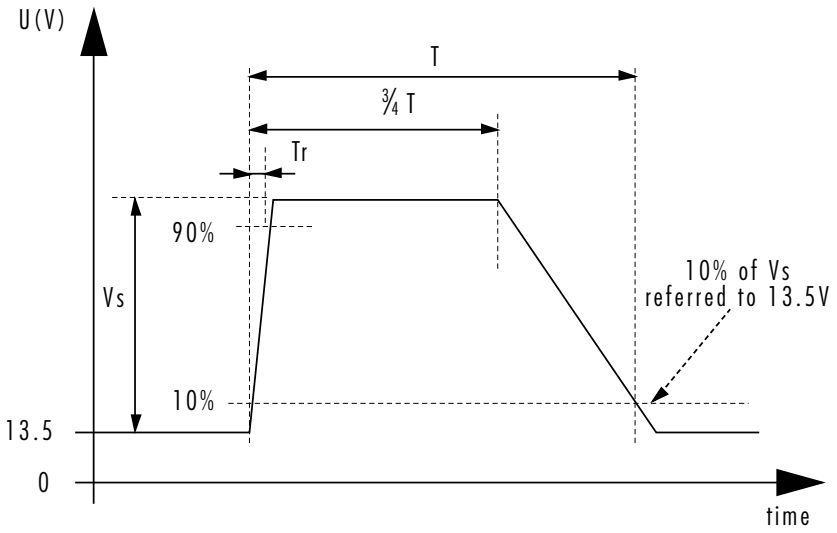


Fig.10: **Pulse 5**

9.0 Pinout and Packaging

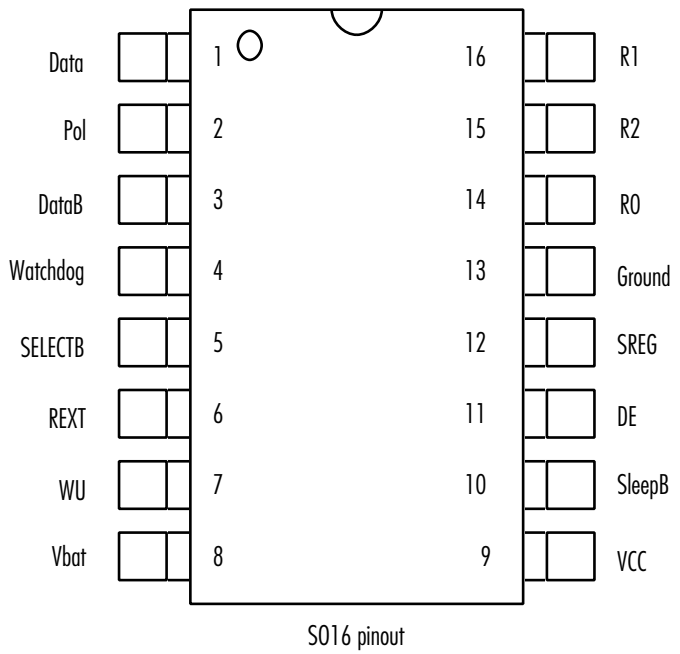


Fig.12: **Pin Configuration**

Nr.	Name	Type	Description
1	Data	interface	positive interface pin
2	Pol	analog out	reference voltage for input filter
3	DataB	interface	negative interface pin
4	Watchdog	analog I/O	current output for watchdog function
5	SELECTB	digital in	Enable input for transmitter and data outputs R0, R1, R2
6	REXT	analog in	current reference input
7	WU	analog I/O	wake up pin
8	Vbat	supply	battery supply voltage
9	Vcc	supply	5V supply
10	SleepB	digital in	sleep input
11	DE	digital in	transmit data in
12	SREG	digital out	output to disable the external voltage regulator
13	GND	supply	ground pin
14	R0	digital out	receive data out
15	R2	digital out	receive error2 out
16	R1	digital out	receive error1 out

10.0 Packaging

Package Name	Package Code	AMI Semiconductor Drawing n°	JEDEC Outline DWG
16 pins PSOP 300 mils	SO16 B	87-0034	MS-013

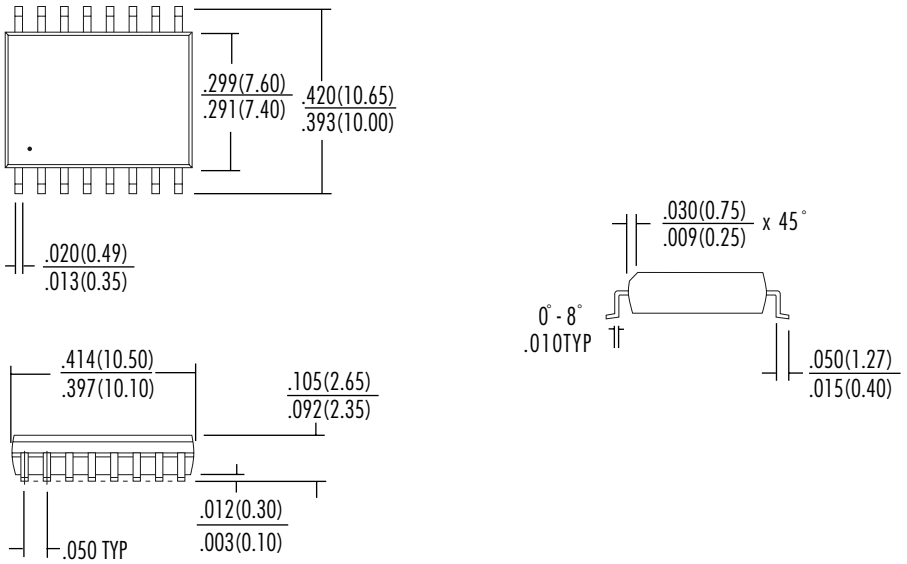


Fig.13: **Package**

Marking

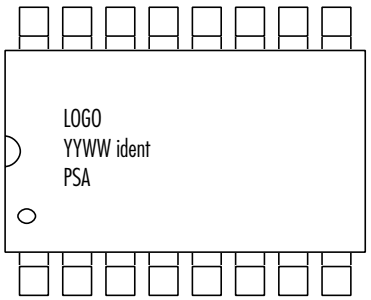


Fig.14: **Topside Marking**

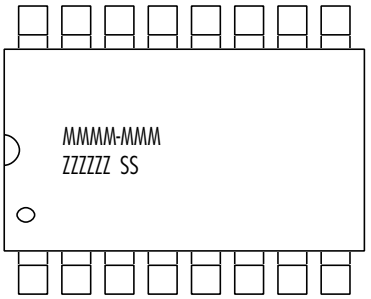


Fig.15: **Backside Marking**

LOGO: Micro-signature Alcatel.
YYWW: assembly year and week.
ident: REMX
SS: Assembly source code.
MMMM-MMM: AMI Semiconductor product name.
ZZZZZZZ: wafer lot identification.

11.0 Delivery

Delivered in tubes

44 devices per tube

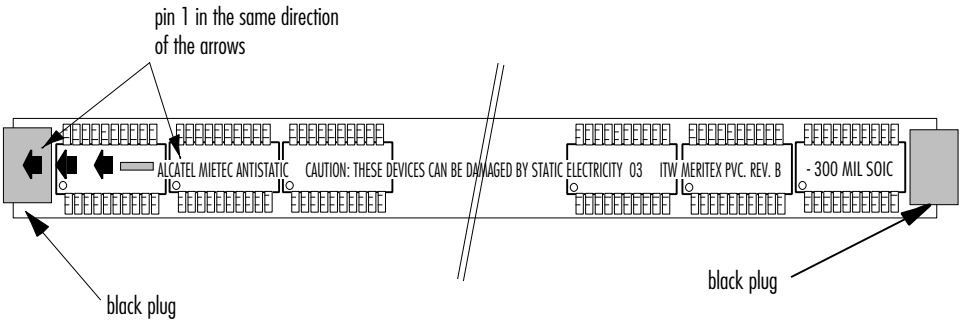


Fig.16: **SOIC Tube**

Delivered Tape on Reel

The plastic small outline (SO), can be placed in tape on reel, eventually in combination with dry pack.

All used materials and procedures are in line with the related EIA, IEC documents.

IEC 286-3 - packing of components for automatic handling

EIA-481-2 - 16 and 24 mm embossed carrier taping of surface mount components for automatic handling

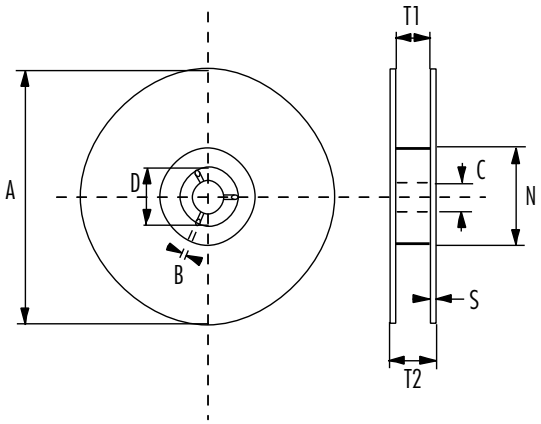


Fig.17

Reels (Fig.17) Tape width	A	N	T1	T2	D	B	C	S
+0.5	+0.5	+0.4	+0.4	+0.2	+0.0	+0.2	typ	
-0.5	-0.5	- 1.6	-0.6	-0.2	-0.5	-0.2		
16	330	62	18	22	30.0	2	13	2.0

(All figures in mm)

12.0 Wake Up Through SleepB Activation

Carrier Tapes

Carrier tapes with width of 12, 16, 24, 32 or 44mm are used.

Material: Conductive polystyrene - black
Thickness: 200 - 400um
Tensile strenght: 19 - 25 Mpa
Elongation at break: 40 - 45%
Surface resistance: 10E4 - 10E6 Ω/SQ
Vicat softening point: 90 - 98°C

Dimensions for 12, 16 or 24mm tape
(All dimensions in mm) (Fig.18).

W: 12 +/- 0.3 or 16 +/- 0.3 or 24 +/- 0.3
D1min: 1.5
E1: 1.75 +/-0.10
P0: 4.0 +/-0.10
S1min: 0.6

Cover Tape
Cover tapes with width of 9.3, 13.5, 21.5, 25.5, 37.5mm are used in relation to the tape width.
Material:
static dissipative polyester
temperature sensitive tape
First layer: Transparent polyester
Second layer: Polyethylene
Total thickness: 0.060 mm
Tensile strength: 110 N/cm
Surface resistivity: 1.2x10E12 Ω/SQ
Elongation at break: 91%

The clearance between the ends of the terminals or body of the component to the sides and depth of the cavity (A0, B0, C0) must be within 0.05mm min and 0.50mm max for 12mm tape, or within 0.15mm min and 0.9mm max for 16mm tape, or within 0.15mm min and 1.0mm max for 24, 32 or 44mm tape.

The cavities of the 44, 68 and 84 pins PLCC (PC) and PQFP (PQ) devices will have a platform supporting the body of the package making sure the lead tip is not touching the cavity.

General

All components are located in the cavity with pin 1 adjacent to the round sprocket holes.
The components are packed with the terminations facing the bottom of the embossed carrier.
There is a leader (start) of 230mm minimum which may consist of carrier and/or cover tape followed by a minimum of 160mm of empty carrier tape sealed with cover tape.
There is a tailer (End) of 160mm minimum of empty carrier tape sealed with cover tape. The entire carrier tape must release from the reel hub as the last portion of the tape unwinds from the reel without damage to the carrier tape and the remaining components in the cavities.

More details can be found in the AMI Semiconductor document spec 16665 and spec 9210.

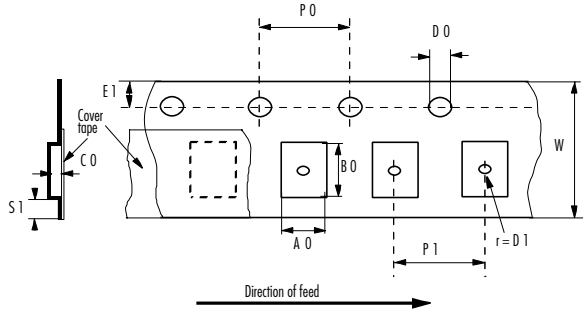


Fig.18

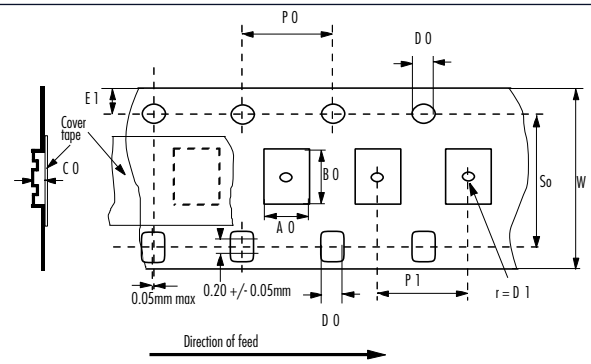


Fig.19

Tooling list for carrier tape:

Package Type	Tape width (W)	Pitch mm (P1)	A0 mm	B0 mm	C0 mm	Standard Qty/reel	Meters /reel	Cavity /reel
SO16 B	16 mm	12	10.7	10.7	3.1	1000	13.0	1083

13.0 Wake Up Through SleepB Activation

Soldering Information

All components meet the minimum requirments of the two requirements outlined below.

- Solder wettability: test Mil STD 883 D method 2003 (95 % solder wetting of the leads)
- Wetting balance solderability test: Mil SRTD 883 D method 2022 (5 sec 245°C)

Through Hole Devices

These devices can be soldered with most industry standard soldering processes.
The devices withstand the resitance to soldering test IEC 68 - 2 - 20 (2 cycles).

Surface Mount Devices

Take into account the dry pack recommendatinos as stated on the label applied.

All SMD components can be soldered with the standard infra red, vapour phase and double wave soldering processes. Recommended profiles can be found in fig. 20, 21 and 22.

IR surface mountable components meet the following test sequence storage 85°C, 85 % RH, 168 hrs followed by 2 cycles of infra red solder heat application (CECC00802) and 100 thermal cycles -55°C /+125°C (Mil STD 883 D method 1010).

Double wave mountable components meet the following test sequence storage 85°C, 85 % RH, 168 hrs followed by 1 cycles of double wave solder heat application (CECC00802) and 100 thermal cycles -55°C /+125°C (Mil STD 883 D method 1010).

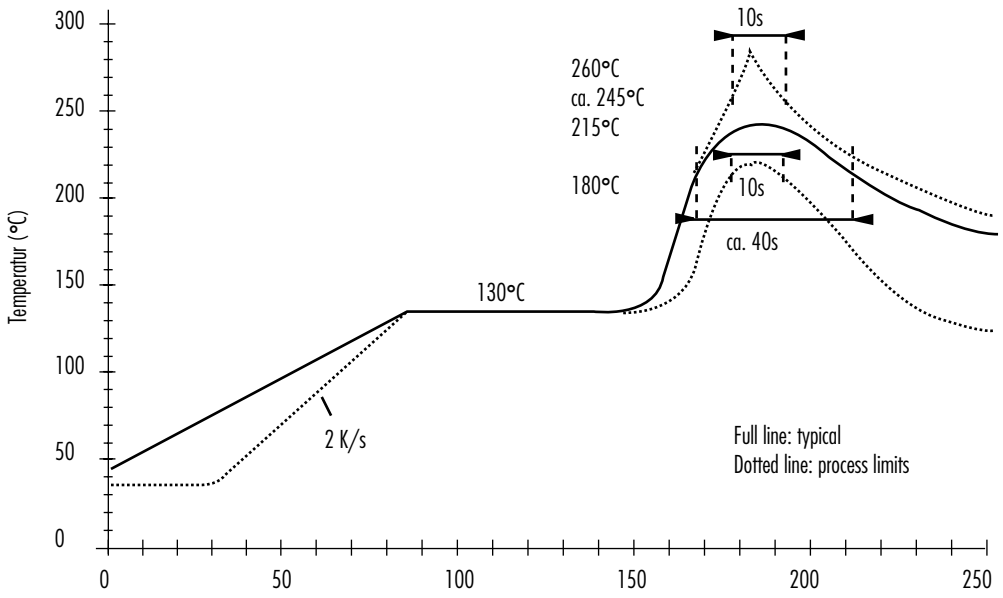
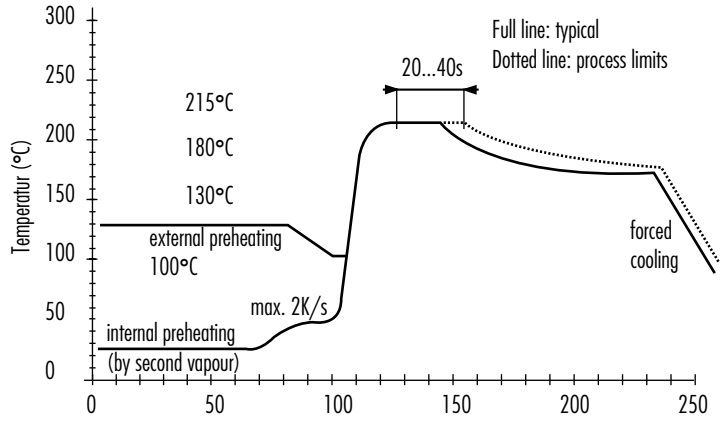


Fig.20: **Infra Red Soldering**



Vapour Phase; Batch System with Preheating

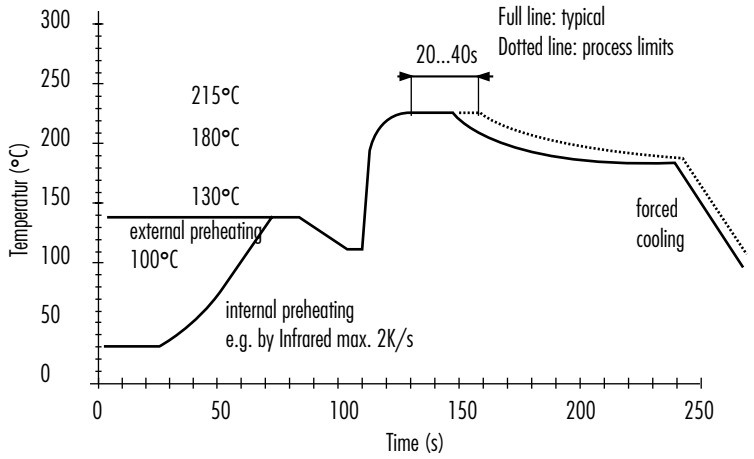


Fig.21: **Vapour Phase; In Line System with Preheating**

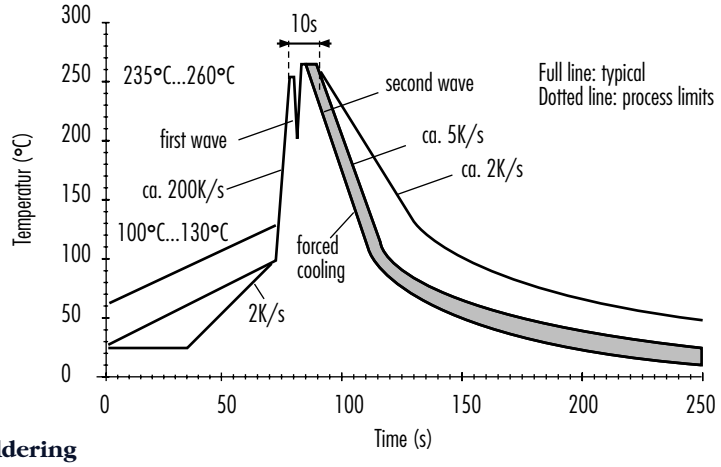


Fig.22: **Double Wave Soldering**

14.0 Electrical Characteristics

Absolute Maximum Ratings

Sym	Description	Min	Max	Unit
Vbatmr	power supply voltage	GND - 0.3	50(Note 1)	V
Vccmr	power supply voltage	GND - 0.3	7	V
VDatamr, VDataBmr	Voltage at Data DataB	-85(Note 1)	+50(Note 1)	V
SleepBmr	Voltage at input SleepB	-0.3	Vbat + 0.3	V
WUmr	Voltage at input WU	-2.0	20.0	V
Vinputsmr	Voltage at inputs DE, SELECTB, Watchdog	-0.3	Vcc + 0.3	V
Tmr	ambient temperature under bias	-45	130	°C

Note 1: The maximum time for Vbat at 50V is related to pulse 5, the maximum time for Data and DataB at 50V and -85V is related to pulse 5 and 1. The related pulses are discribed on pages 11 and 12.

Operating Ranges

Sym	Description	Min	Max	Unit
Vbat_m	power supply voltage for master (note 1)	6.1	16	V
Vbat_sl	power supply voltage for slave during normal-mode		4.75	16 V
Vcc	power supply voltage	4.75	5.25	V
Tamb	ambient temperature	-40	125	°C
Vdata, VdataB	Voltage at Data, DataB	-5	10	V
SleepB	Voltage at input SleepB	0	Vbat	V
WU	Voltage at input WU	0	Vbat	V
Vinputs	Voltage at inputs DE, SELECTB, Watchdog	0	Vcc	V
Cla	load capacitance on ASIC outputs		70	pF

Note 1: All parameters are guaranteed for the voltage range Vbat_sl except parameters Vrev1, Vrev2, Vrev, Idetect, ICR1, ICR2 and tds (all parameters of the sleep/wake-up circuit) which are only guaranteed for the voltage-range Vbat_m.

15.0 Detailed Electrical Characteristics

All characteristics are valid under the full operating range of temperature and supply voltage, mentioned above, unless otherwise noted.

Watchdog Function

The chip is put in Normal mode (V(SleepB) = Vbat).

The internal current-source (IWD) charges the external capacitor when input DE is low. This current is referred to the reference current Iref at input REXT which is determined by an external resistor Rref. This current is depending of an internal reference voltage (VBG). Also the threshold level is depending of the same reference so that the watchdog delay time is independent of the absolute value of this reference.

The capacitor is discharged through an internal switch when input DE is high.

The pin REXT has to be connected to ground via an external resistor of
10 KΩ (tol. < 1%).

The external capacitor at the watchdog pin is 6.8nF for 62.5Kbits/s and 3.3nF for 125Kbits/s. Typical values for the parameters below are Iref = 200uA, Iwd = 16mA, Vwd = 2.42V. These parameters result in the following typical delay times:

- Cwd = 6.8nF => Twatchdog = 1030ms Treset < 4ms (Twatchdog = Cwd*Vwd/Iwd)
- Cwd = 3.3nF => Twatchdog = 500ms Treset < 2ms (Treset < Cwd * Zwd*5).

Specification:

Sym	Description	Min	Max	Unit
Vrext	Voltage at pin Rext	1.9	2.1	V
Iwd	pull-up current at pin watchdog DE = 0	-15%	+15%	Vrext/10KΩ/12.5
Vwd	threshold level for watchdog input DE = 0	-10%	+10%	Vrext *3/2.5
Zwd	output impedance at watchdog input DE = 1		100	Ω

Note 1:
output impedance measured for V(watchdog) = 0.5V. Zwd = V(watchdog)/I(watchdog)

16.0 Power-on-reset Function

The POR-circuit monitors the voltage-levels for the supplies VCC and Vbat.

When Vcc becomes lower than PORLVcc then the device is put in power-down (POR-condition). It will stay in power-down until Vcc becomes higher than PORHVcc.

When Vbat becomes lower than PORVbat and Vcc stays high than the device is in sleep-mode. It will stay in sleep-mode until Vbat becomes higher than PORVbat.

The POR-condition is defined as follows:

- all internal circuits are switched in power-down(PD) to reduce the supply-currents.
- the outputs R0,R1, R2 are put high-impedant
- the transmitter-outputs are put high-impedant
- the internal nodes Ri and RiB are shorted to Vcc
- the switches K1 and K2 are open (same as normal mode)

Specification:

Sym	Description	Min	Max	Unit
PORLVcc	Low level of the POR-circuit for Vcc	2.2	3	V
PORHVcc	High level of the POR-circuit for Vcc	2.8	3.6	V
PORDVcc	Difference between high and low level PORDVcc = PORHVcc - PORLVcc	0.35	0.75	V
PORVbat	Low- and High level of the POR-circuit for Vbat	2.5	3.5	V

Sleep/Wake-up System

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Vrev1	Voltage drop from Vbat to DataB (master node)	0		1	V	Irev1 = 5mA
Vrev2	Voltage drop from DataB to WU (slave node)	0		2.1	V	VDataB = V(Vbat) - Vrev1 Irev2 = 5 mA
Vrev	= Vrev1 + Vrev2	0		3	V	
Idetect	Wake up detection current at DATAB (master node)	10		15	mA	
ICR1	Short circuit current (master)	15		50	mA	
ICR2	Short circuit current (slave)	15		100	mA	
tds	Delay time for Idetect	1		10	ms	C at pin WU = 10 nF
Ifv	Current consumption of a slave node in sleep mode (current from DataB to Gnd)	-50		50	µA	

Transmitter

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Vod	differential output voltage	5.6			V	square wave at DE: - Freq = 20 KHz - duty cycle = 50% note 1
Vmce	common mode voltage (DC condition)			6.6	V	Vbat = 12V
Dvmcei	variation of the common mode voltage within 2us after DE transition	-3		3	V	Fig.25 square wave at DE: - Freq = 20KHz - duty cycle = 50%
Dvmcef	variation of the common mode voltage 2us after DE transition	-1		1	V	Fig.25 square wave at DE: - Freq = 20KHz - duty cycle = 50%
IldD	current limitation in dominant mode at pin Data	40	50	64	mA	VData = Vcc -2.2V
IldDB	current limitation in dominant mode at pin DataB (absolute val.)	40	50	64	mA	VDataB = GND +2.2V
Ilr	current limitation in recessive mode (absolute value for Data)	1	1.2	1.45	mA	VDATA = GND +2.2V VDATAB = Vcc -2.2V
Mim	matching of dominant currents	0		+30	%	note 2
Mir	matching of recessive currents	0		+30	%	note 3
IRG1	Recessive current template level 1	Ilr -20%		Ilr +20%	mA	Fig.24a Fig.24b
IRG2	Recessive current template level 2	-0.5		0.2	mA	Fig.24a Fig.24b
IDG1_D	Dominant current template level 1 for Data	ILdD -35%		ILdD +20%	mA	Fig.24b
IDG1_DB	Dominant current template level 1 for DataB	ILdDB -40%		ILdDB +20%	mA	Fig.24a
IDG2	Dominant current template level 2	-8		2	mA	Fig.24a Fig.24b
Ilm	leakage current for master node at (Data + DataB)			60	µA	note 4
Ils	leakage current for slave node at (Data + DataB)			40	µA	note 4
IFD12	leakage current at pin Data	-50		50	µA	0V < VData < 15V 0 < Vbat < 0.5V
IFD3	leakage current at pin Data	-750		50	µA	-15V < VData < 0 Vbat = Vcc = 0
IFDB12	leakage current at pin DataB	-50		50	µA	0V < VDataB < 15V 0 < Vbat < 0.5V Vcc = 0V or 5V
IFDB3	leakage current at pin DataB	-750		50	µA	-15V < VDataB < 0 Vbat = V56 = 0
Dtpdr1	Absolute value of difference between propagation delay times tpdrlh1(data) and tpdrhl9(datab) for D>R transition	0		250	ns	Fig.23
Dtpdr9	Absolute value of difference between propagation delay times tpdrlh9(data) and tpdrhl1(datab) for D>R transition	0		700	ns	Fig.23
Dtprd1	Absolute value of difference between propagation delay times tprdlh1(datab) and tprdhl9(data) for R>D transition	0		200	ns	Fig.23
Dtprd9	Absolute value of difference between propagation delay times tprdlh9(datab) and tprdhl1(data) for R>D transition	0		500	ns	Fig.23
tpdrlh1 tpdrhl9	Propagation delay D->R	30		500	ns	note 5, Fig.23

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
tpdrlh5 tpdrhl5	Propagation delay D->R	200		1000	ns	note 5, Fig.23
tpdrlh9 tpdrhl1	Propagation delay D->R	500		1700	ns	note 5, Fig.23
tprdlh1 tprdhl9	Propagation delay R->D	100		600	ns	note 5, Fig.23
tprdlh5 tprdhl5	Propagation delay R->D	400		900	ns	note 5, Fig.23
tprdlh9 tprdhl1	Propagation delay R->D	600		1400	ns	note 5, Fig.23

Note 1:
Vod = Abs (VData - VDataB)DE = 0 +Abs (VData - VDataB)DE = 1
This is a peak to peak measurement.

Note 2:
Mim = |(2 * (IData - IDataB))| / (|IData |+ |IDataB|)

Note 3:
Mir = |(2 * (IDataB - IData))| / (|IData| +| IDataB|)

Note 4:
The pins Data and DataB are resistively connected to each other via the integrated receiver filter.
Defining a leakage current at these nodes therefore only makes sense when the voltages at these two nodes are forced at the same voltage, so that no current is flowing through the filter.
As a consequence of this the definition of leakage currents on pins Data and DataB only makes sense when the line transmitter is disabled, i.e. in sleep mode.
When the device is in sleep mode, the pin DataB is connected via a switch either to Vbat or to the pin WU.
Therefore the leakage currents are defined as follows:
- the pins Data and DataB are connected to each other and the sum of the leakage current is measured.
- for Ilm : Vbat = 12 V
  V (Data + DataB) = 12V
- for Ils : Vbat = 0 V
  V(Data + DataB) = Vwu = 12V

Note 5:
During these measurements the load at Data and DataB is :
R->D : 4.3nF to GND + 20mA to simulate the total recessive load at a node
D->R : 270 pF to GND

Note 6:
Dtprd production test limit =100ns
design limit = 50ns

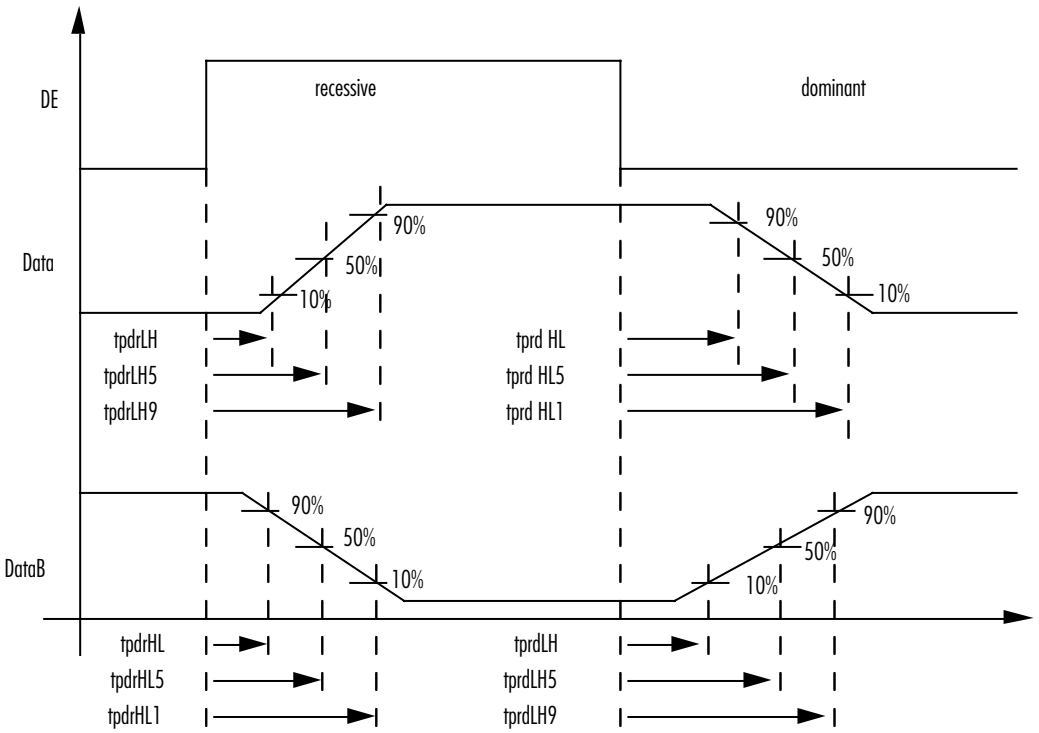


Fig.23: **Level Dependent Delays**

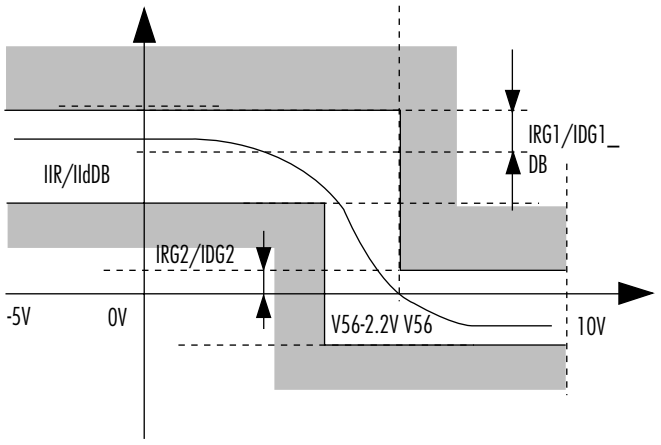


Fig.24a: **Current Gabaryt**

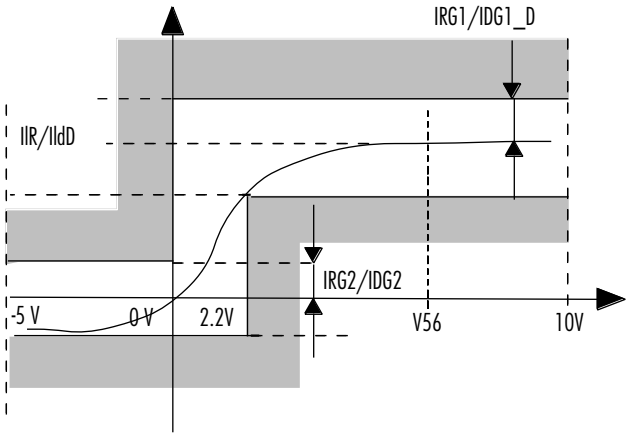


Fig.24b: **Current Gabaryt**

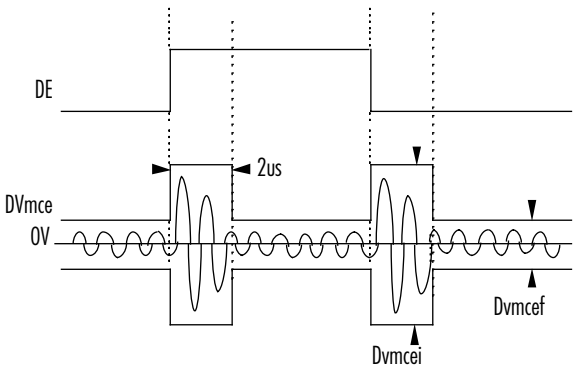


Fig.25: **Transmitter Propagation Delays**

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
Vmcr	Common mode voltage range	-2.8		5	V	
Fr1 §	Resistor value R1 in filter	21	42	72	KΩ	Fig.4 note 1
Fr2 §	Resistor value R2 in filter	14	28	48	KΩ	Fig.4 note 1
Fr12 §	Ratio Fr2/Fr1 = 42/28					Fig.4 note 1
Dfr21 §	Tolerance on FR12	-1		+1	%	Fig.4 note 1
Fc1 §	Capacitor value C1 in filter	8.5	10	11.5	pF	Fig.4 note 1
VCP	Positive comparator threshold level	200		420	mV	note 2
VCN	Negative comparator threshold level	- 420		- 200	mV	note 2
Voff	Input offset voltage (0V to Vcc common mode)	-50		+50	mV	note 2
VoffR0cmr	input offset voltage for the full common mode range	-65		+55	mV	note 1
Vhyst	input hysteresis	480		750	mV	note 2
TprLH, TprHL	Propagation delay time from input input (Data, DataB, Vpol) to output (R0 or R1 or R2)			600	ns	Vin peak-peak = 1V note 3
Dtpr	Difference between propagation delay times			100	ns	Vin peak-peak = 1V
Zgt1 §	Output impedance of pin Vpol			200	Ω	at 1MHz

Note 1:
Matching of resistors and capacitors of the filters on the two inputs is better than 1%. The different elements of the input filter cannot be measured externally. During production test the following parameters will be measured: the total resistance (Fr1+Fr2) between pin Vpol and Datax. These measurements, combined with the measurements on hysteresis, offset and propagation delays will guarantee the correct operation of the receiver section.

Note 2:
The values for positive and negative threshold level, offset and hysteresis of the line receiver are specified at the pins Data and DataB. This is a combination of the actual hysteresis and offset of the comparator, and the ratio of the resistors in the input filter.

Vhyst is defined as (VCP- VCN)
Voff is defined as (VCP+VCN)/2.

Note 3:
To measure the comparator with output R0, Data will be driven with a voltage Vpp1 = 1 V, DataB will be driven with Vpp2 = 1 V Vpp1 and Vpp2 are complementary.
To measure the two other comparators, Datax will be driven with a voltage Vpp = 2 V, and centered around the level Vpol.

Current consumption

Symbol	Condition	Value			
		Min	Typ	Max	
Ivbat_Sle	Current consumption at Vbat in Sleep mode (note 1a)			330	µA
Ivbat_POR	Current consumption at Vbat during POR (note 1b)			700	µA
Ivbat_Wu	Current consumption at Vbat in normal mode (note 2)			1	mA
Ivcc_Sle	Current consumption at Vcc in Sleep mode (note 1a)			50	µA
Ivcc_POR	Current consumption at Vcc during POR (note 1b)			200	µA
Ivcc_rec	Current consumption at Vcc in normal mode DE = 1 (note 2a)			20	mA
Ivcc_dom	Current consumption at Vcc in normal mode DE = 0 (note 2b)			35	mA

Note 1a:
The current consumption in sleep mode will be measured under the following conditions:
- Vbat = 16V
- Vcc = 5.25V and Vcc = 0V
- pin SleepB is left open
- DE = '1' (i.e. is left open).

Note 1b:
The current consumption during POR will be measured under the following conditions:
- Vbat = 16V
- Vcc = 2.5V after been lower than PORLVCC
- V(SleepB) = 16V
- DE = '1' (i.e. is left open)

Note 2a:
The current consumption in Normal mode will be measured under the following conditions:
- Vbat = 16V
- Vcc = 5.25V
- V(SleepB) = 16V
- DE = '1' (i.e. is left open)

Note 2b:
The current consumption in dominant mode will be measured under the following conditions:
- Vbat = 16V
- Vcc = 5.25V
- V(SleepB) = 16V
- DE = '0' (i.e. is connected to GND) + V(WATCHDOG) = 0V (to disable watchdog function)

Common for Note 1a, 1b, 2a, 2b:
- pin Vpol not loaded resistively
- pin WU is left open
- pin REXT loaded with 10KΩ to GND

Sym	Description	Min	Max	Unit
VSleepBt	hreshold level for input SleepB	2	3	V
RSleepB	Pull down resistor at input SleepB	10	45	KΩ
VHin	High level for digital inputs DE, SELECTB		0.7	Vcc
VLin	Low level for digital inputs DE, SELECTB	0.3	Vcc	
Vhyst §	Hysteresis for digital inputs DE, SELECTB	0.075		Vcc
IHinDE	Input current for digital input DE during sleep-mode (note 3)		50	µA
IHinSEB	Input current for digital input SELECTB during sleep-mode (note 3)		50 + V(selectb)/ Rinpd	µA
Rinpu	Pull-up resistor at digital input DE	5	20	KΩ
Rinpd	Pull-down resistor at digital input SELECTB	5	20	KΩ
VHout	High level of R0, R1, R2 for Isource = 2mA for Isource = 100µA (Note 2)	 0.8 0.9		 Vcc Vcc
VLout	Low level of R0, R1, R2 for Isink = 2mA for Isink = 100µA (Note 2)		 0.2 0.1	 Vcc Vcc
ILout	Leakage current at outputs R0, R1, R2 when outputs in tristate & outputs = 0V or outputs = Vcc	-50	50	µA
TdLH,TdHL §	rise and fall time at outputs R0, R1, R2 load: R = 1MegΩ, C = 20pF (Note 1)		50	ns

Note 1:
These 2 parameters are design-targets and will as such not be measured during production. Indirectly they are measured when measuring the parameters TprLH, TprHL, and DTpr for the receiver.

Note 2:
Only the most critical current (100uA or 2mA) will be tested during production. The other can be guaranteed when the most critical current reach the spec.

Note 3:
Input current for pins DE, SELECTB at 5V with Vbat = 0V and Vcc not connected.

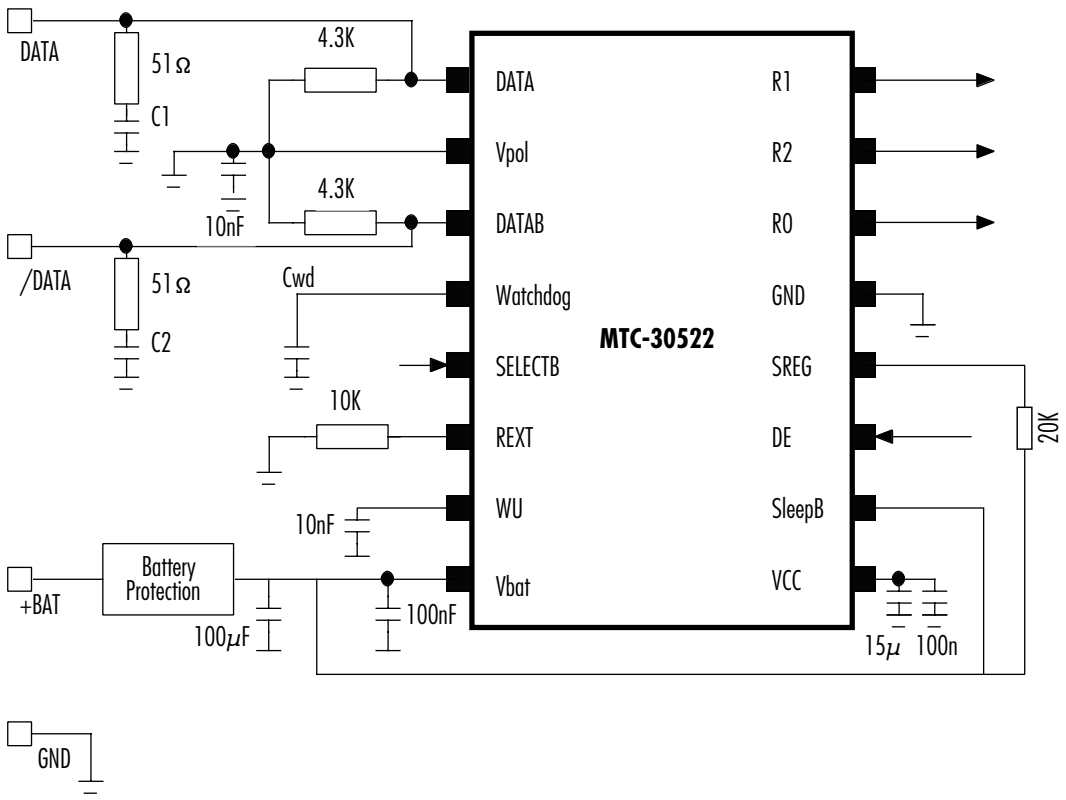


Fig.26: REMX Applications diagram

C1 & C2 = 330pF @ 62,5 kTs/s
150pF @ 125 kTs/s

Cwd = 6,8nF @ 62,5 kTs/s
3,3nF @ 125 kTs/s

17.0 Quality and Reliability

Reliability Performance

In order to fulfil the automotive applications requirements, AMI Semiconductor will commit to quality and reliability goals as described hereunder. AMI Semiconductor commits to analyse failing devices and to define and implement corrective actions to prevent future occurrence of these failures. These targets are valid for component operation within the specified operating conditions.

Failures due to external overstresses such as ESD, voltage and current overstresses which are above this current component spec are not included in this figures.

• External Stress Immunity
- Electrostatic discharges:
The device withstands 2000 Volts
Standardized Human Body Model
ESD pulses when tested according to MIL std 883c method 3015.7 (pin combination 2)
- Latch-up:
Static latch-up protection level is 100mA at 125°C when tested according to JEDEC nr.17.

• The Useful Life
The useful life, when used under moderate conditions, is at least 10 years. The term useful life is specified as the point in the lifetime, where the intrinsic failure rate exceeds the long term failure rate specified under the paragraph: 'The Intrinsic Failure Rate'.

Mechanical and Electrical quality level (up to km 0):

Target in ppm		
98/99	99/00	00/01
98/99	99/00	00/01

Field returns during first year operating:

Target in ppm		
98/99	99/00	00/01
10	10	5

Long-term reliability failure rate:
4 Fits under specified operating conditions.

Quality

Lot-by-lot Acceptance Tests

Lot conformance to specification of products delivered in volume production (after R1 release), is guaranteed by means of following tests:

Test	Conditions	AQL level	Inspection level
Electrical functional and parametric	To product specification at Tamb = 25°C, low and high Temp	0.065	II
External visual	Physical damage to body or leads. Dimensions affecting PCB manufacturability such as bent leads, coplanarity,...	0.065	II
External visual	Correctness of marking. All other cosmetics defects.	0.065	II

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury.

AMI Semiconductor customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify AMI Semiconductor for any damages resulting from such improper use or sale.