2 MEGAPIXEL CMOS DIGITAL IMAGE SENSOR

MT9D001

Micron Part Number: MT9D001C12STC

Features

- DigitalClarity ™ CMOS Imaging Technology
- High frame rate
- Excellent low light performance
- Low dark current
- Simple two-wire serial interface
- Auto black level calibration
- Operating Modes:
  - Snapshot and flash control
  - High frame rate preview
  - Electronic panning
- Programmable Controls
  - Channel gain
  - Frame rate
  - Exposure
  - Window size and panning
- Register and pin compatible with the 1.3MP MT9M001

Table 1: Key Performance Parameters

PARAMETER		TYPICAL VALUE
Optical Format		1/2-inch (4:3)
Active Imager Size		6.7mm(H) x 5.0mm (V), 8.4mm Diagonal
Active Pixels		1600H x 1200V
Pixel Size		4.2um x 4.2um
Color Filter Array		RGB Bayer Pattern
Shutter Type		Electronic Rolling Shutter (ERS)
Max. Data Rate/Max. Master Clock		48 MPS/48 MHz
Frame Rate	UXGA (1600x1200)	20 fps
	SXGA (1280x1024)	28 fps
	VGA (640x480)	100 fps
	CIF (352x288)	230 fps
ADC Resolution		10 bit
Responsivity		1.2 V/lux-sec (550nm)
Dynamic Range		>61dB
SNR_{MAX}		>44dB
Supply Voltage		3.0 to 3.6 Volts (3.3V Nominal)
Power Consumption		250mW (Nominal)
Operating Temperature		0°C to +60°C
Packaging		48 CLCC

Description

Micron® Imaging's 2-megapixel CMOS image sensor features DigitalClarity, our breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS. Our MT9D001 produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of consumer and industrial applications, including digital still cameras, digital video cameras, and PC cameras.

The Micron Imaging MT9D001 is a UXGA-½-inch format CMOS active-pixel digital image sensor. The active imaging pixel array is 1,600H x 1,200V. It incorporates sophisticated camera functions on-chip such as windowing, column and row skip mode, and snapshot mode. It is programmable through a simple two-wire serial interface.

The sensor can be operated in its default mode or programmed by the user for frame size, exposure, gain setting, and other parameters. The default mode outputs a UXGA-size image at 20 frames per second (fps). An on-chip analog-to-digital converter (ADC) provides 10 bits per pixel. FRAME_VALID and LINE-VALID signals are output on dedicated pins, along with a pixel clock that is synchronous with valid data. The MT9D001 is pin-to-pin compatible with the MT9M001.

Figure 1: Sensor Architecture Block Diagram

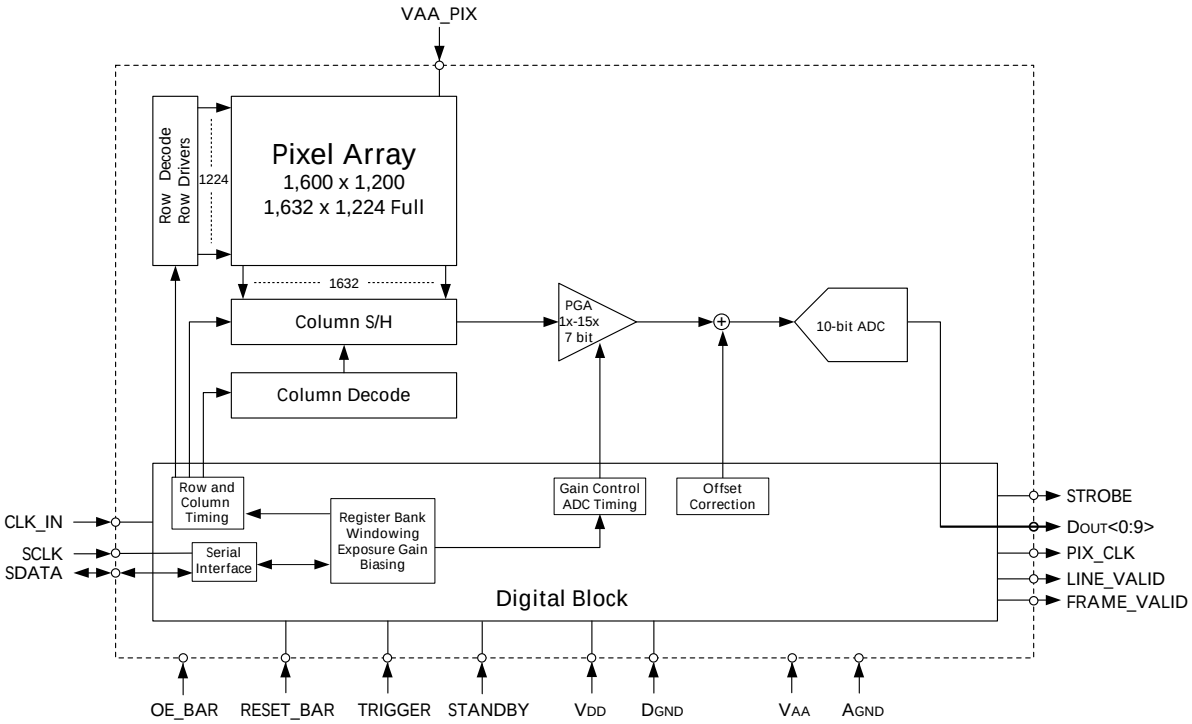


Figure 2: 48-Pin CLCC

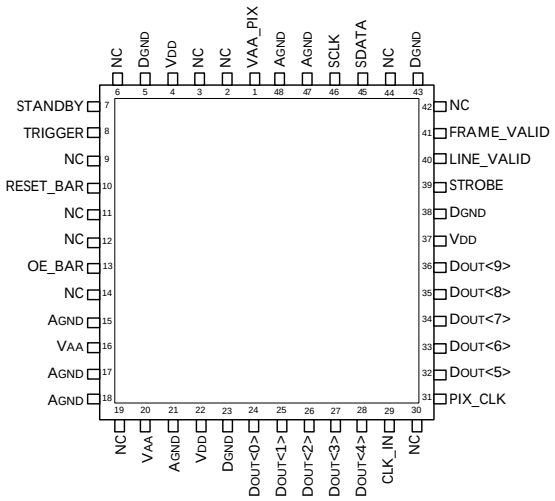


Table 2: Pin Descriptions

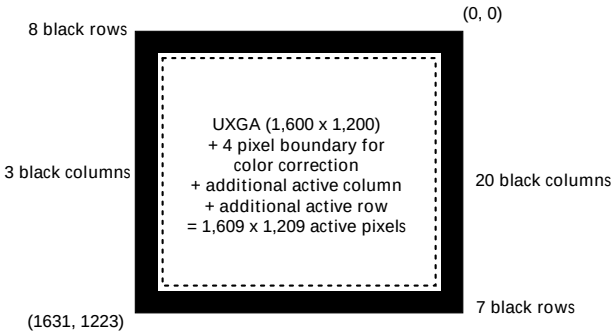
PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
29	CLK_IN	Input	Clock In: Master clock into sensor (48 MHz maximum).
13	OE_BAR	Input	Output Enable: OE_BAR when HIGH places outputs DOUT<0-9>, FRAME_VALID, LINE_VALID, PIX_CLK, and STROBE into a tri-state configuration.
10	RESET_BAR	Input	Reset: Activates (LOW) asynchronous reset of sensor. All registers assume factory defaults.
46	SCLK	Input	Serial Clock: Clock for serial interface.
7	STANDBY	Input	Standby: Activates (HIGH) standby mode, disables analog bias circuitry for power saving mode.
8	TRIGGER	Input	Trigger: Activates (HIGH) snapshot sequence.
45	SDATA	Input/ Output	Serial Data: Serial data bus, requires 1.5KΩ resistor to 3.3V for pull-up.
24–28, 32–36	DOUT<0–9>	Output	Data Out: Pixel data output bits 0, DOUT<9> (MSB), DOUT<0> (LSB).
41	FRAME_VALID	Output	Frame Valid: Output is pulsed HIGH during frame of valid pixel data.
40	LINE_VALID	Output	Line Valid: Output is pulsed HIGH during line of selectable valid pixel data (see Reg0x20 for options).
31	PIX_CLK	Output	Pixel Clock: Pixel data outputs are valid during falling edge of this clock. Frequency = (master clock).
39	STROBE	Output	Strobe: Output is pulsed HIGH to indicate sensor reset operation of pixel array has completed.
15, 17, 18, 21, 47, 48	AGND	Supply	Analog Ground: Provide isolated ground for analog block and pixel array.
5, 23, 38, 43	DGND	Supply	Digital Ground: Provide isolated ground for digital block.
16, 20,	VAA	Supply	Analog Power: Provide power supply for analog block, 3.3V ±0.3V.
1	VAA_PIX	Supply	Analog Pixel Power: Provide power supply for pixel array, 3.3V ±0.3V.
4, 22, 37	VDD	Supply	Digital Power: Provide power supply for digital block, 3.3V ±0.3V.
2, 3, 6, 9, 11, 12, 14, 19, 30, 42, 44	NC	–	No Connect: These pins must be left unconnected.

Pixel Data Format

Pixel Array Structure

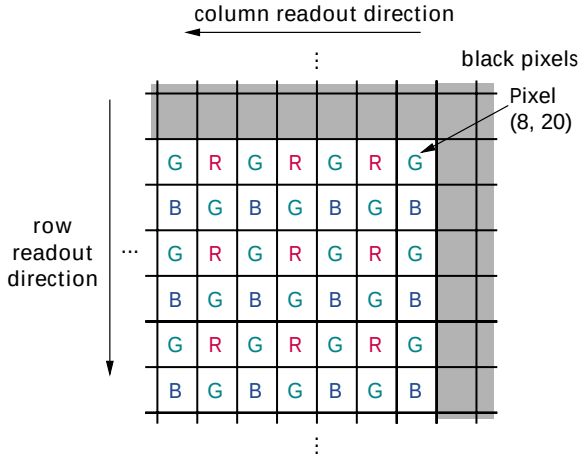
The MT9D001 pixel array is 1,632 columns by 1,224 rows (shown in Figure 3). Columns 0 to 19 and rows 1 to 7 are optically black and can be used to monitor the black level. Note: Row 0 is used for testing purposes only. The last three columns and the last seven rows of pixels are also optically black. The black row data is used internally for the automatic black level adjustment. However, the black rows can also be read out by setting the sensor to raw data output mode (Reg0x20, bit 11 = 1). There are 1,609 columns by 1,209 rows of optically active pixels, which provides a four-pixel boundary around the UXGA (1, 600 x 1, 200) image to avoid boundary effects during color interpolation and correction.

Figure 3: Pixel Array Description



The MT9D001 uses a Bayer color pattern, as shown in Figure 4. The even-numbered rows contain green and red color pixels, and odd numbered rows contain blue and green color pixels. Likewise, the even numbered columns contain green and blue color pixels, and odd numbered columns contain red and green color pixels.

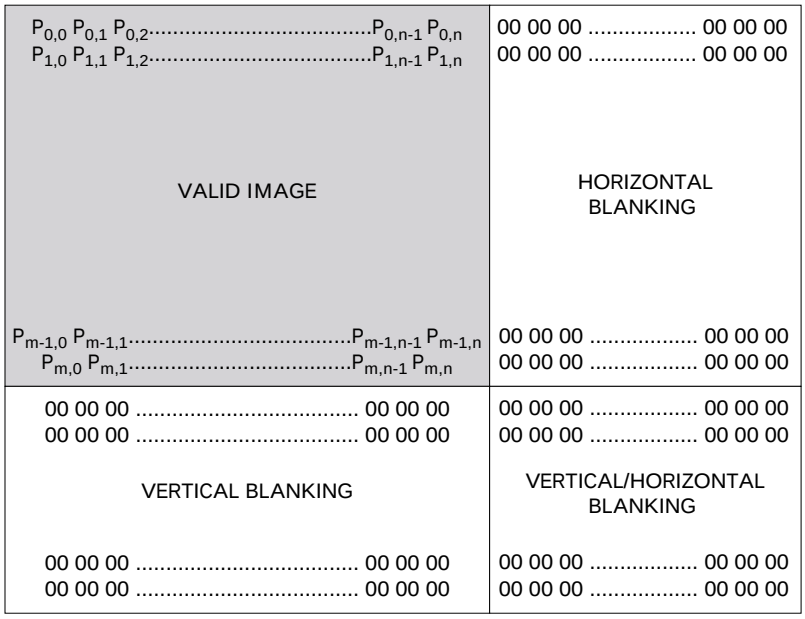
Figure 4: Pixel Color Pattern Detail (Top Right Corner)



Output Data Format

The MT9D001 image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, as shown in Figure 5. The amount of horizontal blanking and vertical blanking is programmable through Reg0x05 and Reg0x06, respectively. LINE_VALID is HIGH during the shaded region of the figure. FRAME_VALID timing is described in the next section.

Figure 5: Spatial Illustration of Image Readout



Output Data Timing

The data output of the MT9D001 is synchronized with the PIX_CLK output. When LINE_VALID is HIGH, one 10-bit pixel datum is output every PIX_CLK period.

The rising edges of the PIX_CLK signal are nominally timed to occur on the rising DOUT edges. This allows PIX_CLK to be used as a clock to latch the data. DOUT data is valid on the falling edge of PIX_CLK. The PIX_CLK is HIGH while master clock is HIGH and then LOW while master clock is LOW. It is continuously enabled, even during the blanking period

Figure 6: Timing Example of Pixel Data

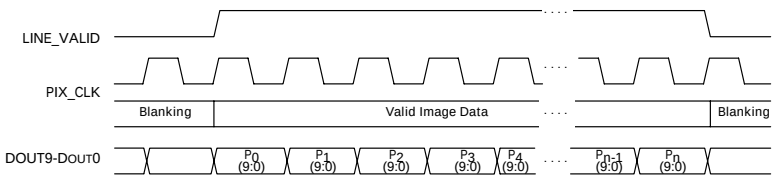
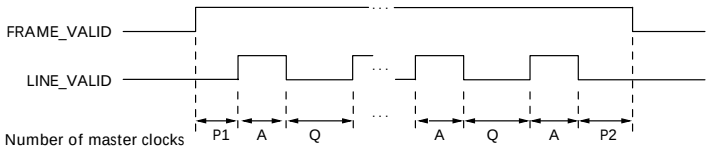


Figure 7: Row Timing and FRAME_VALID/LINE_VALID Signals



Frame Timing Formulas

Table 3: Frame Timing

PARAMETER	NAME	EQUATION (MASTER CLOCK)	DEFAULT TIMING
A	Active Data Time	(Reg0x04 + 1)	1,600 pixel clocks = 33.33µs
P1	Frame Start Blanking	(322)	322 pixel clocks = 6.71µs
P2	Frame End Blanking	(Reg0x05 - 17) (MIN Reg0x05 value = 19)	36 pixel clocks = .075µs
P3	Shutter Overhead	(295)	295 pixel clocks = 6.15µs
Q = P1 + P2	Horizontal Blanking	(305 + Reg0x05) (MIN Reg0x05 value = 19)	358 pixel clocks = 7.46µs
t_{row}	Row Time	P1 + max{(A + P2) OR (P3)}	1,958 pixel clocks = 40.79µs
V	Vertical Blanking	(Reg0x06 + 1) * (t_{row}) (MIN Reg0x06 value = 15)	50,908 pixel clocks = 1.06µs
N_{rows} * (t_{row})	Frame Valid Time	(Reg0x03 + 1) * (t_{row})	2,349,600 pixel clocks = 48.95ms
F	Total Frame Time	(Reg0x03 + 1 + Reg0x06 + 1) * (t_{row})	2,400,508 pixel clocks = 50.01ms

Sensor timing is shown above in terms of pixel clock and master clock cycles (please refer to Figure 6). The recommended master clock frequency is 48 MHz. The vertical blank and total frame time equations assume that the number of integration rows (bits 13 through 0 of Reg0x09) is less than the number of active plus blanking rows (Reg0x03 + 1 + Reg0x06 + 1). If this is not the case, the number of integration rows must be used instead to determine the frame time, as shown in Table 4.

Table 4: Frame Time – Long Integration Time

PARAMETER	NAME	EQUATION (MASTER CLOCK)	DEFAULT TIMING
V'	Vertical Blanking (long integration time)	(Reg0x09 – Reg0x03) * (t_{row})	50,908 pixel clocks = 1.06µs
F'	Total Frame Time (long integration time)	(Reg0x09 + 1) * (t_{row})	2,400,508 pixel clocks = 50.01ms

Serial Bus Description

Registers are written to and read from the MT9D001 through the two-wire serial interface bus. The MT9D001 is a two-wire serial interface slave and is controlled by the two-wire serial clock (SCLK), which is driven by the two-wire serial interface master. Data is transferred into and out through the MT9D001 through the two-wire serial interface data (SDATA) line. The SDATA line is pulled up to 3.3V off-chip by a 1.5KΩ resistor. Either the slave or master device can pull the SDATA line down—the two-wire serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial bus defines several different transmission codes, as follows:

- a start bit
- the slave device eight-bit address
- a(n) (no) acknowledge bit
- an eight-bit message
- a stop bit

Sequence

A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's eight-bit address. The last bit of the address determines if the request will be a read or a write, where a “0” indicates a write and a “1” indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the eight-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data eight bits at a time, with the slave sending an acknowledge bit after each eight bits. The MT9D001 uses 16-bit data for its internal registers, thus requiring two eight-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and eight-bit register address, just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The eight-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A “0” (0xBA) in the LSB (least significant bit) of the address indicates write mode, and a “1” (0xBB) indicates read mode.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred eight bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

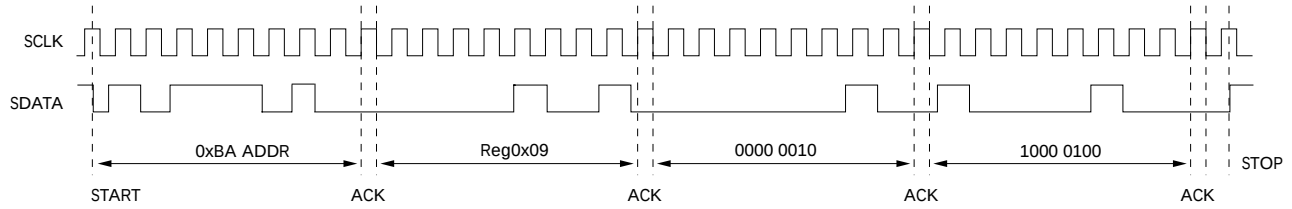
The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

Two-Wire Serial Interface Sample Write and Read Sequences

16-Bit Write Sequence

A typical write sequence for writing 16 bits to a register is shown in Figure 8. A start bit given by the master, followed by the write address, starts the sequence. The image sensor will then give an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each eight-bit transfer, the image sensor will give an acknowledge bit. All 16 bits must be written before the register will be updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

Figure 8: Timing Diagram Showing a Write to Reg0x09 with the Value 0x0284



16-Bit Read Sequence

A typical read sequence is shown in Figure 9. First the master has to write the register address, as in a write sequence. Then a start bit and the read address specifies that a read is about to happen from the register. The master then clocks out the register data eight bits at a time. The master sends an acknowledge bit after each eight-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 9: Timing Diagram Showing a Read from Reg0x09; Returned Value 0x0284

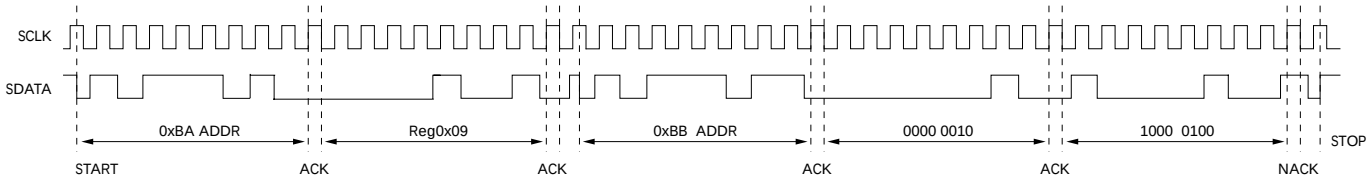


Table 5: Register List and Default Values

Note 1

REGISTER#(HEX)	DESCRIPTION	DATA FORMAT (BINARY)	DEFAULT VALUE (HEX)
0x00	Chip Version	1000 0101 0001 0001	0x8511
0x01	Row Start	0000 0ddd dddd dddd	0x000C
0x02	Column Start	0000 0ddd dddd dddd	0x0018
0x03	Row Size (Window Height)	0000 0ddd dddd dddd	0x04AF
0x04	Col Size (Window Width)	0000 0ddd dddd dddd	0x063F
0x05	Horizontal Blanking	0000 0ddd dddd dddd	0x0035
0x06	Vertical Blanking	0000 0ddd dddd dddd	0x0019
0x07	Output Control	d000 0000 0d00 00dd	0x0002
0x09	Shutter Width	00dd dddd dddd dddd	0x04C9
0x0B	Restart	0000 0000 0000 000d	0x0000
0x0C	Shutter Delay	0000 0ddd dddd dddd	0x0000
0x0D	Reset	0000 0000 0000 000d	0x0000
0x1E	Read Options 1	1000 dddd 00dd dd00	0x8040
0x20	Read Options 2	dd01 0dd1 d00d d10d	0x1104
0x2B	Green1 Gain	0000 0000 0ddd dddd	0x0008
0x2C	Blue Gain	0000 0000 0ddd dddd	0x0008
0x2D	Red Gain	0000 0000 0ddd dddd	0x0008
0x2E	Green2 Gain	0000 0000 0ddd dddd	0x0008
0x35	Global Gain	0000 0000 0ddd dddd	0x0008
0x5F	Cal Threshold	dddd dddd d0dd dddd	0xA39D
0x60[2]	Cal Green1	0000 000d dddd dddd	0x0000
0x61[2]	Cal Green2	0000 000d dddd dddd	0x0000
0x62	Cal Ctrl	d00d d100 1001 1ddd	0x8498
0x63[2]	Cal Red	0000 000d dddd dddd	0x0000
0x64[2]	Cal Blue	0000 000d dddd dddd	0x0000
0xF1	Chip Enable	0000 0000 0000 00dd	0x0001

NOTE:

1. 1 = always 1
   0 = always 0
   d = programmable
2. In default mode, calibration values start at “0” but are set via dark level calibration.

Register Description

Table 6: Register Description

REGISTER	BIT	DESCRIPTION
Chip ID		
0x00	15–0	This register is read-only.
Window Control These registers control the size of the window.		
0x01	10–0	First row to be read out—default = 0x000C (12).
0x02	10–0	First column to be read out—default = 0x0018 (24), register value must be an even number.
0x03	10–0	Window height (number of rows - 1)—default = 0x04AF (1199), minimum value for 0x03 = 0x0002.
0x04	10–0	Window width (number of columns - 1)—default = 0x063F (1599), register value must be an odd number. Minimum value for 0x04 = 0x0003.
Blanking Control These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). Horizontal blanking is specified in terms of pixel clocks. Vertical blanking is specified in terms of row readout times. The actual imager timing can be calculated using Table 3 on page 6.		
0x05	10–0	Horizontal Blanking—default = 0x0035 (53 pixels).
0x06	10–0	Vertical Blanking—default = 0x0019 (25 rows).
Output Control This register controls various features of the output format for the sensor.		
0x07	0	Synchronize changes (copied to Reg0xF1, bit1). 0 = normal operation. Update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal blanking and vertical blanking, window size, row/column skip, or row mirror) at the next frame boundary. 1 = do not update any changes to these settings until this bit is returned to “0.”
	1	Chip Enable (copied to Reg0xF1, bit0). 1 = normal operation. 0 = stop sensor readout. When this is returned to “1,” sensor readout restarts at the starting row in a new frame. The digital power consumption can then also be reduced to less than 5uA by turning off the master clock.
	6	Test Data Generation. 0 = normal operation. 1 = output programmed test data (see Reg0x32). First valid columns will output contents of test data register; second columns will output inverted data. Third columns will output noninverted data, fourth inverted, etc.
	15	Invert Output Pixel Clock—default = 0. When Inv_Pix = 1, the output pixel clock will be an inversion of the input clock.

Table 6: Register Description (continued)

REGISTER	BIT	DESCRIPTION
Pixel Integration Control These registers (along with the window size and blanking registers) control the integration time for the pixels. The formula for calculating the pixel integration time is: Reg0x0C ≤ (Row time - 617)/4 pixel clock cycles: ^{t}INT = (Reg0x09 - 1) * Row time - 180 - (4 x Reg0x0C) Reg0x0C > (Row time - 617)/4 pixel clock cycles: ^{t}INT = (Reg0x09 - 1) * (4 x Reg0x0C + 617) + 439 Where: Row time = Frame Start Blanking + Max{[Active Data Time + Frame End Blanking] OR [Shutter Overhead]} = 322 + MAX{[Reg0x04 + 1) + (Reg0x05 -17)] OR [295]} Overhead time = 180 pixel clock periods Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. If Reg0x09 is increased beyond the total number of rows per frame, the MT9D001 will add additional blanking rows as needed. A second constraint is that ^{t}INT must be adjusted to avoid banding in the image from light flicker. Under 60Hz flicker, this means ^{t}INT must be a multiple of 1/120 of a second. Under 50Hz flicker, ^{t}INT must be a multiple of 1/100 of a second.		
0x09	0-13	Number of rows of integration—default = 0x04C9 (1225).
0x0C	0-10	Shutter delay—default = 0x0000 (0). This is the number of pixel clocks that the timing and control logic waits before asserting the reset for a given row.
Frame Restart		
0x0B	0	Setting bit 0 to “1” of Reg0x0B will cause the sensor to abandon the readout of the current frame and restart from the first row. This register automatically resets itself to 0x0000 after the frame restart. The first frame after this event is considered to be a "bad frame" (see description for Reg0x20, bit0).
Reset		
0x0D	0	This register is used to reset the sensor to its default, power-up state. To reset the MT9D001, first write a “1” into bit 0 of this register. To put in reset mode, then write a “0” into bit 0 to resume operation.

Table 6: Register Description (continued)

REGISTER	BIT	DESCRIPTION
Read Mode 1 In read mode 1, this register is used to control many aspects of the readout of the sensor.		
0x1E	0	Reserved—default is 0; set to zero at all times.
	1	Reserved—default is 0; set to zero at all times.
	2	Column Skip 4—default is 0 (disable). 1 = enable.
	3	Row Skip 4—default is 0 (disable). 1 = enable.
	4	Column Skip 8—default is 0 (disable). 1 = enable.
	5	Row Skip 8—default is 0 (disable). 1 = enable.
	6	Noise suppression—default = 1 (enabled). 0 = disable.
	8	Snapshot Mode—default is 0 (continuous mode). 1 = enable (wait for TRIGGER; TRIGGER can come from outside signal (TRIGGER pin on the sensor) or from serial interface register restart, i.e. programming a “1” to bit 0 of Reg0x0B.
	9	STROBE Enable—default is 0 (no STROBE signal). 1 = enable STROBE (signal output from the sensor during the time all rows are integrating. See STROBE width for more information).
	10	STROBE Width—default is 0 (STROBE signal width at minimum length, 1 row of integration time, prior to line valid going HIGH). 1 = extend STROBE width (STROBE signal width extends to entire time all rows are integrating; width must be > = row size + vertical blanking)
	11	STROBE Override—default is 0 (STROBE signal created by digital logic). 1 = override STROBE signal (STROBE signal is set HIGH when this bit is set, LOW when this bit is set LOW. It is assumed that STROBE enable is set to “0” if STROBE override is being used).
Read Mode 2 This register is used to control many aspects of the readout of the sensor.		
0x20	0	No bad frames—1 = output all frames (including bad frames). 0 (default) = only output good frames. A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, row or column skip, or mirroring.
	2	Reserved—default is 1; set to “1” at all times.
	3	Column skip—1 = read out two columns, and then skip two columns (i.e. col 0, col 1, col 4, col 5...). 0 = normal readout (default).
	4	Row skip—1= read out two rows, and then skip two rows (i.e. row 0, row 1, row 4, row 5...). 0 = normal readout (default).
	6	Reserved—default is 0; set to zero at all times.
	8	Reserved—default is 1; set to “1” at all times.
	9	1 = "Continuous" LINE_VALID (continue producing LINE_VALID during vertical blanking). 0 = normal LINE_VALID (default, no LINE_VALID during vertical blanking.)
	10	1 = LINE_VALID = "Continuous" LINE_VALID XOR FRAME_VALID. 0 = LINE_VALID determined by bit 9.

Table 6: Register Description (continued)

REGISTER	BIT	DESCRIPTION
Gain Settings The gain is individually controllable for each color in the Bayer pattern as shown in the register chart. Formula for gain setting: Gain <= 8 Gain = (Bit[6] + 1) x (Bit[5-0] x 0.125) Gain > 8 (Bit[6] = 1 and Bit[5] = 1) Gain = 8.0 + Bit[2-0] Since Bit[6] of the gain registers are multiplicative factors for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. The following lists the recommended gain settings: Gain — Increments — Recommended Settings 1.000 to 4.000 — 0.125 — 0x08 to 0x20 4.25 to 8.00 — 0.25 — 0x51 to 0x60 9.0 to 15.0 — 1.0 — 0x61 to 0x67		
0x2B	6–0	Green1 gain—default = 0x08 (8) = 1x gain.
0x2C	6–0	Blue gain—default = 0x08 (8) = 1x gain.
0x2D	6–0	Red gain—default = 0x08 (8) = 1x gain.
0x2E	6–0	Green2 gain—default = 0x08 (8) = 1x gain.
0x35	6–0	Global gain—default = 0x08 (8) = 1x gain. This register can be used to set all four gains at once. When read, it will return the value stored in Reg0x2B.
Black Level Calibration These registers are used in the black level calibration. Their functionality is described in detail in the next section.		
0x5F	5–0	Thres_lo—Lower threshold for black level in ADC LSBs—default = 29.
	7	1 = Override automatic Thres_hi and Thres_lo adjust (Thres_hi always = bits 14–8, Thres_lo always = bits 5–0). Default = 1 = Manual Thres_hi and Thres_lo adjustment.
	14–8	Thres_hi—Upper threshold for black level in ADC LSBs—default = 35. Black level maximum is set to this value when bit 7 = 1, black level maximum is reset to this value after every black level average restart if Bit 15 = 1 and bit 7 = 0. If both Bit 15 = 0 and bit 7 = 0, Thresh_hi = Thresh_lo + 5.
	15	No gain dependence—Default = 1. Thres_lo is set by the programmed value of bits 5–0, Thres_hi is reset to the programmed value (bits 14-8) after every black level average restart. 0 = Thres_hi is set automatically, as described above.
0x60	8–0	Cal Green1. Analog offset correction value for Green 1, bits 0–7 sets magnitude, bit 8 set sign. 0 = positive. 1 = negative.
0x61	8–0	Cal Green2. Analog offset correction value for Green 2, bits 0–7 sets magnitude, bit 8 set sign. 0 = positive. 1 = negative.

Table 6: Register Description (continued)

REGISTER	BIT	DESCRIPTION
0x62	0	Manual override of black level correction. 1 = override automatic black level correction with programmed values. 0 = normal operation (default).
	2–1	Force/disable black level calibration. 00 = apply black level calibration during ADC operation only (default). 10 = apply black level calibration continuously. X1 = disable black level correction (Offset Correction Voltage = 0.0V). (In this case, no black level correction is possible).
	4–3	Reserved—default is 1; do not change.
	6–5	Reserved—default is 0; do not change.
	7	Reserved—default is 1; do not change.
	8	Reserved—default is 0; do not change.
	11	1 = do not reset the upper threshold after a black level recalculation sweep. 0 = reset the upper threshold after a black level recalculation sweep (default).
	12	1 = start a new running digitally filtered average for the black level (this is internally reset to “0” immediately), and do a rapid sweep to find the new starting point. 0 = normal operation (default).
	14–13	Reserved—default is 0; set to zero at all times.
	15	1 = do not perform the rapid black level sweep on new gain settings. (Default). 0 = normal operation.
0x63	8–0	Cal Red. Analog offset correction value for Red, bits 0–7 sets magnitude, bit 8 set sign. 0 = positive. 1 = negative.
0x64	8–0	Cal Blue. Analog offset correction value for Blue, bits 0–7 sets magnitude, bit 8 set sign. 0 = positive. 1 = negative.
Chip Enable and Two-Wire Serial Interface Write Synchronize		
0xF1	0	Mirrors the functionality of Reg0x07 bit 1 (Chip Enable). 1 = normal operation. 0 = stop sensor readout. When this is returned to “1,” sensor readout restarts at the starting row in a new frame.
	1	Mirrors the functionality of Reg0x07 bit 0 (Synchronize changes). 0 = normal operation, update changes to registers that affect image brightness (integration time, integration delay, gain, horizontal blanking and vertical blanking, window size, row/column skip, or row/column mirror) at the next frame boundary. 1 = do not update any changes to these settings until this bit is returned to “0.”

Feature Description

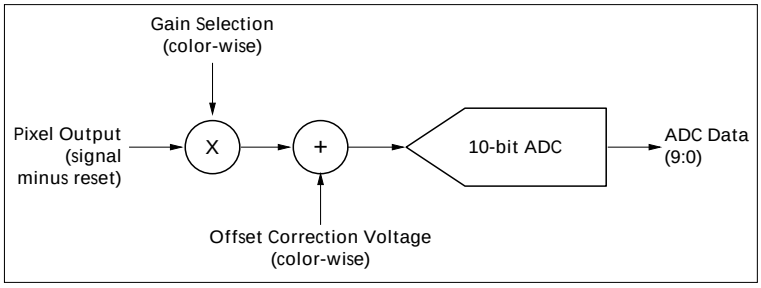
Signal Path

The MT9D001 sensor analog signal path consists of the pixel array, the column sample and hold (S/H) circuitry, the programmable gain stage, the analog offset correction and the analog-to-digital converter (ADC).

The reset and signal voltages from the pixel are sampled onto the column sample and hold circuitry on a row-wise basis. After signal sampling is complete, the differential signal (reset - signal) is transferred to the programmable gain stage.

After the gain stage, the differential signal goes through the analog offset correction circuitry. The user can decide if a positive or negative offset or no offset needs to be added to the differential signal. The signal is then sampled onto the sample and hold circuitry of the ADC before being digitized.

Figure 10: Signal Path



Programmable Gain Stage

Reg0x2B, Reg0x2C, Reg0x2D, Reg0x2E, and Reg0x35

The gain settings can be independently adjusted for Green1, Blue, Red, and Green2 and are programmed through registers Reg0x2B, Reg0x2C, Reg0x2D, and Reg0x2E, respectively. The gain may also be adjusted globally through Reg0x35. The formula for obtaining the gain is shown in Table 7.

Table 7: Obtaining Gain

Gain $\leq$ 8	Gain = (Bit[6] + 1) * (Bit[5-0] * 0.125)
Gain > 8	Gain = 8.0 + Bit[2-0]; Bit[5] = 1 and Bit[6] = 1

For example, for total gain = 12, the value to program is Bit[6-0] = 1100100. The maximum Total gain is 15, i.e. Bit[6-0] = 1100111.

Recommended Gain Settings

The gain circuitry in the MT9D001 is designed for signal gains from one to 15. Any reduction of the gain below this value may cause the sensor to saturate at ADC output values less than the maximum, under certain conditions. It is recommended that this guideline be followed at all times.

Since Bit[6] of the gain registers is a multiplicative factor for the gain settings, there are alternative ways of achieving certain gains. Some settings offer superior noise performance to others, despite the same overall gain. Table 8 lists the recommended gain settings:

Table 8: Recommended Gain Settings at 48 MHz

NOMINAL GAIN	INCREMENTS	RECOMMENDED SETTINGS
1 to 4.000	0.125	0x08 to 0x20
4.25 to 8.00	0.25	0x51 to 0x60
9 to 15	1.0	0x61 to 0x67

Programmable Analog Offset

Reg0x60, Reg0x61, Reg0x62, Reg0x63, and Reg0x64

The programmable analog offset stage corrects for analog offset that might be present in the analog signal. The user would need to program Reg0x62 appropriately to enable the analog offset correction. The analog offset settings can be independently adjusted for the colors of Green1, Green2, Red, and Blue, and are programmed through registers Reg0x60, Reg0x61, Reg0x63, and Reg0x64, respectively. Note that Bit[8] of Reg0x60, Reg0x61, Reg0x63 and Reg0x64 determines the sign of the analog offset. Bit[8] = 1 makes the analog correction negative instead of positive.

The lower eight bits (Bit[7-0]) determines the absolute value of the analog offset to be corrected and Bit[8] determines the sign of the correction. When Bit[8] is "1," the sign of the correction is negative and vice versa. The analog value of the correction relative to the analog gain stage can be determined from the following formula:

Analog offset (Bit[8] = 0) = Bit[7-0] x 2mV
Analog offset (Bit[8] = 1) = - (Bit[7-0] x 2mV)

Note that the 2mV value in the formula is an estimate; it will deviate from 2mV with process variation.

Window Control

Reg0x01, Reg0x02, Reg0x03, and Reg0x04

Window Size

The default programmed window size is 1,600 columns by 1,200 rows (1600H x 1200V). The control logic allows the flexibility to change the window size by programming Reg0x03 and Reg0x04. Reg0x03 controls the window height (number of rows) and Reg0x04 controls the window width (number of columns). The value to be programmed in Reg0x03 is the desired number of rows -1. The value to be programmed in Reg0x04 is the desired number of columns -1.

The minimum value for Reg0x03 is 0x0002; for Reg0x04 is 0x0003. Thus, the smallest window size is four columns by three rows (4H x 3V). Note that the value of Reg0x04 must be an odd number (there can only be even number of columns). It is also important to note that the user can program the window size to be any formats desired; e.g. 8H x 8V, 128H x 128V, 256H x 256V, 640H x 480V, 1,024H x 768V, 1,280H x 1,024V, 640H x 96V, 1,200H x 128V, 1,600H x 256V and so on.

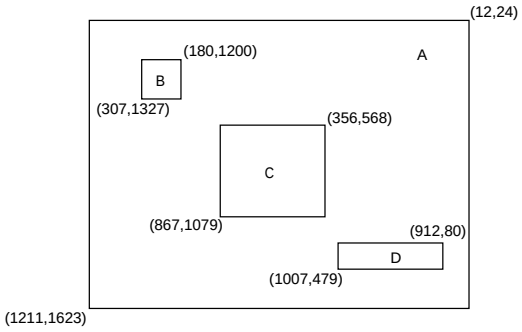
Electronic Panning

In addition to changing the window size, the user has the flexibility to change the location of the readout window. Reg0x01 controls the first row to be read out and Reg0x02 controls the first column to be read out. The default values are 0x000C (decimal 12) for Reg0x01 and 0x0018 (decimal 24) for Reg0x02. Note that the first column to be read out must be an even number.

Reg0x01 and Reg0x02, together with Reg0x03 and Reg0x04, allow the user to choose any segment of the imager array to be read out. This is especially beneficial when the user needs to zoom in on a small portion of the image and perform analysis on the image content.

Figure 11 shows some examples of the electronic panning/zoom-in and windowing capabilities of the sensor.

Figure 11: Windowing Capabilities



	Window Size	Reg0x01	Reg0x02	Reg0x03	Reg0x04
Window A	1,600 x 1,200	0x000C	0x0018	0x04AF	0x063F
Window B	128 x 128	0x00B4	0x04B0	0x0080	0x0080
Window C	512 x 512	0x0164	0x0238	0x0200	0x0200
Window D	400 x 96	0x0390	0x0050	0x0060	0x0190

Blanking Control

Reg0x05 and Reg0x06

Reg0x05 controls the horizontal blanking time in a row. The value is specified in terms of pixel clocks. Default value of 0x0035 for Reg0x05 results in a horizontal blanking time of 358 pixel clocks. The formula for obtaining horizontal blanking time in number of pixel clocks is:

Horizontal blanking time = (305 + Reg0x05) pixel clocks

Note that the minimum value for Reg0x05 is 19; thus, the minimum horizontal blanking time is 324 pixel clocks.

Reg0x06 controls the vertical blanking time. The value is specified in terms of the number of rows. Default value of 0x0019 for Reg0x06 results in a vertical blanking time of 26-row time.

Vertical blanking time = (1 + Reg0x06) x (row time)

Where:

Row time=Frame Start Blanking+Max{[Active Data Time+Frame End Blanking] OR [Shutter Overhead]}

= 322+MAX{[Reg0x04+1)+(Reg0x05 -17)] OR [295]}

Frame Time

Reg0x03, Reg0x04, Reg0x05, and Reg0x06

Total frame time in terms of pixel clocks can be obtained using the following formula:

Total frame time = (number of row readout + vertical blank rows) x (row time)
= (Reg0x03 + 1 + Reg0x06 + 1) x Row Time

Note that the minimum values for the registers are shown in Table 9.

Table 9: Register Minimum Values

REGISTER	MINIMUM VALUE
Reg0x03	0x0002 (2 decimal)
Reg0x04	0x0003 (3 decimal)
Reg0x05	0x0013 (19 decimal)
Reg0x06	0x000F (15 decimal)

The user can change the number of column and row readout, horizontal blanking time, and vertical blanking times to obtain different frame rates.

Column and Row Skip Mode

Reg0x1E and Reg0x20

In addition to specifying the number of columns and rows to be read out, the control logic allows the user to skip the number of columns or rows. This effectively reduces the resolution of the image while maintaining the same field of view. The different skip modes supported are 2x, 4x, and 8x in both the column and row directions. The register bits controlling the different skip modes are shown in Table 10.

Table 10: Skip Modes

REGISTER BIT	SKIP MODES
Reg0x20 Bit[3]	Column skip 2x
Reg0x1E Bit[2]	Column skip 4x
Reg0x1E Bit[4]	Column skip 8x
Reg0x20 Bit[4]	Row skip 2x
Reg0x1E Bit[3]	Row skip 4x
Reg0x1E Bit[5]	Row skip 8x
SKIP MODES	**READOUT**
No column skip	col0, col1, col2, col3, col4, col5, etc.
Column skip 2x	col0, col1, col4, col5, col8, col9, etc.
Column skip 4x	col0, col1, col8, col9, col16, col17, etc.
Column skip 8x	col0, col1, col16, col17, col32, col33, etc.
No row skip	row0, row1, row2, row3, row4, row5, etc.
Row skip 2x	row0, row1, row4, row5, row8, row9, etc.
Row skip 4x	row0, row1, row8, row9, row16, row17, etc.
Row skip 8x	row0, row1, row16, row17, row32, row33, etc.

Figure 12: Column Skip 2x; Row Skip 2x Enabled

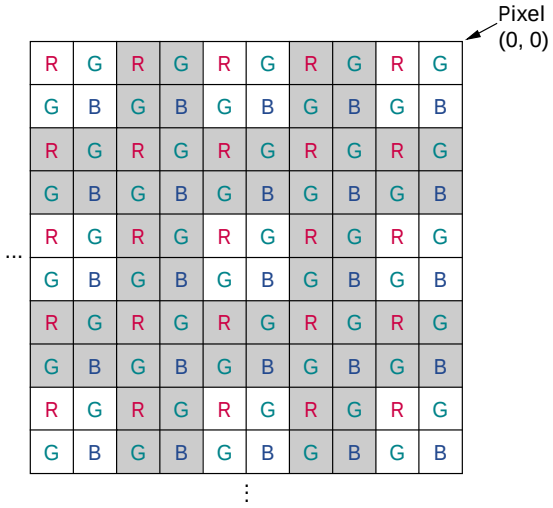


Figure 13: Column Skip 4x; Row Skip 4x Enabled

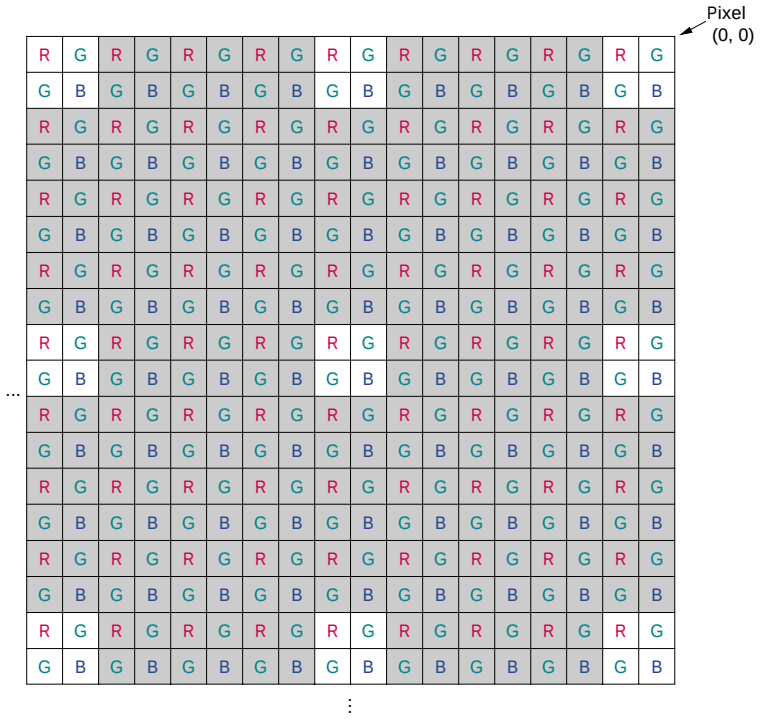


Figure 14: Column Skip 8x; Row Skip 8x Enabled

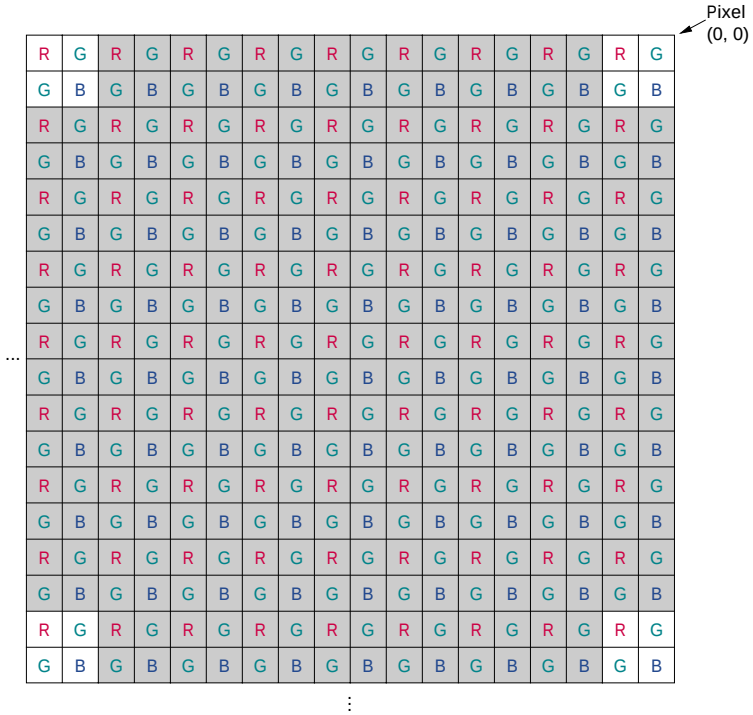


Table 11: Readout Resolution Register Settings

FORMAT	RESOLUTION	ROW SIZE (REG0X03)	COLUMN SIZE (REG0X05)	HORZIONTAL BLANKING (REG0X05)	VERTICAL BLANKING (REG0X06)	SHUTTER WIDTH[1] (REGOX09)	SHUTTER DELAY (REG0X0C)	FRAME RATE
UXGA	1,600H x 1200V	0x04AF	0x063F	0x0035	0x0019	0x04C9	0	20 fps
SXGA	1,280H x 1024V	0x03FF	0x04FF	0x0030	0x0019	0x0418	0	28 fps
XGA	1,024H x 768V	0x02FF	0x03FF	0x001F	0x000F	0x30E	0	45 fps
SVGA	800H x 600V	0x0257	0x031F	0x00AD	0x0019	0x0270	0	60 fps
VGA	640H x 480V	0x01DF	0x027F	0x0017	0x000F	0x01EE	0	100 fps
CIF	352H x 288V	0x011F	0x015F	0x0013	0x0014	0x0133	0	230 fps
QVGA	320H x 240V	0x00EF	0x013F	0x0017	0x000F	0x00FE	0	290 fps
QCIF	176H x 144V	0x008F	0x00AF	0x0013	0x000F	0x009E	0	486 fps

NOTE:

[1] This value is the maximum shutter width for the given Frame Rate.

Smaller Format Resolution

Reg0x01, Reg0x02, Reg0x03, Reg0x04, Reg0x05, Reg0x06, Reg0x1E, and Reg0x20

Utilizing the flexible windowing capability of the sensor enables the user to read out different resolution formats from default of UXGA to SXGA, XGA, SVGA, VGA, CIF, QVGA, QCIF, etc. Table 11 shows some examples of programmable register settings to obtain the estimated frame rates for the desired formats.

The user can change the values of Reg0x05 and Reg0x06 to obtain different frame rates than those shown in Table 11. Note that the field of view of the image will be reduced since the programmed settings effectively reduce the readout window to the specified settings without skipping any rows or columns.

If the user only changes the register settings in Table 11 without changing the row and column start address, the readout window would start from that coordinate. To read out the center of the image or any portion that is desired, the user would need to program Reg0x01 and Reg0x02, thus performing electronic panning.

To maintain the same field of view while reducing the readout resolution, the user would need to perform row and column skip. For example, the desired readout resolution needs to be SVGA (800H x 600V) instead of UXGA (1,600H x 1,200V). To maintain the same field of view, the user can select column skip 2x and row skip 2x modes. This effectively reduces the horizontal and vertical resolution by 2x for a factor of 4x reduction in overall number of pixels that are read out. To perform this readout mode, set the following:

Reg0x03 = 0x04AF	1,200V rows
Reg0x04 = 0x063F	1,600H columns
Reg0x20 Bit[3]=1	Column skip 2x—> 800H columns readout
Reg0x20 Bit[4] = 1	Row skip 2x —> 600V rows readout

Note that if the user sets Reg0x03 = 0x0257 (600V rows), Reg0x04 = 0x031F (800H columns), and then enable Column skip 2x and Row skip 2x, the effective readout resolution will be 400H x 300V.

High Frame Rate Readout Modes

Reg0x01, Reg0x02, Reg0x03, Reg0x04, Reg0x05, and Reg0x06

In addition to having the flexibility to readout smaller standard formats, the sensor allows the option of reading out non-standard formats. This is particularly useful when zooming into a particular segment of the image to perform high-speed mathematical calculations (high-speed viewfinder or auto-focus applications).

In applications such as the auto-focus mode, the user may need more horizontal resolution than vertical. Thus, the user can window down to the midsection of the imager array by programming Reg0x01 and Reg0x03 to change the row start address and the window height. Figure 15 is an example of windowing down to 1,600H x 512V from the default of 1,600H x 1,200V.

Figure 15: Windowing

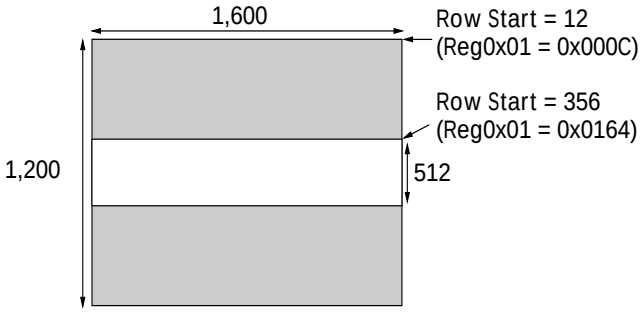


Table 12 shows different types of high-frame rate readout modes available. Note that Reg0x05 and Reg0x06 have been set to the minimum values. The frame rate derived for each of the resolutions shown is the estimated fastest frame rate available for that particular resolution. The user can change Reg0x05, Reg0x06 to obtain the desired frame rate.

Note that the user may also want to perform row skip modes to obtain larger field of view if high-frequency vertical resolution is not critical.

Table 12: High Frame Rate Readout Modes

RESOLUTION	ROW SIZE (REG0X03)	COLUMN SIZE (REG0X04)	HORIZONTAL BLANKING (REG0X05)	VERTICAL BLANKING (REG0X06)	SHUTTER WIDTH[1] (REGOX09)	SHUTTER DELAY (REG0X0C)	FRAME RATE
1,600H x 512V	0x01FF	0x063F	0x0013	0x000F	0x04C9	0	47 fps
1,600H x 256V	0x00FF	0x063F	0x0013	0x000F	0x0418	0	92 fps
1,600H x 128V	0x007F	0x063F	0x0013	0x000F	0x30E	0	173 fps
512H x 512V	0x01FF	0x01FF	0x0013	0x000F	0x0270	0	109 fps
256H x 256V	0x00FF	0x00FF	0x0013	0x000F	0x01EE	0	286 fps
128H x 128V	0x007F	0x007F	0x0013	0x000F	0x0133	0	540 fps
64H x 64V	0x003F	0x003F	0x0013	0x000F	0x00FE	0	972 fps

NOTE:

[1] This value is the maximum shutter width for the given Frame Rate.

Pixel Integration Time Control

Reg0x09 and Reg0x0C

The integration time of the pixel is the amount of time the pixels are set to collect charges generated from light. The user can change the integration time of the sensor by programming Reg0x09. The value of Reg0x09 sets the number of row time for integration. The sensor also supports sub-row integration time for fine control of pixel integration time.

The formula for calculating the pixel integration time is:

Reg0x0C < (row time - 617)/4 pixel clock cycles:

t_{INT} = (Reg0x09 -1) * row time - 180 - (4* Reg0x0C)

Reg0x0C > (row time - 617)/4 pixel clock cycles:

t_{INT} = (Reg0x09 -1) * (4* Reg0x0C +617) + 439

Where:

Row time=Frame Start Blanking+Max{[Active Data Time+Frame End Blanking] OR [Shutter Overhead]}

= 322+MAX{[Reg0x04+1)+(Reg0x05 -17)] OR [295]}

Overhead time = 180 pixel clock periods

Typically, the value of Reg0x09 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is not affected by the integration time. However, if Reg0x09 is increased beyond the total number of rows per frame, then additional blanking rows are added as needed.

While the user can adjust the integration time to the desired value according to the aforementioned formula, not all integration times may be desired under certain lighting conditions. If the light source has a flicker component, then the integration time needs to be set properly to avoid banding in the image from light.

Under 60 Hz flicker, the integration time must be a multiple of 1/120 of a second to avoid flicker. Under 50 Hz flicker, the integration time must be a multiple of 1/100 of a second to avoid flicker.

Frame Restart

Reg0x0B

Setting Bit[0] of Reg0x0B to "1" will cause the sensor to abandon the readout of the current frame and restart from the first readout row. This register automatically resets itself to 0x0000 after the frame restarts. The first frame after this event is considered to be a bad frame with no data output.

Sensor Reset

Reg0x0D and RESET_BAR

There are two ways to reset the sensor:

1. Use RESET_BAR (pin 10) by pulling the RESET_BAR signal to 0V. The RESET operation is an asynchronous reset and the sensor will remain in reset as long as RESET_BAR = 0V.
2. Program Reg0x0D Bit[0] = 1. The sensor will remain in reset mode until Reg0x0D Bit[0] is reprogrammed with a value of "0." In both methods of reset, the sensor register settings will return to the default power-up state.

Standby Control and Chip Enable

Reg0x27, STANDBY pin

There are two ways to set the sensor in standby mode:

1. Through the two-wire serial interface program Reg0x07 Bit[1] = 0. This stops the sensor readout and powers down the digital logic and the analog circuitry of the sensor. The sensor will stay in standby mode until the user reprograms Reg0x07 Bit[1] = 1. To further reduce the power consumption in standby mode, the user can stop the master clock going into the sensor.
2. Set STANDBY (pin 7) to HIGH with Reg0x27 in default settings. The sensor allows the user to control the activation polarity of the standby pin. If Reg0x27 Bit[2] is programmed "0" then STANDBY = 0 will activate the standby mode. To further reduce the power consumption in standby mode, the user can stop the master clock going into the sensor.

Pixel Clock Control

Reg0x07

The pixel data from the sensor changes at the rising edge of the pixel clock. Thus, the user should latch the data at the falling edge of the pixel clock since this is when the data is valid. However, the user may not have the ability to grab the data at the falling edge of the pixel clock. The pixel clock polarity can be reversed by programming Reg0x07 Bit[15] = 1. When programmed, the pixel clock can be an inversion of the input clock. The pixel data will now change at the falling edge of the pixel clock and will be valid during the rising edge the of pixel clock.

Snapshot Mode and Flash Control

Reg0x1E, STROBE pin, and TRIGGER pin

Setting up for Snapshot Mode

Snapshot mode must be enabled before use by setting bit 8 = 1 of Reg0x1E. There are two important signals used for snapshot mode: TRIGGER and STROBE. The TRIGGER signal initiates the start of a single frame capture and STROBE is an output pulse that may be used to turn on a flash and/or activate a mechanical shutter.

Triggering A Snapshot

The TRIGGER signal required for starting a frame capture may be generated in the following two ways:

1. External TRIGGER Pulse
   Pin 8 is a digital input that may be used to supply an external trigger signal input. The snapshot operation begins after the TRIGGER pulse transitions from a HIGH to LOW state.
2. TRIGGER from Register Setting
   A second method for triggering a snapshot is by setting bit 0 = 1 of Reg0x0B (Restart). This register automatically returns bit 0 to "0" after the TRIGGER is initiated. This bit does not need to be reset by the user after use.

STROBE Pulse Output

The STROBE pulse must be enabled before use by setting bit 9 = 1 of Reg0x1E. The STROBE signal has two options for pulse length and may be selected using bit 10 of Reg0x1E, as shown in Table 13.

Note that the Shutter_Width Reg0x09 must be greater than or equal to the Row_Width Reg0x04 + 16 to provide a pulse.

Table 13: STROBE Pulse Output

REGISTER 0X1E, BIT 10	STROBE PULSE WIDTH
0	1 Row Time (default)
1	[((Shutter_Width - Row_Width) - 15) * Row_Time][((Reg0x09[13..0] - Reg0x04[10..0]) - 15) * Row_Time]

Table 14 shows default row times for various pixel clocks/frame rates.

Table 14: Default Rows

PIXEL CLOCK/FRAME RATE	DEFAULT ROW TIME
48 MHz / 20 fps	40.79µs
24 MHz/ 10 fps	81.58µs
12 MHz/ 5 fps	163.16µs

After the TRIGGER pulse has signaled a snapshot operation, each row of the imager array is reset in sequence to clear out any accumulated signal. Once each row of the imager is reset, the STROBE pulse is output from the imager with a length dependent upon the characteristics described above. After the STROBE pulse goes LOW, the imager waits eight additional rows. After that, each row from the pixel array is read out.

LINE_VALID Formats

Reg0x20

By setting Bit 9 and 10 of Reg0x20 the LINE_VALID signal can get three different output formats. The formats (Figure 16) are shown when reading out four rows and two vertical blanking rows. In the last format, the LINE_VALID signal is the XOR between the continuously LINE_VALID signal and the FRAME_VALID signal.

Figure 16: Different LINE_VALID Formats

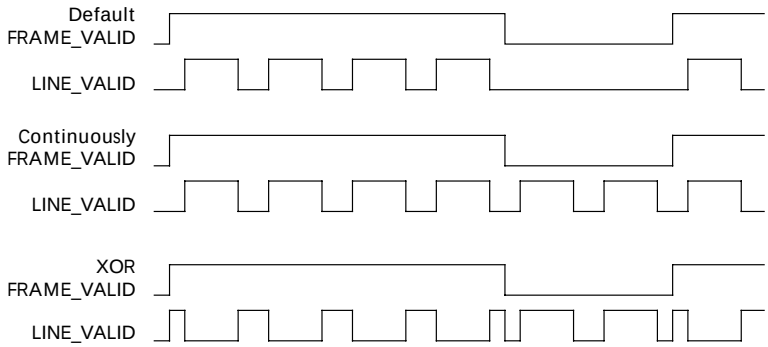
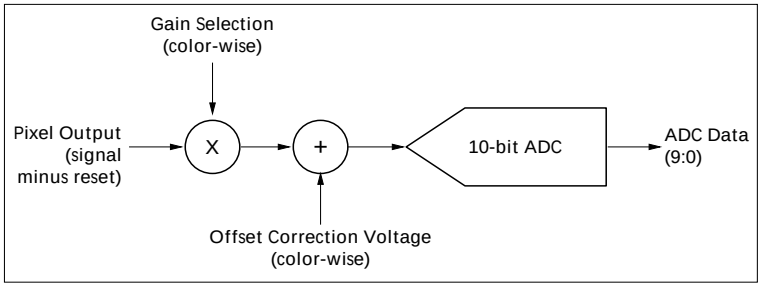


Figure 17: Black Level Calibration Flow Chart



Black Level Calibration

Reg0x5F, Reg0x60, Reg0x61, Reg0x62, Reg0x63, and Reg0x64

The digitized black level of the sensor will potentially vary with temperature or gain setting changes. The sensor allows the user the flexibility of automatic black level calibration or manual black level control.

Noise Suppression

Reg0x1E

In default, the noise suppression is enabled. To disable the suppression set Reg0x1E:Bit[6] = 0. In high-gain applications, the sensor is more sensitive to noise.

Table 15: Black Level Registers

REGISTERS	BITS	DESCRIPTION
Automatic Black Level Calibration Reg0x5F:bit[7]=0, Reg0x62:bit[0]=0		
		In the automatic black level calibration mode, the sensor measures the average of 256 pixels from two dark rows for each of the red, green, and blue pixels. The average is then digitally filtered over many frames. This average is compared to a minimum (lower threshold) and a maximum (upper threshold) acceptable levels. If the average is lower than the lower threshold level, the offset correction voltage for that color is increased by 1 offset LSB. Note that the offset LSBs do not match ADC LSBs. Typically, one offset LSB is approximately 2mV. If the average is above the upper threshold level, the offset correction is decreased by one offset LSB. However, if the average black level shifts from below the lower threshold to above the upper threshold, the upper threshold will be adjusted upwards automatically. This will prevent black level oscillation. The new upper threshold is updated based on the following: If new black level < 64: Thres_hi = Thres_lo + 2 + (2 x Delta) If new black level > 63 and < 119: Thres_hi = new black level + 4 If new black level > 119: Thres_hi = 123 Delta = new black level - Thres_lo In default mode, Reg0x5F:bit[15] = 1 so the lower threshold does not vary with gain settings. However, if the user prefers to have the lower threshold changes with gain settings, set Reg0x5F:bit[15] = 0. The lower threshold is updated based on the following formula: $Thres\_lo = RegGain_{max}/4 \times (RegGain_{max}, bit\ 6 + 1) \times (RegGain_{max}, bit\ 7 + 1)$ $RegGain_{max}$ is the maximum of the four independent gain register settings. In default, the lower threshold is 29 (0x1D) and the upper threshold is 35 (0x23). The user can change the lower and upper thresholds through bits[5–0] and bits[14–8] of Reg0x5F, respectively. In default mode, these thresholds will not vary with gain. Whenever the gain or any of the readout timing registers is changed (shutter width, vertical blanking, number of rows or columns, or the shutter delay) or if the black level recalculation bit, reset bit or restart bit is set, the running digitally filtered average is reset to the first average of the dark pixels. The digital filtering over many frames is then restarted. Whenever the gain or the readout timing registers are changed, the upper threshold is restored to its default value. After changes to the sensor configuration, large shifts in the black level calibration can result. To quickly adapt to this shift, a rapid sweep of the black level during the dark row readout is performed on the first frame after certain changes to the sensor registers. Any changes to the registers listed above will cause this recalculation. The data from this sweep allows the sensor to choose an accurate new starting point for the running average. This procedure can be disabled as described under Reg0x5F.

Table 15: Black Level Registers (continued)

REGISTERS	BITS	DESCRIPTION
Black Level Thresholds		
Reg0x5F This register controls the operation of the black level calibration thresholds.		
	15	No gain dependence. 1 = Thres_lo is set by the programmed value of bits 5–0, Thres_hi is reset to the programmed value (bits 14-8) after every black level average restart. 0 = Thres_lo and Thres_hi are set automatically as described below.
	14–8	Thres_hi: Maximum allowed black level in ADC LSBs (default = Thres_lo + 5). Black level maximum is set to this value when bit 7 = 1, black level maximum is reset to this value after every black level average restart if Bit 15 = 1 and bit 7 = 0.
	7	1 = override automatic Thres_hi and Thres_lo adjust. (Thres_hi always = bits 14–8, thres_lo always = bits 5–0). 0 = automatic Thres_hi and Thres_lo adjustment.
	5–0	Thres_lo—Lower threshold for black level in ADC LSBs.
After any recalculation of the black level and average restart, Thres_hi is reset to either Thres_lo + 5. (automatic, default mode), Thres_hi (bit 7 = 1). Reg0x62, bit 11 will override this.		
Black Level Control Reg0x62 This register is used to control the automatic black level calibration circuitry.		
	15	1 = do not perform the rapid black level sweep on new gain settings. 0 = normal operation.
	14–13	Reserved—default is 0; do not change.
	12	1 = start a new running digitally filtered average for the black level (this is internally reset to “0” immediately), and do a rapid sweep to find the new starting point.
	11	1 = do not reset the upper threshold after a black level recalculation sweep. 0 = reset the upper threshold after a black level recalculation sweep (default).
	8	Reserved—default is 0; do not change.
	7	Reserved—default is 1; do not change.
	6–5	Reserved—default is 0; do not change.
	4–3	Reserved—default is 1; do not change.
	2–1	Force/disable black level calibration. 00 = apply black level calibration during ADC operation only (default). 10 = apply black level calibration continuously. X1= disable black level correction (Offset Correction Voltage = Skew Voltage = 0.0V). (In this case, no black level correction is possible.)
	0	Manual override of black level correction. 1 = override automatic black level correction with programmed values. 0 = normal operation (default).

Table 15: Black Level Registers (continued)

REGISTERS	BITS	DESCRIPTION
Manual Black Level Calibration Reg0x60, Reg0x61, Reg0x62, Reg0x63, Reg0x64		
		Instead of using the automatic black level correction, the user can override the black level correction values with programmed values. To enable the manual correction, the user needs to set Reg0x62 Bit[0] = 1. The analog offset for each of the color pixels can then be programmed through Reg0x60, Reg0x61, Reg0x63, Reg0x64 for Green1, Green2, Red, and Blue colors, respectively. These registers contain the nine-bit signed black level calibration values for the four colors in the Bayer pattern. This feature can be used in conjunction with readout of the black rows (Reg0x20, bit 11) if the user would like to use an external black level calibration circuit. The offset correction voltage is generated according to the following formula: Offset Correction Voltage = (9-bit signed calibration value, -256 to 255) * (2mV) * Enable bit ADC input voltage = Pixel Output Voltage * Analog Gain - Offset Correction

Electrical Specifications

Table 16: DC Electrical Characteristics

(V_{PWR} = 3.3 ±0.3V; T_A = 25°C)

SYMBOL	DEFINITION	CONDITION	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	Input High Voltage		V_{PWR} - 0.3		V_{PWR} + 0.3	V	
V_{IL}	Input Low Voltage		-0.3		0.8	V	
I_{IN}	Input Leakage Current	No Pull-up Resistor; V_{IN} = V_{PWR} or V_{GND}	-15		15	µA	
V_{OH}	Output High Voltage		V_{PWR} - 0.2			V	
V_{OL}	Output Low Voltage			0.0	0.2	V	
I_{OZ}	Tri-state Output Leakage Current				15	µA	
I_{PWRA}	Analog Quiescent Supply Current	Default settings	TBD	50	TBD	mA	
I_{PWRD}	Digital Quiescent Supply Current	CLK_IN = 48 MHz; default setting, C_{LOAD} = 10pF	16	22		mA	
I_{PWRA} Standby	Analog Standby Supply Current	STDBY = V_{DD}	TBD	TBD	TBD	µA	1
I_{PWRD} Standby	Digital Standby Supply Current	STDBY = V_{DD}, CLK_IN = 0 MHz	TBD	TBD	TBD	µA	1
I_{PWRD} Standby ClkOn	Digital Standby Supply Current with Clock On	STDBY = V_{DD}, CLK_IN = 48 MHz	TBD	TBD	TBD	µA	

NOTE:

1. To place the chip in standby mode, first raise STANDBY to V_{DD}, then wait two master clock cycles before turning off the master clock. Two master clock cycles are required to place the analog circuitry into standby, low-power mode.

Table 17: AC Electrical Characteristics

(V_{PWR} = 3.3 ±0.3V; T_A = 25°C; CLK_IN at 48 MHz)

SYMBOL	DEFINITION	CONDITION	MIN	TYP	MAX	UNITS
FCLK_IN	Input Clock Frequency Clock		1		48	MHz
	Duty Cycle		45/55		55/45	MIN/MAX
t_R	Input Clock Rise Time		TBD	TBD	TBD	ns
t_F	Input Clock Fall Time		TBD	TBD		ns
t_{PLHP}	CLK_IN to PIX_CLK propagation delay, LOW-to-HIGH	C_{LOAD} = 10pF	4	5	6	ns
t_{PLHP}	CLK_IN to PIX_CLK propagation delay, HIGH-to-LOW	C_{LOAD} = 10pF	6	7	8	ns
t_{PLHD}	CLK_IN to D_{OUT}<9-0> propagation delay, LOW-to-HIGH	C_{LOAD} = 10pF		TBD		
t_{PLHD}	CLK_IN to D_{OUT}<9-0> propagation delay, HIGH-to-LOW	C_{LOAD} = 10pF		TBD		
t_{OH}	Data Hold Time			TBD		
$t_{PLHF,L}$	CLK_IN to FRAME_VALID and LINE_VALID propagation, LOW-to-HIGH		TBD	TBD	TBD	ns
$t_{PHLF,L}$	CLK_IN to FRAME_VALID and LINE_VALID propagation, HIGH-to-LOW		TBD	TBD	TBD	ns

Propagation Delay for FRAME_VALID and LINE_VALID Signals

The FRAME_VALID and LINE_VALID signals change on the same falling master clock edge as the data output. The LINE_VALID goes HIGH on the same rising master clock edge as the output of the first valid pixel's data and returns LOW on the same master clock rising edge as the end of the output of the last valid pixel's data.

As shown in the "Output Data Format" on page 5 and "Output Data Timing" on page 5, FRAME_VALID goes HIGH 322 pixel clocks prior to the time that the first LINE_VALID goes HIGH. It returns LOW at a time corresponding to (Reg0x05 - 17 pixel clocks) after the last LINE_VALID goes LOW.

The typical output delay, relative to the master clock edge, is 7.5 ns. Note that the data outputs change on the rising edge of the master clock.

Figure 18: Propagation Delays for FRAME_VALID and LINE_VALID Signals

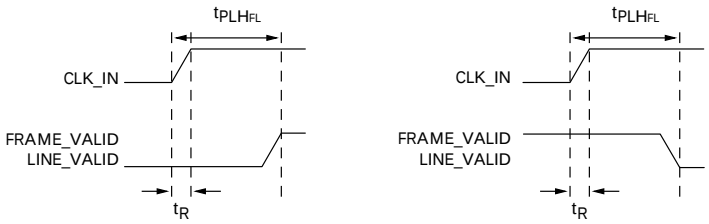
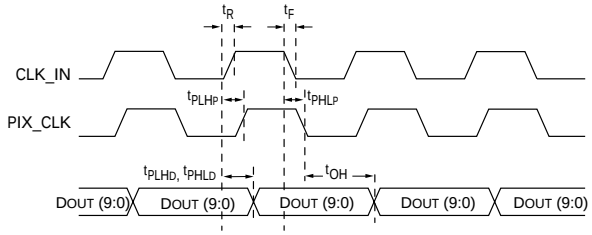


Figure 19: Propagation Delays for PIX_CLK and Data Out Signals



Two-Wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the following diagrams in master clock cycles.

Figure 20: Serial Host Interface Start Condition Timing

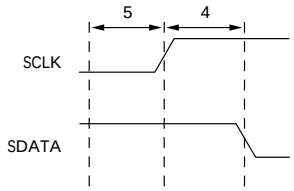
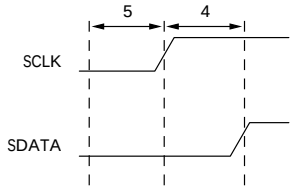


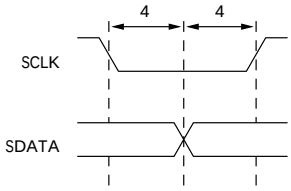
Figure 21: Serial Host Interface Stop Condition Timing



NOTE:

All timing are in units of master clock cycle.

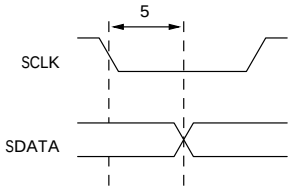
Figure 22: Serial Host Interface Data Timing for Write



NOTE:

SDATA is driven by an off-chip transmitter.

Figure 23: Serial Host Interface Data Timing for Read



NOTE:

SDATA is pulled LOW by the sensor, or allowed to be pulled HIGH by a pull-up resistor off-chip.

Figure 24: Acknowledge Signal Timing After an 8-Bit Write to the Sensor

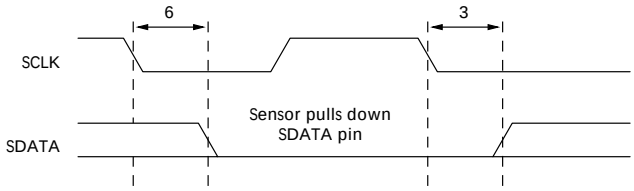
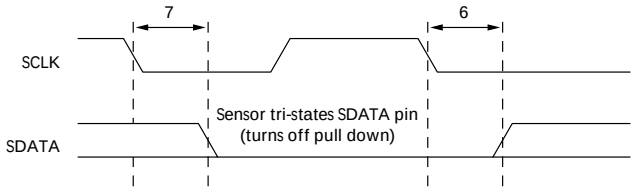


Figure 25: Acknowledge Signal Timing After an 8-Bit Read from the Sensor



NOTE:

After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. When read sequence is complete, the master must generate a no acknowledge by leaving SDATA to float HIGH. On the following cycle, a start or stop bit may be used.

Image Center Offset and Orientation

Figure 26: Image Center Offset

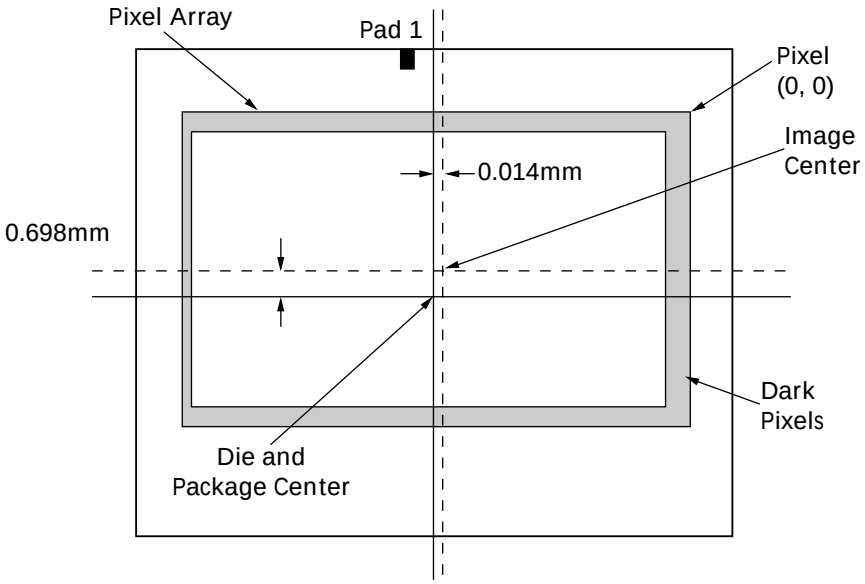


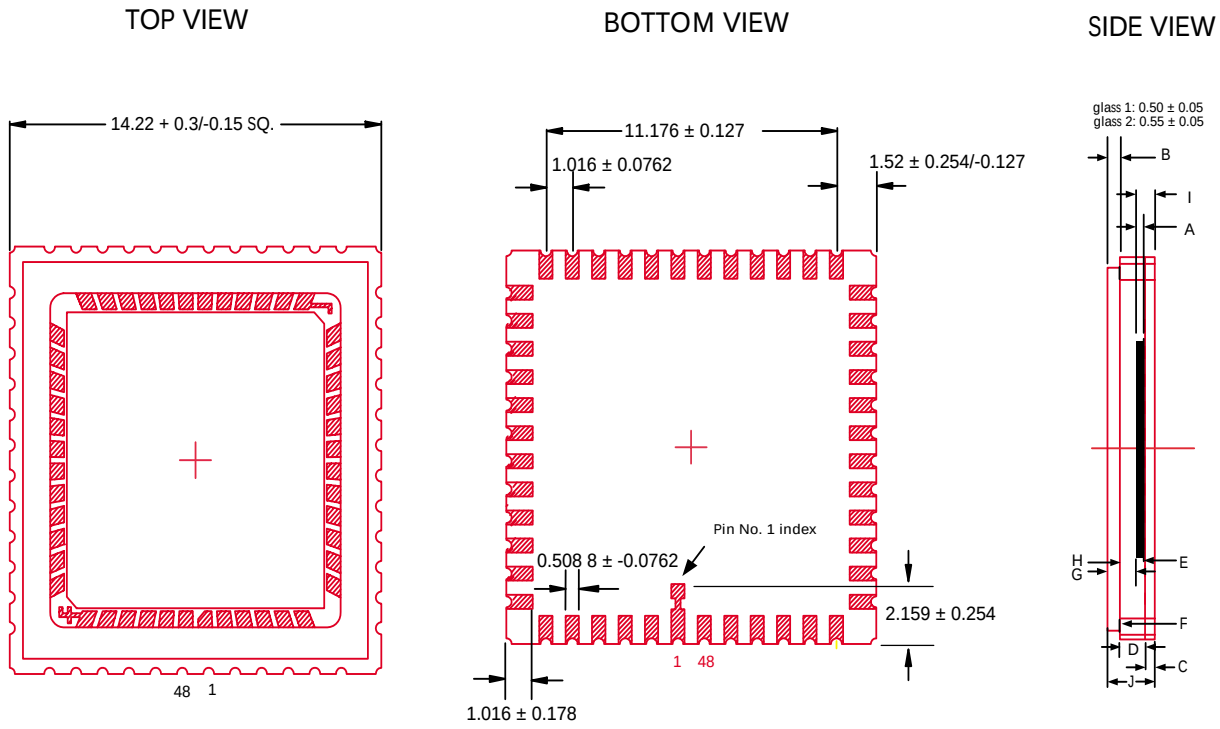
Table 18: Optical Area Dimensions

OPTICAL AREA	PIXEL	X-DIMENSION	Y-DIMENSION
UXGA	Center of pixel (24, 12)	3,373.7µm	3,217.7µm
	Center of Pixel (1623,1211)	-3,346.4µm	-1,822.2µm

NOTE:

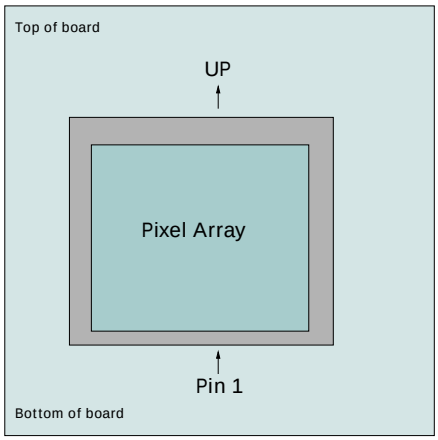
1. X and Y coordinates referenced to center of die.
2. Die center = package center.

Figure 27: Package Drawing



Description		Units (mm)		
		nominal	min	max
A	Die thickness	0.725	0.705	0.745
B	Glass thickness	0.525	0.450	0.600
C	Base layer thickness	0.510	0.460	0.560
D	Dam thickness	1.140	1.010	1.270
E	Die attach bondline thickness	0.035	0.020	0.050
F	Glass attach bondline thickness	0.035	0.020	0.050
G	Sensor array to outer glass lid	0.940	0.685	1.195
H	Sensor array to inner glass lid (air gap)	0.415	0.235	0.595
I	Sensor array to seating plane	1.270	1.185	1.355
J	Package total thickness	2.210	1.940	2.480

Figure 28: Optical Orientation



Data Sheet Designation

Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

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