MT92101

IP Phone Processor

Preliminary Information

DS5251 ISSUE 1 February 2000

Features

- Low Voltage Operation, 1.65 to 1.95 Volts
- Standard 3.3 Volt Signal Interfaces
- On-chip RISC CPU and Powerful DSP
- Standard Integrated System Interfaces
- Embedded Physical Layer Firmware
- G.729.AB and G.723.1A Vocoders, including VAD and CNG*
- Group 3 Fax Relay, 2400 – 14400 bps
- H.323, MGCP, or SIP Protocol Software Available
- JTAG Port for Debug and Boundary Scan

Applications

- Voice over IP Enterprise Telephones and Related Equipment

* subject to patent indemnification

Ordering Information

MT92101A/PR/BP1R 288 Ball PBGA
MT92101A/PR/GP1R 208 Pin QFP

-40°C to +85°C

Description

The MT92101 IP Phone Processor provides a highly integrated solution for an IP phone for use in enterprise applications. The IP Phone Processor integrates an ARM-Thumb RISC CPU and supporting subsystem including dual Ethernet MAC and bridge, together with an OAKDSPCore™, full RAM and ROM and a supporting subsystem. Firmware is embedded to allow the implementation of multi-channel voice compression, echo cancellation and supporting functions on the DSP.

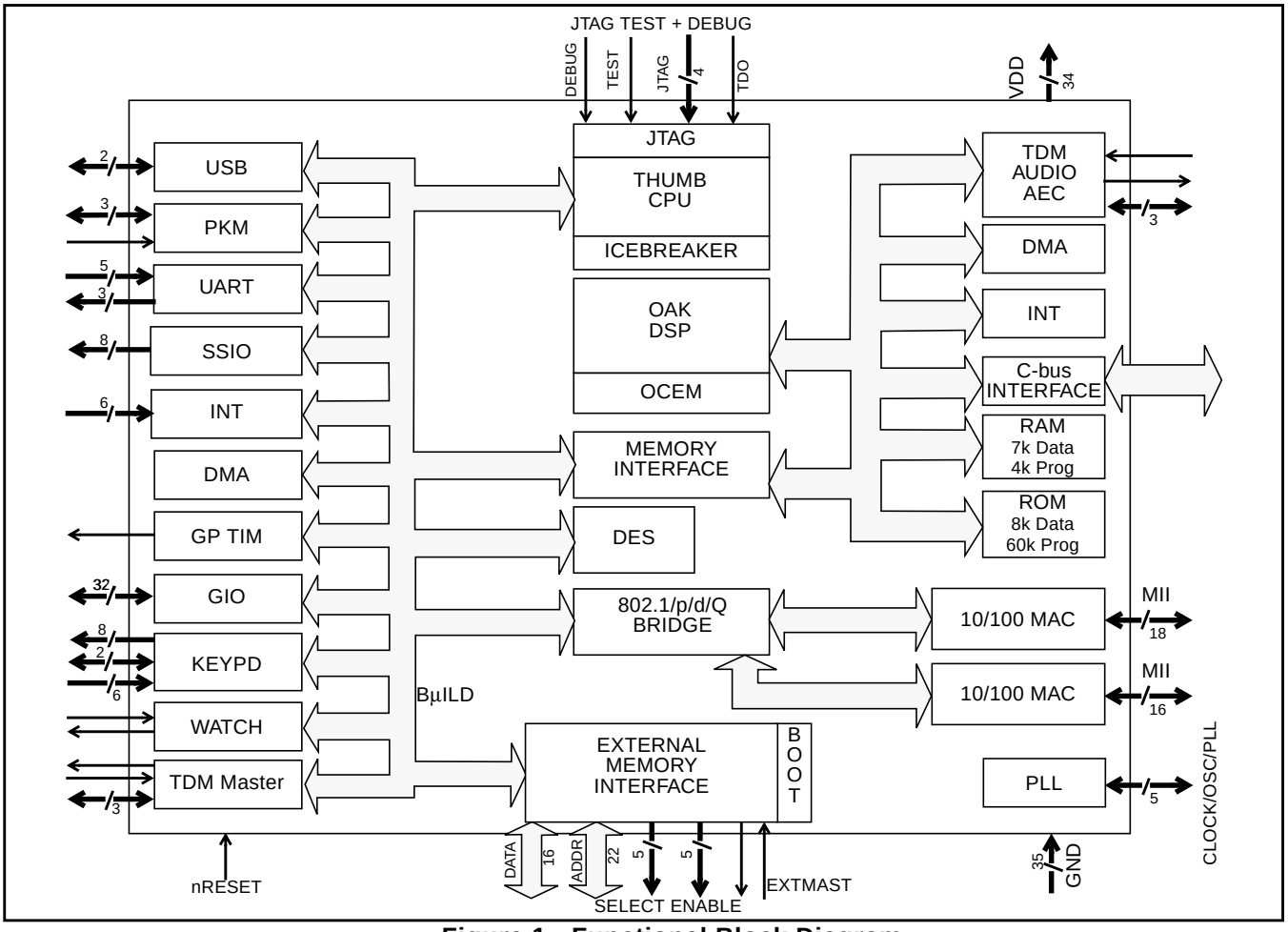


Figure 1 - Functional Block Diagram

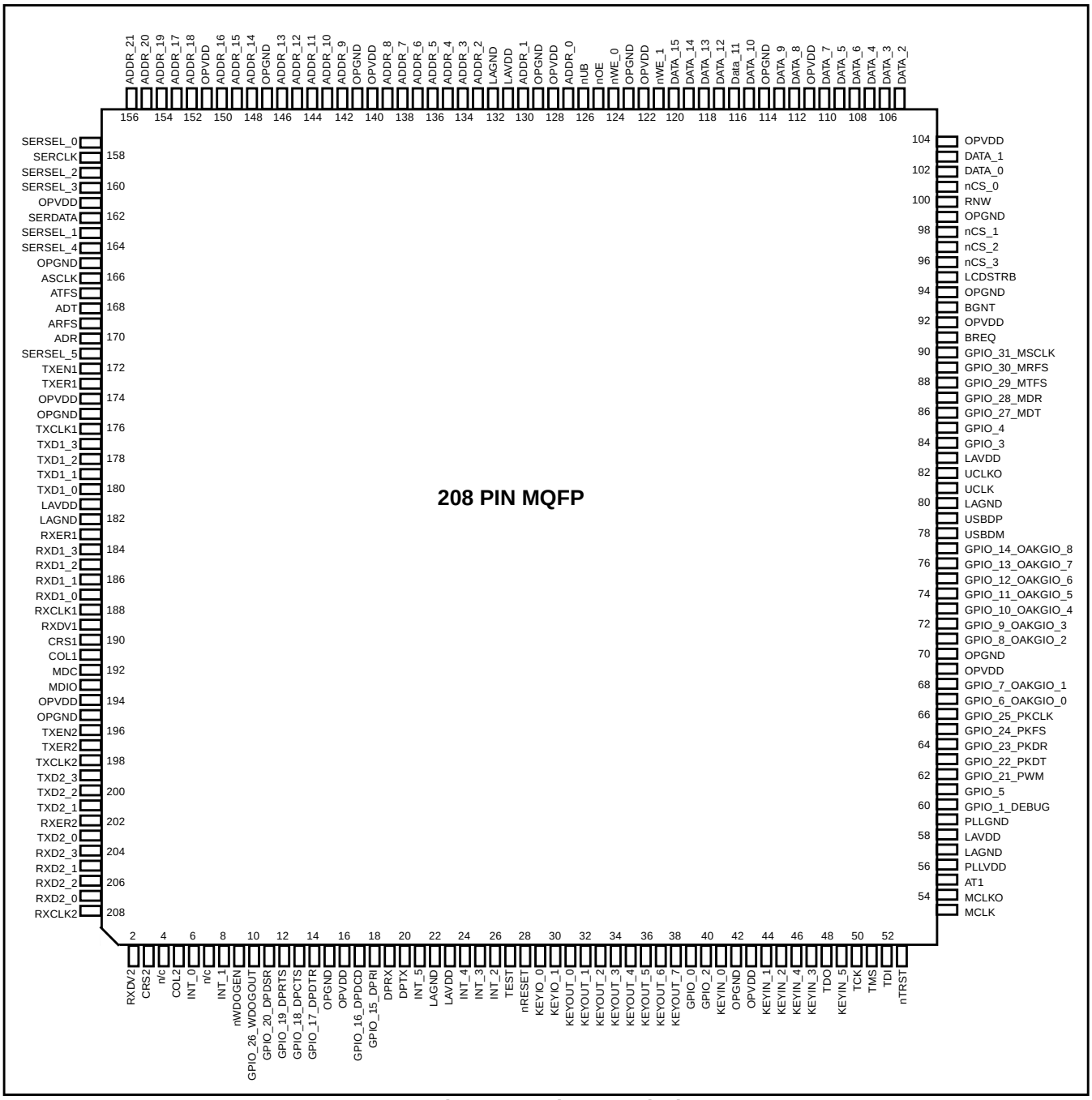
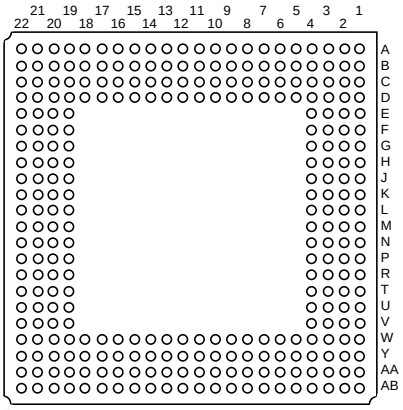


Figure 2 - Pin Description

288 PIN PBGA



Ball 288 pin PBGA	Pin Name
A2	RNW
A3	DATA_0
A4	nCS_1
A5	nCS_3
A6	BREQ
A7	GPIO_30_MRFS
A8	GPIO_28_MDR
A9	GPIO_3
A10	UCLK
A11	GPIO_14_OAKGIO_8
A12	GPIO_13_OAKGIO_7
A13	GPIO_11_OAKGIO_5
A14	GPIO_9_OAKGIO_3
A15	GPIO_7_OAKGIO_1
A16	GPIO_25_PKCLK
A17	GPIO_23_PKDR
A18	GPIO_21_PWM
A19	GPIO_5
A20	PLLGND
A21	AT1
A22	nTRST
B1	DATA_3
B3	DATA_1
B4	nCS_0
B5	nCS_2
B6	LCDSTRB
B7	GPIO_31_MSCLK
B8	GPIO_29_MTFS
B9	GPIO_4
B10	UCLKO
B11	USBDP
B12	GPIO_12_OAKGIO_6
B13	GPIO_10_OAKGIO_4
B14	GPIO_8_OAKGIO_2
B15	GPIO_6_OAKGIO_0
B16	GPIO_24_PKFS
B17	GPIO_22_PKDT
B18	GPIO_1_DEBUG
B19	LAGND
B20	PLLVDD
B21	MCLK
B22	TDI
C1	DATA_6

Ball 288 pin PBGA	Pin Name
C2	DATA_2
C4	OPVDD
C5	OPGND
C6	LAGND
C7	BGNT
C8	CA_8
C9	GPIO_27_MDT
C10	LAVDD
C11	USBDM
C12	CA_12
C13	CA_14
C14	DBGP
C15	IPROG
C16	nCDIRESETN
C17	OPGND
C18	LAVDD
C19	MCLKO
C20	LAVDD
C21	TMS
C22	TDO
D1	DATA_5
D2	DATA_4
D3	LAVDD
D4	OPGND
D5	LAVDD
D6	OPVDD
D7	OPVDD
D8	OPGND
D9	CA_9
D10	LAGND
D11	CA_10
D12	CA_11
D13	CA_13
D14	CA_15
D15	OPGND
D16	OPVDD
D17	BOOTP
D18	nABORTN
D19	OPVDD
D20	TIDDQ
D21	TCK
D22	KEYIN_3
E1	DATA_8
E2	DATA_7

Ball 288 pin PBGA	Pin Name
E3	CA_6
E4	OPGND
E19	OPVDD
E20	KEYIN_5
E21	KEYIN_4
E22	KEYIN_2
F1	DATA_10
F2	DATA_9
F3	OPVDD
F4	OPVDD
F19	BCLK
F20	LAGND
F21	KEYIN_1
F22	KEYIN_0
G1	DATA_12
G2	Data_11
G3	LAGND
G4	CA_5
G19	OPGND
G20	OPGND
G21	GPIO_2
G22	GPIO_0
H1	DATA_13
H2	DATA_14
H3	OPGND
H4	CA_4
H19	OPVDD
H20	KEYOUT_7
H21	KEYOUT_6
H22	KEYOUT_5
J1	nWE_1
J2	DATA_15
J3	CA_3
J4	OPVDD
J19	XDIAG_3
J20	KEYOUT_4
J21	KEYOUT_3
J22	KEYOUT_2
K1	nOE
K2	nWE_0
K3	OPGND
K4	CA_2
K19	XDIAG_1
K20	XDIAG_2
K21	KEYOUT_1
K22	KEYOUT_0
L1	ADDR_0
L2	nUB
L3	CA_1
L4	OPVDD
L19	OPGND
L20	KEYIO_1
L21	KEYIO_0
L22	nRESET
M1	ADDR_1
M2	ADDR_2
M3	LAVDD
M4	OPGND
M19	OPVDD
M20	XDIAG_0
M21	INT_2
M22	TEST
N1	ADDR_3
N2	ADDR_4
N3	CA_0
N4	LAGND
N19	CBUS_0
N20	LAVDD
N21	INT_4

Ball 288 pin PBGA	Pin Name
N22	INT_3
P1	ADDR_5
P2	ADDR_6
P3	nCDRN
P4	nCBRN
P19	LAGND
P20	DPRX
P21	DPTX
P22	INT_5
R1	ADDR_7
R2	ADDR_8
R3	OPVDD
R4	OPVDD
R19	CBUS_1
R20	OPVDD
R21	GPIO_16_DPDCD
R22	GPIO_15_DPRI
T1	ADDR_9
T2	ADDR_10
T3	nCDWN
T4	OPGND
T19	CBUS_2
T20	CBUS_3
T21	GPIO_18_DPCTS
T22	GPIO_17_DPDTR
U1	ADDR_11
U2	ADDR_12
U3	OPGND
U4	OPGND
U19	OPGND
U20	LAVDD
U21	GPIO_20_DPDSR
U22	GPIO_19_DPRTS
V1	ADDR_13
V2	ADDR_15
V3	OPVDD
V4	LAVDD
V19	CBUS_4
V20	INT_0
V21	nWDOGEN
V22	GPIO_26_WDOGOUT
W1	ADDR_14
W2	ADDR_18
W3	ADDR_20
W4	LAGND
W5	LAGND
W6	OPGND
W7	OPVDD
W8	OPGND
W9	nCPWN
W10	LAVDD
W11	CBUS_14
W12	CBUS_13
W13	OPGND
W14	CBUS_11
W15	CBUS_10
W16	CBUS_9
W17	OPGND
W18	CBUS_8
W19	CBUS_7
W20	CBUS_5
W21	COL2
W22	INT_1
Y1	ADDR_16
Y2	ADDR_17
Y3	LAVDD
Y4	nCPRN
Y5	OPVDD
Y6	OPGND

Ball 288 pin PBGA	Pin Name
Y7	OPVDD
Y8	SERSEL_5
Y9	TXCLK1
Y10	CBUS_15
Y11	LAGND
Y12	OPVDD
Y13	CBUS_12
Y14	COL1
Y15	OPVDD
Y16	TXD2_3
Y17	CBUS_6
Y18	LAVDD
Y19	LAGND
Y20	LAGND
Y21	n/c
Y22	n/c
AA1	ADDR_19
AA2	ADDR_21
AA3	SERSEL_2
AA4	SERSEL_3
AA5	SERSEL_4
AA6	ATFS
AA7	ARFS
AA8	TXEN1
AA9	TXD1_3
AA10	TXD1_1
AA11	RXER1
AA12	RXD1_1
AA13	RXCLK1
AA14	CRS1
AA15	MDIO
AA16	TXER2
AA17	TXD2_2
AA18	RXER2
AA19	RXD2_1
AA20	RXD2_0
AA21	RXCLK2
AA22	CRS2
AB1	SERSEL_0
AB2	SERCLK
AB3	SERDATA
AB4	SERSEL_1
AB5	ASCLK
AB6	ADT
AB7	ADR
AB8	TXER1
AB9	TXD1_2
AB10	TXD1_0
AB11	RXD1_3
AB12	RXD1_2
AB13	RXD1_0
AB14	RXDV1
AB15	MDC
AB16	TXEN2
AB17	TXCLK2
AB18	TXD2_1
AB19	TXD2_0
AB20	RXD2_3
AB21	RXD2_2
AB22	RXDV2

Figure 3 - Pin Description

Connection List

Function	Direct	Multiplexed	Pin Names
TDM AUDIO	5		ASCLK, ARFS, ATFS, ADR, ADT
CLOCK/PLL	5		MCLK, MCLKO, UCLK, UCLKO, AT1
MAC 1	18		TXD1[3:0], TXER1, TXEN1, TXCLK1, RXD1[3:0], RXER1, RXDV1, RXCLK1, COL1, CRS1, MDC, MDIO
MAC 2	16		RXCLK2, COL2, CRS2, TXD2[3:0], TXER2, TXEN2, TXCLK2, RXD2[3:0],RXER2, RXDV2

Connection List (continued)

Function	Direct	Multiplexed	Pin Names
EXT MEM INT	48		DATA[15:0], ADDR[21:0], NCS[3:0], LCDSTRB, NOE, NWE[1:0], RNW, NUB
TDM MASTER	0	{5}	{MSCLK, MRFS, MTFS, MDR, MDT}
WATCHDOG	1	{1}	WDOGEN, {WDOGOUT}
KEYPAD	16		KEYOUT [7:0], KEYIN[5:0], KEYIO[1:0]
GPIO	32		GPIO[13:0] directly, GPIO[31:14] via multiplex with other signals
PKM	0	{4}	{PKCLK, PKFS, PKDR, PKDT}
INTERRUPT	6		INT[5:0]
GP TIM	0	{1}	{PWM}
SSIO	8		SERCLK, SERDATA, SERSEL[5:0]
UART	2	{6}	DPRX, DPTX, {DPDSR, DPRTS, DPCTS, DPDTR, DPDCD, DPRI}
USB	2		USBDP, USBDM
JTAG/TEST/ DEBUG	6	{1}	TMS, TCK, TDI, TDO, NTRST, TEST, {DEBUG}
RESET	1		NRESET
EXTERNAL BUS MASTER	2		BREQ, BGNT
POWER	QFP:19 BGA:34		VDD, VIO
GROUND	QFP:19 BGA:34		GND
NC	2		NO CONNECTION
TOTAL	**208 Pins / 238 Balls**		

Note: A number of secondary signals are multiplexed with higher GPIO signals to allow some user flexibility.

The development version of the part provides the following pins in addition to those on the production part:

Function	Direct	Multiplexed	Pin Names
C-BUS INTERFACE	37		CBUS[15:0], CA[15:0], CPWN, CPRN, CDWN, CDRN, CBRN
OCEM CONFIG/ CONTROL	5		DBGP, BOOTP, IPROG, CDIRESETN, ABORTN
CPU DIAGNOSTICS	5		BCLK, XDIAG[3:0]
IDDQ TEST	1		TIDDQ
DEVELOPMENT TOTAL	**286 Balls**		

Overview

The CPU subsystem supports guaranteed operation at up to 25MHz and the DSP subsystem at up to 60MHz (60 MIPs) from a 3.3V power supply.

The device implements a flexible standard serial interface (TDM/Audio) to the external voice subsystem. The MT92101 is compatible with the Mitel MT92303 dual CODEC, but may also be used with most third party CODECs.

Multiple simultaneous full duplex voice channels can be supported. The number of channels is limited by the available DSP or CPU MIPs and is typically dependant upon the speech compression and echo cancellation algorithms selected. Fax transmissions may be relayed using a robust demodulation/ remodulation scheme.

The device has been fully optimised for low power operation. It uses low power cell libraries, supports software controlled low power modes for each subsystem and macrocell and fully implements local clock gating. The product is realised in three metal layer, small geometry, 0.35µm, CMOS technology. The next generation product, the MT92102, will be realised on very small geometry, four metal layer, 0.18µm CMOS technology.

Note: The term ‘Word’ is used to represent 16- and 32-bit numbers within this document. When used in the context of the DSP subsystem a Word is a 16-bit number. When used in the context of the CPU subsystem, a Word is a 32-bit number, with a 16-bit number being a half-Word.

CPU Subsystem

The ARM-Thumb CPU subsystem integrates the ARM7-Thumb CPU together with a range of peripherals chosen for this application. The Mitel BµILD architecture is used to provide a robust, standard bus interface between each peripheral block. Low power design techniques are used to save power wherever possible.

The subsystem comprises the following blocks:

- ARM-Thumb CPU,
- Synchronous Serial Interface,
- TDM Master Serial Interface,
- General Purpose Timer,
- Universal Asynchronous Receiver/Transmitter, UART,
- Quad Direct Memory Access Controller, (DMAC),
- USB Device Interface,
- 802.1 Ethernet Bridge and Dual MAC,
- DES Accelerator,
- 32-bit General Purpose Input/Output,
- Programmable Key Module Interface,
- Keypad Scanner,
- Interrupt Controller,
- Watchdog Timer,
- External Memory Interface,
- Memory Interface (or ARM-OAK Interface, AOI),
- Power Control,
- BµILD Broadcast Module,
- Boot ROM, 1024 Byte.

Simple external bus mastership is supported to allow sharing of all external memory/peripheral resources. On-chip resources are not available to external masters.

ARM7-Thumb CPU

The ARM7-Thumb CPU is a high performance, low power, 32-bit RISC processor core and include a hardware instruction decompressor to support 16-bit instruction half-Words. This core is based upon the proven ARM7 and retains its full 32-bit address, instruction and data Word widths. It contains a total of 37 registers and supports 6 operating modes. The core supports a fast response to interrupts (4 to 28 cycles) and all data processing instructions are fully conditional. Operation with 16-bit instruction widths is supported via a hardware decompressor operating with zero timing overhead (3-stage pipeline maintained). Code size in this mode is typically reduced to 65% of the requirement for full 32-bit instruction mode.

The core contains an ICEBreaker extension and JTAG interface to support non-intrusive debug. This JTAG interface also supports full boundary scan access.

In the MT92101, the ARM-Thumb may be clocked at up to 25MHz, although this is programmable (the MT92102 will be clocked at up to 40MHz). A low power sleep mode is supported.

Synchronous Serial Interface

The CPU subsystem has a Synchronous Serial Interface, which typically controls a variety of devices that employ a Synchronous Serial Interface. Examples are serial EEPROMS, NVRAM, LCD and

other display devices, CODEC and other voice circuits. The interface is fully flexible and provides:

- MICROWIRE™ Interface compatibility, to allow interfacing to memory and peripheral devices supporting this standard;
- Serial Peripheral Interface (SPI) compatibility, an interface found on certain Motorola, TI and ST microcontrollers;
- data transfer with either Byte or Word oriented protocols, with the Word width being configurable from 2 to 32 bits;
- triple buffered Transmit and Receive Channels;
- operation in either Interrupt or Polled mode;
- support for up to 6 slave devices (i.e., 6 enable signals, 1 clock and 1 bi-directional data);
- fly-by support for single addressed DMA transfers.

TDM Master Serial Interface

The TDM Master Serial Interface included in the CPU subsystem is provided for use in tele-worker or non-IP applications, where it becomes the main system interface for voice data. The interface is substantially the same as the TDM Audio interface within the DSP subsystem, and is a fully flexible multi-channel PCM based interface that provides:

- a five pin interface (1 clock, RX and TX frame syncs, input data and output data); frame syncs and clock support programmable direction and polarity;
- single or multi-channel capability; the multichannel facility allows time division multiplexing of the serial bitstream into up to 32 channels. Any number of these channels can be used for transmit or receive independently. The CPU must supply data for the transmit channels in the correct order and sort data from the receive channel.
- compatibility with Mitel ST-Bus and most PCM busses;
- transmit and receive sections can operate with DMA from/to memory to reduce CPU interaction;
- inclusion of a compander circuit to support A-law and μ-law interfaces; when enabled, the companding operation is transparent to the CPU. The compander may also be accessed independantly by the CPU to allow separate compression and expansion operations, in parallel with companded or non-companded serial IO.

General Purpose Timer

The CPU subsystem has a flexible general purpose timer that may be used for timing multiple events. Two identical independent timer/counter elements are provided; each contains the following:

- a 12-bit, variable prescaler generating the counter clock;
- a 32-bit fully programmable up/down timer/ counter;
- multiple counter modes including free running, halt-on-zero/overflow;
- four 32-bit compare registers;
- flexible interrupt generation from the timer and/ or compare registers;
- PWM signal output option using main counter and compare register 1.

Universal Asynchronous Rx/Tx, UART

A Universal Asynchronous Receiver Transmitter (UART) is included in the CPU subsystem, providing industry standard levels of support for full-duplex asynchronous serial communications. It is typically used for communication with a PC for configuration or test purposes, but may also be used to implement an IRDA port. Features of the UART include:

- full duplex operation, independent transmit and receive channels;
- software configurable as either a DTE or DCE;
- fully programmable baud rate selection derived from subsystem clock; all standard baud rates up to and including 153.6 and 230.4 kbit/s are supported within acceptable margins;
- theoretical limit for the interface of one half of the subsystem clock frequency;
- automatic baud rate and character format detection for received data;
- automated support of Hardware (RS-232C and RS-232E) and Software Flow Control;
- input filters for serial input data and modem control inputs;
- data formatting for 7 or 8 bit serial character, 1 or 2 stop bits, and even, odd, mark, space or no parity;
- line break detection/generation;
- framing, overrun and parity errors, with interrupt generation;
- fly-by support for single addressed DMA transfers.

Quad Direct Memory Access Controller, DMAC

The DMA Controllers allow data to be moved around the subsystem with little CPU intervention. Each of the 4 controllers contains a pair of sub-controllers, each capable of managing a single addressed (fly-by) DMA transfer between memory and an implicitly addressed device, such as the UART. Alternatively, a pair of sub-controllers may be used to perform dual addressed transfers, where both source and destination require address generation. A typical application might allocate 4 sub-controllers to support the Ethernet Bridge, leaving 2 controllers (or 4 sub-controllers) to support the UART, SSIO and any memory to memory transfers. Each controller supports the following:

- transfer rates at up to 4 bytes per clock cycle, single addressed, 2 bytes per cycle, dual addressed;
- transfer counts up to 64k items;
- block and packet transfer modes;
- chained transfers to support scatter-gather operations;
- hardware or software triggered transfers.

USB Device Interface

A standard USB interface for connection to a PC or similar host is included, and has the following features:

- supports 8 programmable end points;
- has a 16-byte FIFO buffer per end point.

802.1 Ethernet Bridge and Dual MAC

The 802.1 Ethernet Bridge and Dual MAC allows connection of a desktop workstation (PC) to a LAN through the IP telephone; one port connects to the LAN, the other to the workstation. Using dual ports in this way avoids the need for a dedicated LAN port for the telephone and also reduces cable bulk.

The MAC ports support 10Base-T and 100Base-TX Ethernet formats and have standard MII interfaces to external PHYs. FIFO buffers are inserted in transmit and receive paths between each MAC and the switch. Input buffers are 3328 bytes deep to allow at least 2 full packets to be accommodated, output buffers are 1536 bytes deep, accommodating at least 1 full packet. The switch allows packet injection and packet extraction for communication with the phone.

A watchdog counter allows the splitting of packet transfers through the switch to avoid problems with CPU/bus sharing.

DES Accelerator

The DES Accelerator is a hardware accelerator for execution of the Data Encryption Standard (DES) algorithm as defined in FIPS PUB 46-1, which is equivalent to the Data Encryption Algorithm (DEA) provided in ANSI x3.92-1981. Standard DES is executed in just 16 clock cycles; cipher block chaining (CBC) is supported and related DES algorithms such as triple-DES and DES-X are also supported.

32-bit General Purpose Input/Output

The General Purpose I/O is a set of up to 32 signals that may be individually written to or read by the CPU for general purpose control. Each signal is programmable for direction (input or output) and pull-resistors may be selectively disabled. Nine of these signals may be configured such that they are controlled directly from the DSP. Most General Purpose I/O (GPIO) pins have internal pull-resistors to either VIO or GND, split roughly equally; a few GPIO pins have no pull-resistors. Therefore, individual GPIO signals may be selected in order to minimize static current consumption in the application, based upon the known external conditions.

A number of the GPIO signals are multiplexed with other functions in order to reduce pincount. Multiplexing is controlled from the CPU and a minimum of 14 GPIO signals are always available.

Programmable Key Module Interface

The Programmable Key Module Interface is a simple serial interface intended to support a specialized KEY and LED expansion port, which is required in some systems. The features include the following:

- a 4-wire interface: output clock, output frame marker, output data and input data;
- ability to send 16 bytes of control and receive 16 bytes of status information per frame;
- a programmable clock divider from subsystem clock, to facilitate low frequency operation (typically 3kHz).

Because the PKM interface signals are mulitplexed with GPIO pins and the interface may be powered down, it may be disabled in systems where it is not required.

Keypad Scanner

The flexible keypad interface supports keypad configurations of up to 8x8 keys (e.g., 10x6, 9x7,

8x8). There are 8 row outputs, 6 column inputs and 2 programmable row/column IOs. Keypad scanning involves reading the input register and interpreting it based on the driven output state. Interrupts may be masked on a per input basis. Key debounce, if required, must be handled in software.

Interrupt Controller

The Interrupt Controller block manages all internally generated CPU subsystem interrupts, plus 6 external interrupts. It translates interrupts into regular IRQs and fast, higher priority FIQs for the ARM-Thumb CPU. A hardware priority scheme is used to minimize interrupt latency. Each interrupt source may be individually configured for the following:

- polarity, active high or low;
- enabled or disabled;
- edge or level sensitivity;
- interrupt type, IRQ or FIQ.

Watchdog Timer

The watchdog timer ensures that system lock-up does not occur due to hardware or run-time software errors. It is driven from the CPU subsystem clock and contains a 32-bit primary counter and an 8-bit secondary counter with prescaler. These counters are user programmable, allowing control of the watchdog CPU interrupt rate and of the time duration in which this interrupt must be cleared. Any lock-up situation would be cleared via a system reset generated on time-out of the secondary counter.

The timer may be disabled for debug or similar reasons via a control pin. An output is provided for power-down or disabling of external functions during watchdog time-out.

External Memory Interface

The External Memory Interface is the interface between the on-chip BµILD bus and any external memory and peripherals. It performs byte and half-Word packing and sub-bus width writes to allow any on-chip bus master to access 8- or 16-bit external components. The external interface consists of 16 data pins, 22 address pins, 5 select pins, and 4 control/enable signals. It can address up to 4 Mbytes of memory in 5 separate areas. Each area may be independently configured for memory/peripheral type and number of start/access/stop wait states (0 to 15). One area is dedicated to LCD control and therefore, generates a strobe signal in place of the normal chip select. Zero wait state operation at the maximum specified operating frequency is supported for devices having a 10nS access time or better.

Memory Interface (AOI - ARM-OAK Interface)

The Memory Interface allows the DSP to access the CPU's memory map, including all off-chip memory. A fixed 16 kWord window in the DSP's data memory map may be mapped to any position within the CPU's memory map via a programmable BASE ADDRESS. This window is termed 'shared memory'. Two separate BASE ADDRESS registers, one accessible from the CPU and one from the DSP, are implemented. The BASE ADDRESS is defined by the contents of one of these registers, with selection being controlled by the CPU.

In order to minimize latency, by default the Memory Interface is the highest priority master on the BµILD bus. However, the relative priorities of the Memory Interface and each of the 2 DMA Controllers may be fully software configured via the System Configuration Register.

Three modes of operation are supported for data transfer across the AOI. The simplest mode, suitable for limited data transfers at slow speed only, generates wait states to the DSP during transfers. As the DSP is typically operating faster than the CPU this results in significant lost time to the DSP.

The second mode, READ AHEAD, stores the current accessed address in a local register and returns data from the previous access. The new data is then read from memory and stored in the Memory Interface ready for the next READ AHEAD cycle. This mechanism avoids any DSP waits, at the expense of a single sample latency, and is not suitable for transferring large blocks of data.

The third mode, DMA, allows fast transfer and would be the mechanism chosen for transferring larger blocks of data. Blocks of data up to the full 16 kWord shared memory area may be transferred with no CPU or DSP intervention once the transfer is initiated. A DSP interrupt is generated when the transfer is complete.

Inter-processor communication through the AOI uses a pair of registers: the CPU status register (writable by the CPU only, readable by both processors) and the DSP status register (writable by the DSP only, readable by both processors). Each contains an interrupt bit, 3 associated interrupt type bits, a ready bit and 4 additional general purpose bits that may be used to implement a polling mechanism.

The AOI transfers data between the asynchronous clock domains of the 2 processors. Its implementation relies upon the DSP being clocked at

twice the rate of the CPU (or greater) to guarantee correct operation.

Power Control

The Power Control block allows selection of power states (enabled or disabled) for each CPU subsystem peripheral during STANDBY and RUN power modes. All CPU subsystem peripherals may be powered down in this way, although some core activity remains in the key blocks (External Memory Interface, BµILD Broadcast Module, Watchdog Timer, and within this block). The Power Control block also contains a control bit to allow selection of STANDBY mode.

BµILD Broadcast Module

The BµILD Broadcast Module block performs a number of functions essential to operation of the **B**us for µController **I**ntegration in **L**ow-power **D**esigns (BµILD).

- bus master arbitration,
- control of bus modes,
- hardware system debug support and diagnostic generation,
- stores system configuration data,
- handshaking to allow external bus masterhip.

System configuration data includes clock selection, PLL programming, bus master prioritization and DMA assignment.

External bus masters are supported via a simple two-pin handshaking mechanism. Upon granting external bus mastership, all the external memory interface pins (address, data, chip select and enables) are tri-stated. The external bus master may then access any external memory or other peripheral devices. However, the interface does not support external bus master accesses of on-chip memory or peripherals.

Boot ROM

Application boot normally runs directly from external ROM/FLASH at location 0x00000000. Alternatively, if pin GPIO[0] is held low on exit from system reset, boot occurs from the internal boot ROM (FLASH Load Mode). The internal ROM contains a simple algorithm to allow download and execution of a user-defined program directly from the UART. Typically during a FLASH Load, this program will download full application code via the UART and program it into the on-board FLASH ROM during end product manufacture or field re-program. Alternatively, in situations where full debug tools are not appropriate, test software could be downloaded.

CPU Memory Map

Address space is split into 8 equal segments, decoded from the top 3 address lines. The bottom 6 segments form the main memory areas for the internal Boot ROM and the 5 external memory areas. The next segment is reserved and the final area is used for all internal memory mapped registers. This final segment is further subdivided into sub-segments, each of 1024 Words, with all memory-mapped blocks being allocated one sub-segment.

Reserved, Test Access Only	0xE0030000→ 0xE03FFFF
Ethernet MAC 2	0xE002 E000 → EFFF
Ethernet MAC 1	0xE002 D000 → DFFF
802.1 Ethernet Bridge	0xE002 C000 → CFFF
USB Device Interface	0xE002 A000 → AFFF
Programmable Key Module	0xE002 9000 → 9FFF
Synchronous Serial Interface	0xE002 7000 → 7FFF
General Purpose Timer	0xE002 6000 → 6FFF
Keypad Scanner	0xE002 5000 → 5FFF
General Purpose IO	0xE002 4000 → 4FFF
Memory Interface (AOI)	0xE002 0000 → 0FFF
TDM Master SIO	0xE001 C000 → CFFF
UART	0xE001 8000 → 8FFF
DMAC 2	0xE000 D000 → DFFF
DMAC 1	0xE000 C000 → CFFF
External Memory Interface	0xE000 8000 → 8FFF
Interrupt Controller	0xE000 6000 → 6FFF
Power Control	0xE000 5000 → 5FFF
Watchdog Timer	0xE000 4000 → 4FFF
BuILD Broadcast Module	0xE000 2000 → 2FFF
Reserved, Test Access Only	0xE000 0000 → 0FFF

Table 1. CPU Subsystem Memory Mapped Registers

Further details of this allocation and of all register bits are described in a separate publication, MT92101 IP Phone Processor Handbook, DM5252.

Each main memory area may address up to 512 Mbytes (ADDR[28:0]). However, this is limited to just 4Mbytes (ADDR[21:0]), due to the number of address pins available on the MT92101. Any attempt to access memory outside of this range will access copied images of the 4Mbyte areas.

The lower 3 external memory areas are nominally allocated to ROM (External Mem 1), RAM (External Mem 2) and EEPROM (External Mem 3). The top external memory area is dedicated to an LCD controller. The positions of Internal Boot ROM and External Mem 1 (ROM) or of Internal Boot ROM and External Mem 2 (RAM) may be swapped under software control via the System Configuration Register. Alternatively, the positions of Internal Boot ROM and External Mem 1 (ROM) will be swapped if pin GPIO[0] is held high during device reset. These features allow the CPU to boot from internal ROM or from external ROM, or to execute code resident in RAM in a flexible manner. Apart from these limitations, each external memory area may used to map any type of memory or peripheral.

Reserved	0xFFFFFFFF 0xE0400000
Mem Map Registers	0xE03FFFFF 0xE0000000
	0xDFFFFFFF 0xC0400000
Reserved	0xC03FFFFF 0xC0000000
	0xBFFFFFFF 0xA0400000
External Mem 5 (LCD)	0xA03FFFFF 0xA0000000
	0x9FFFFFFF 0x80400000
External Mem 4 (Spare)	0x803FFFFF 0x80000000
	0x7FFFFFFF 0x60400000
External Mem 3 (EEPROM)	0x603FFFFF 0x60000000
	0x5FFFFFFF 0x40400000
External Mem 2 (RAM)	0x403FFFFF 0x40000000
	0x3FFFFFFF 0x20400000
External Mem 1 (ROM)	0x203FFFFF 0x20000000
	0x1FFFFFFF 0x00000400
Internal Boot ROM	0x000003FF 0x00000000

Table 2. CPU Subsystem Memory Map

CPU Power Modes

The CPU subsystem supports 2 main operating modes: normal operating (or RUN mode) and low power (or STANDBY mode). The power state of each block within the CPU subsystem may be programmed individually in both modes. STANDBY mode is entered via software control, with exit to RUN mode occurring via an interrupt or system reset only.

An alternative power saving mechanism may be used when the CPU is not required, but when other bus masters (Memory Interface and DMAC) may require access to the bus. This mechanism is known as SLEEP mode and utilizes a coprocessor instruction to fully suspend the ARM-Thumb, with wake-up into RUN mode again occurring via an interrupt or system reset.

DSP Subsystem

The DSP subsystem integrates the OAKDSPCore™ with a range of peripherals and memory to support all physical layer processing. A dual phase clocking scheme is used to maximize performance while maintaining a low power solution. The subsystem comprises the following blocks:

- OAKDSPCore™,
- OCEM,
- Memory Interface (AOI),
- C-bus Interface (to support full debug),
- TDM Audio Serial Interface,
- Acoustic Echo Canceller (via firmware upgrade),
- Direct Memory Access Controller, DMAC,
- Interrupt Controller,
- Bus Interface Unit (BIU),
- Clock Generation (ACLK and CLKGEN),
- Data RAM, 7 kWord,
- Data ROM, 8 kWord,
- Program ROM, 60 kWord,
- Program RAM, 4 kWord.

OAKDSPCore™

The OAKDSPCore™ is a high performance, 16-bit fixed point DSP core. It contains a 36-bit ALU, plus four 36-bit accumulators, and includes a bit manipulation unit containing a 36-bit left/right barrel shift. The core utilizes a software stack.

In the MT92101, the OAK is clocked at 60 MHz to provide a maximum of 60 DSP MIPS, although this is programmable. In the MT92102, the OAK will be clocked at 90MHz. The core has low power sleep modes.

OCEM

Debug is supported via an **O**n-**C**hip **EM**ulation circuit (OCEM), accessed via the external parallel C-bus or via the CPU JTAG port and the Memory Interface. Five device pins are required for selection and control of the various emulation boot modes, and are only provided on the development pinned device.

Note: DSP debug access through the JTAG port and Memory Interface is currently limited.

Memory Interface (AOI, or ARM-OAK Interface)

The AOI is the primary link between the CPU and DSP subsystems and is described in the CPU subsystem part of this datasheet (see page 8).

C-bus Interface

The C-bus interface is required to support full DSP debug and is a 37-pin parallel interface giving access to the combined (multiplexed) DSP data and program busses. The C-bus interface is only available on the development pinned device.

TDM Audio Serial Interface

The TDM Audio Serial Interface is used for transferring audio data to one or more voice CODECs or similar devices. The interface is substantially identical to the TDM Master interface within the CPU subsystem and is a fully flexible multi-channel PCM based interface, which provides the following:

- a five pin interface (1 clock, RX and TX frame syncs, input data and output data);
- frame syncs and clock support programmable direction and polarity;
- single or multi-channel capability, allowing time division multiplexing of the serial bitstream into up to 32 channels; any number of these channels can be used for transmit or receive independently; the DSP must supply data for the transmit channels in the correct order, and sort data from the receive channel;
- compatible with Mitel ST-Bus and most PCM busses;
- transmit and receive sections can operate with DMA from/to memory to reduce DSP interaction; the DMA controller can be programmed with the number of Words to transmit or receive (up to 8192 Words each) and generates an interrupt when complete;
- a compander circuit is included to support A-law and μ-law interfaces. When enabled the companding operation is transparent to the DSP. The compander may also be accessed independently by the DSP to allow separate compression and expansion operations, in parallel with companded or non-companded serial IO.

Acoustic Echo Canceller (AEC)

The AEC is achieved through a firmware upgrade and is a half-duplex DSP firmware solution. It operates in conjunction with the TDM Audio Serial Interface to cancel acoustic echo on a single, programmable, audio channel.

Direct Memory Access Controller (DMAC)

The DMAC operates in conjunction with the TDM Audio Interface and the AOI to allow data to be transferred to or from the external voice CODECs and DSP data memory, and to or from the CPU subsystem (usually shared external memory) and DSP data memory with no DSP intervention. The hardware associated with this function is located in the Bus Interface Unit and in the AOI.

Interrupt Controller

The Interrupt Controller block manages all internally generated DSP subsystem interrupts, plus 2 external interrupts (sharing INT[5:4] pins with CPU interrupts). The controller translates these to one of three interrupt priority levels to the OAKDSPCore™ in a fully programmable way. Inputs are edge sensitive.

Bus Interface Unit

The Bus Interface Unit (BIU) controls all access to the on-chip DSP data and program busses. It produces the C-bus and contains the DSP GPIO and DMA circuitry. It allows individual selection of external C-bus program, data, mailbox and monitor program wait states. Power control for data memories and peripherals is also managed from this block.

DSP Memory Map

The DSP data space contains 7kWords of RAM (2-kWord on-core XRAM, 2-kWord on-core YRAM and 3-kWord off-core XRAM) plus 8-kWords ROM for storage of data tables and filter coefficients. Another 16-kWords is allocated to shared memory, 1-kWords to an external emulation mailbox, 1-kWords to external file IO and 4-kWords to memory mapped registers. A 16-kWord window is available for external C-bus access to support development. Each memory-mapped block is assigned its own 256-Word window.

The DSP program space contains 59-kWords of application ROM plus 4-kWords of RAM to support program patches and customisation. The remaining 1kWord is reserved for an external monitor program to support emulation and debug. This program memroy map is mirrored internally to allow an internal monitor program to support enhanced debug via the Memory Interface and JTAG port in the future. All of this space, with the exception of boot code, may be mapped to the C-bus for external development use.

On-core YRAM (2k)	0xFFFF 0xF800	
OCEM Mem Map Registers (16w)	0xF7FF 0xF7F0	
Reserved (2k-16w)	0xF7EF 0xF000	
External Memory (16k)	0xEFFF 0xB000	
Reserved	0xAFFF 0xA7E0	*Mapped: Off-chip*
Mailbox (992w)	0xA7DF 0xA400	
File IO (1k)	0xA3FF 0xA000	
Data ROM (8k)	0x9FFF 0x8000	
Shared Memory (16k)	0x7FFF 0x4000	
Reserved (4k)	0x3FFF 0x3000	
Mem Map Registers (4k)	0x2FFF 0x2000	
Reserved (3k)	0x1FFF 0x1400	
Off-core XRAM (3k)	0x13FF 0x0800	
On-core XRAM (2k)	0x07FF 0x0000	

Table 3. DSP Subsystem Data Memory Map

Attempted access to internal program ROM (0x0000 to 0xEFFF) via a `movp` instruction will be detected and blocked by a program protection mechanism, to prevent unauthorised copying of embedded firmware.

BIU Boot (2w)	0xFFFF 0xFFFE	
Application/Patch RAM (4k–2w)	0xFFFD 0xF000	*On Chip*
Monitor (1k)	0xEFFF 0xEC00	*On or Off Chip*
Boot Code (64w)	0xEBFF 0xEBC0	*On Chip*
Application ROM (59k – 96w)	0xEBBF 0x0020	*On or Off-chip* *IPROG = 1 or 0*
Interrupt Vectors (32w)	0x001F 0x0000	

Table 4. DSP Subsystem Program Memory Map

All ROM may be programmed during wafer metalisation to allow fast generation of code updates and variants.

DSP Power Modes

The DSP subsystem supports three operating modes: normal operation (or ACTIVE mode), low power IDLE mode, and lowest power STOP mode. The DSP is powered down in both IDLE and STOP modes. In IDLE mode, the PLL remains active to allow a fast switch to ACTIVE mode. In STOP mode, the PLL is fully powered down and therefore, a time delay is necessary to allow the PLL to lock and settle. This time delay is automatically generated and will be nominally 200µs for a 40MHz master clock, and proportionately longer for a slower clock.

Exit from IDLE mode is normally made via an interrupt, although it may also occur via a system reset, a soft DSP subsystem reset, or a CDI reset.

Exit from STOP mode normally is achieved under control of the CPU via an OAK CONTINUE signal, generated by the AOI. Alternatively, an external interrupt, a system reset, a soft DSP subsystem reset, or CDI reset may be used. Exit from STOP mode is directly to ACTIVE mode. The OAK CONTINUE signal ensures that the DSP recommences operation in exactly the same state from which it entered STOP mode (i.e., all register states are maintained).

Clock Provision and PLL Clock Generation

The number of externally provided clocks is minimised, while offering sufficient flexibility to cover all possible applications. Two external, dedicated clock sources are required:

- Master Clock (MCLK)
- USB Clock (UCLK), fixed at 48.000 MHz

MCLK provides the CPU Subsystem clock directly and the TDM Clock via simple division. Two modes of operation are possible as described below:

a) Internal TDM Clock
The master clock is limited to an integer multiple of the required TDM clock frequency. The TDM clocks are generated by dividing MCLK; the ratio is programmable by the CPU (for the TDM Master Interface) or the DSP (for the TDM Audio Interface).

b) External TDM Clock
The master clock may be any frequency up to 40MHz. TDM clocks are input to the serial interface clock pins.

Each USB clock may be driven from an off-chip logic level source, or may be generated via an on-chip crystal oscillator (i.e., requiring 2 pins per clock, 4 pins in total). MCLK must be active at all times to allow the CPU to wake from STANDBY mode, although UCLK may be externally disabled when the USB is not being used, and when it is not selected as the PLL clock source.

MCLK is typically used directly by the CPU subsystem, but may be divided to lower power consumption; division ratios of 2, 4, 8 and 16 are supported.

The DSP subsystem clock is generated from MCLK or UCLK via a fully embedded programmable PLL (n*0.25*CLK, up to 90MHz). It is generated through a programmable divide by 1 / 2 / 4, followed by a fully programmable PLL giving integer multiplication. A further programmable divide by 1 / 2 stage after the PLL allows further flexibility. Clock source selection for the PLL is programmable by the CPU, although the default is to MCLK. Changes to this clock source may only be made while the DSP subsystem is in STOP mode. When active, the DSP clock must always operate at least twice as fast as the CPU clock to allow correct operation of the AOI block. See Figure 3 for an illustration.

The reset pin, nRESET, utilises a power-on-reset cell, which may be used as the source of a reset for other devices. A single external component (a capacitor) is required to provide the appropriate time constant.

Embedded DSP Firmware

The OAK subsystem has embedded full physical layer firmware, including multi-channel voice compression, acoustic functions and a host interface. Multiple simultaneous voice channels can be supported, up to the 90 DSP MIP limit, dependent upon voice compression and audio echo cancellation requirements.

Acoustic functions supported include DTMF/call progress tone generation, acoustic echo cancellation, volume control and sidetone generation.

The host interface provides a communications link between the DSP subsystem and the controlling CPU. All information passed between the two processors is processed by this module.

All firmware modules are run within a simple RTOS that handles all scheduling and prioritising of tasks and maximises usage of available DSP MIPS. All firmware modules have been extensively verified using a combination of software simulation and hardware emulation.

Firmware Feature List

The following features are supported in firmware:

- G.729.AB compression;
- G.723.1A compression;

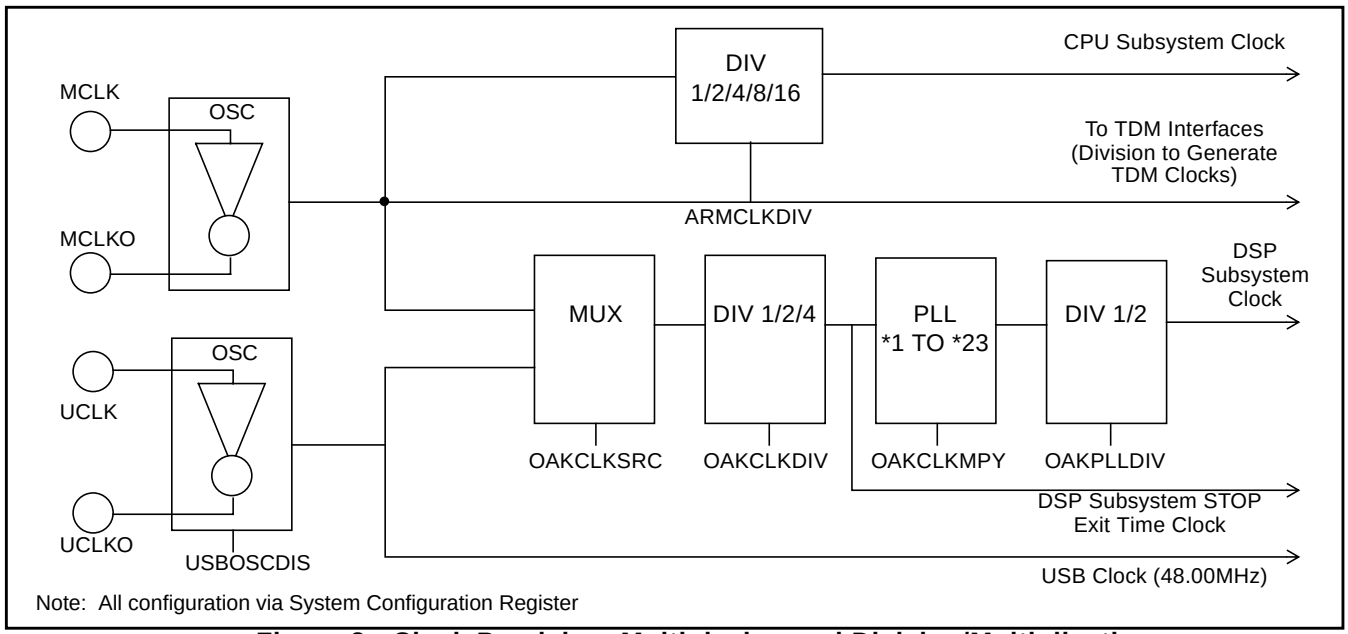


Figure 3 - Clock Provision, Multiplexing and Division/Multiplication

Master Clock MCLK	USB Clock UCLK	CPU Subsystem Clock	DSP Subsystem Clock	TDM Clock
10 MHz	48 MHz	10 MHz (MCLK)	56.25 MHz (9 * ECLK / 4)	1 MHz (MCLK / 10)
24.576	48	24.576 (MCLK)	60MHz (6 * MCLK)	2.048 (MCLK / 12)
40.96	48	40.96 (MCLK)	81.92 (2 * MCLK)	4.096 (MCLK / 10)
40	48	2.5 (MCLK / 16)	STOP	External - Inactive

Table 5 - Example Clock Configurations

- VAD / CNG;
- audio echo suppression;
- DTMF / call progress tone detection and generation;
- sidetone and loopback;
- caller ID in-band signalling generation;
- adaptive playout;
- signal classifier;
- executive/RTOS.

CPU Software

Full software is provided for demonstration purposes and as the basis for a full system. The H.323, SIP and MGCP/MEGACO protocol stacks, if required, are available only as object code and have an associated per-use license cost.

All software modules have been verified and are believed to support full interoperability with existing equipment. However, full independent verification/ approval of this software has not yet been achieved.

Software Feature List

The following features are available as software modules:

- protocol stacks: H.323, SIP and MGCP/ MEGACO;
- RTP/RTCP transport layer;
- interface API to the DSP subsystem;
- reference phone application, including a basic MMI;
- BSP and hardware drivers associated with all of the above;
- standard RTOS support for Precise/MQX from Precise Software Technologies Inc.

Alternative operating systems may also be supported, dependant upon customer requirements. Possibilities include pSOS from Integrated Systems Inc., Nucleus from Accelerated Technology Inc., and VxWorks from Wind River Systems.

Technology and Packaging

The MT92101 is realised in our well proven 0.35µm triple layer metal CMOS technology, for earliest availability of prototypes at minimum risk. This part supports audio echo cancellation only as a firmware upgrade to the DSP, and operates at maximum clock speeds of 25MHz for the CPU subsystem and 60MHz (MIPs) for the DSP subsystem. DSP access to external memory over the C-bus can reach 40MHz, dependant upon memory speed. It is available in 208 pin TQFP, 28 x 28 x 1.4 mm, 0.5mm pitch, or in 288 ball (238 used ball) PBGA, 23 x 23 x 1.2mm, 1mm pitch, package options.

A further package option is supported for development devices only. These development devices use all connections on the above PBGA package to provide access to the DSP combined program and data buses (C-bus), to allow full DSP debug and operation with external DSP memory.

Next Generation Realisation on 0.18µm Technology, MT92102

The MT92102 will be realised in a very small geometry, 0.18µm, quad layer metal CMOS technology for lowest cost and power consumption and supports all features and parametric performance outlined here. Additionally, the MT92102 will support fully audio echo cancellation, and will operate at greater maximum clock speeds.

The MT92102 will be fully pin compatible with the MT92101, although it will be necessary to supply two power supply voltages. The development device for the MT92102 will have the ability to use external program memory - zero-wait at up to about 50MHz, dependant upon memory speed, is included.

Development Support

The MT92101 is supported with a development/ evaluation kit which includes two evaluation boards and a comprehensive suite of software APIs, development tools and PC-based exercisers to allow the rapid development of IP phone applications, SOHO gateways and similar applications. The kit will also support the MT92102. The boards support full CPU debug access and basic DSP debug access via a JTAG interface. Full DSP debug access may be provided optionally via a C-bus interface.

H.323 Development Toolkit

An optional add-on software toolkit is available to provide a full complement of H.323, including H.235 and H.450 extensions.

MGCP/MEGACO and SIP

Development toolkits for SIP and MGCP/MEGACO will be available shortly.

Absolute Maximum Ratings* - Voltages are with respect to ground (GND) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Any VDD Pin to any GND Pin		- 0.3	2.5	V
2	Any Signal Pin to GND		- 0.3	VDD + 0.5	V
3	Storage Temperature Range		- 55	125	˚C
4	ESD		2	2	kV

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

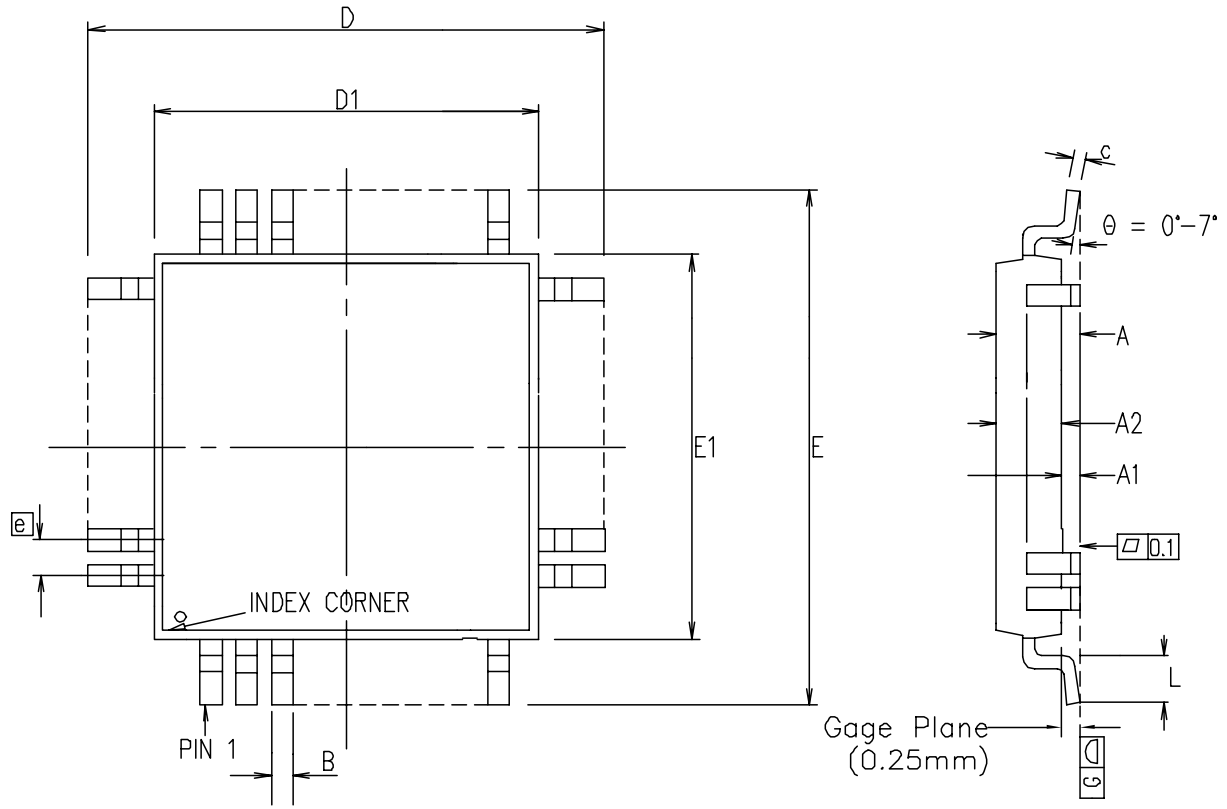
	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Operating voltage range[a]	VDD	3.0	3.3	3.6	V	Chip core power supply
2	Operating temperature range	OT	-40		+85	˚C	
3	Input high voltage	VIH	0.7*VDD			V	
4	Input low voltage	VIL			0.3*VDD	V	
5	Input pull-up/down current	IIPU/IIPD		33	90	µA	0 < VIN < 3.6
6	Input current	II			5	µA	0 < VIN < 3.6 All other inputs
7	Input capacitance	CIN			10	pF	All inputs and IO's
8	Output high voltage	VOH	0.8*VDD			V	|IOUT|=100 uA (microA)
9	Output low voltage	VOL			0.4*VDD	V	|IOUT|=100 uA (microA)
10	Three-state leakage current	IO			10	µA	All outputs and IO's
11	Output capacitance	COUT			40	pF	Total external load, all outputs and IO's

a. MT92102 will have an additional 1.8V nominal power supply.

Electrical Characteristics†

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Clock input frequency	MCLK			25	MHz	CPU subsystem frequency
2	Clock input frequency	UCLK		48	60	MHz	Unity input ratio
3	Clock input ratio	MCLK	45:55		55:45	%	Digital input 25 MHz
4	Clock input ratio	UCLK	40:60		60:40	%	Digital input 48 MHz
5	Crystal load capacitance			12	30	pF	MCLK and UCLK
6	Crystal start time			400		mS	MCLK and UCLK
Power Consumption							
7	MCLK = 25 MHz UCLK disabled			0.8		mA	CPU Subsystem STANDBY DSP Subsystem STOP
8	MCLK = 25 MHz , DSP Subsystem clock = 60MHz			4		mA	CPU Subsystem STANDBY DSP Subsystem IDLE
9	CPU Subsystem			0.5		mA per MHz	CPU Subsystem RUN DSP Subsystem STOP
10	DSP Subsystem			1.0		mA per MIP	CPU Subsystem STANDBY DSP Subsystem ACTIVE

†Electrical Characteristics are over Recommended Operating Conditions unless otherwise stated.
‡Typical figures are at 25°C with nominal VDD + VIO and are for design aid only.



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	---	1.60		---	0.063
A1	0.05	0.15		0.002	0.006
A2	1.35	1.45		0.053	0.057
D	30.00 BSC			1.181 BSC	
D1	28.00 BSC			1.102 BSC	
E	30.00 BSC			1.181 BSC	
E1	28.00 BSC			1.102 BSC	
L	0.45	0.75		0.018	0.030
e	0.50 BSC			0.020 BSC	
b	0.17	0.27		0.007	0.011
c	0.09	0.20		0.004	0.008
	Pin features				
N	208				
ND	52				
NE	52				
NOTE	SQUARE				

Conforms to JEDEC MS-026 BJB Iss. C

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar protusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

ORIGINATING SITE: SWINDON

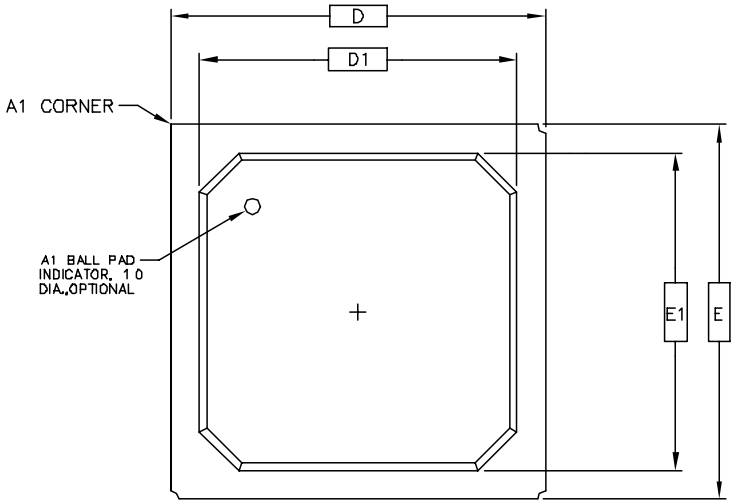
ISSUE	1	2			
ACN	200998	207155			
DATE	17.JUL.96	16JUL99			
APPROVED					

MITEL SEMICONDUCTOR

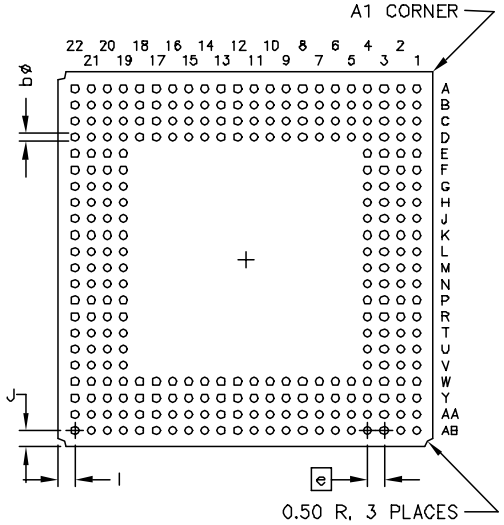
Title: Package Outline Drawing for 208 lds LQFP (GP) (28x28x1.4) mm, Body+2.0 mm

Drawing Number

GPD00214



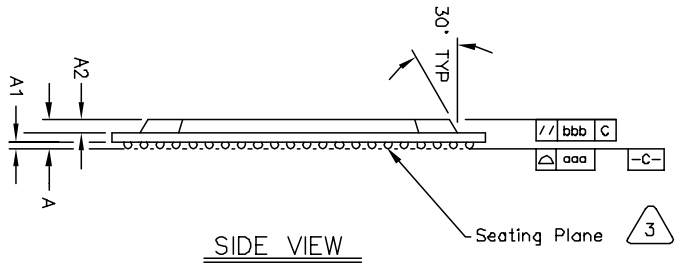
TOP VIEW



BOTTOM VIEW

DIMENSION	MIN	MAX
A	1.35	1.75
A1	0.30	0.50
A2	0.75	0.85
D	23.00 BSC	
D1	19.00	20.20
E	23.00 BSC	
E1	19.00	20.20
I	1.00 REF.	
J	1.00 REF.	
b	0.40	0.60
e	1.00 BSC	
N	288	

Conforms to JEDEC MO-151 AAJ-1 Iss. D



SIDE VIEW

NOTE:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER
3. PRIMARY DATUM -C- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. ALL DIMENSIONS ARE IN MILLIMETERS.
5. NOT TO SCALE.
6. BALL ARRANGEMENT: OUTER ROWS 4 DEEP (TOTAL 288).

ORIGINATING SITE: Swindon

ISSUE	1				
ACN	207901				
DATE	29NOV99				
APPRD.					

MITEL SEMICONDUCTOR

Title: Package Outline For 288 PBGA (23 X 23)MM (BP)

Drawing Number

GPD00689

MITEL

SEMICONDUCTOR

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