SRAM MODULE

64K x 32 SRAM
LOW VOLTAGE

FEATURES

- High speed: 17, 20, 25, 30 and 35ns
- High-performance, low-power CMOS process
- Single +3.3V ± 0.3V power supply
- 5V-tolerant I/O
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- Low profile
- Industry-standard pinout
- All inputs and outputs are TTL-compatible
- Upgradable with 128K x 32 and 256K x 32 modules

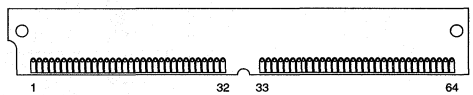
OPTIONS — MARKING

- Timing
  - 17ns access — -17
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - 64-pin SIMM — M
  - 64-pin ZIP — Z
- 2V data retention — L
- 2V data retention, low power — LP
- Part Number Example: MT8LS6432Z-20 LP

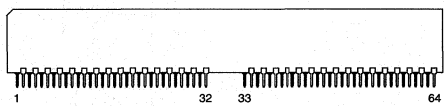
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

64-Pin SIMM
(SF-2)



64-Pin ZIP
(SG-3)



PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	$\overline{CE4}$	49	A4
2	PD0	18	A9	34	$\overline{CE3}$	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	$\overline{OE}$	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	$\overline{WE}$	44	DQ19	60	DQ23
13	A0	29	A15	45	DQ28	61	DQ31
14	A7	30	A14	46	DQ20	62	DQ24
15	A1	31	$\overline{CE2}$	47	A3	63	DQ32
16	A8	32	$\overline{CE1}$	48	A10	64	Vss

GENERAL DESCRIPTION

The MT8LS6432 is a high-speed SRAM memory module containing 65,536 words organized in a x32-bit configuration. The module consists of eight low voltage 64K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4 printed circuit board.

Data is written into to the SRAM memory when write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and output enable ($\overline{OE}$) are LOW. $\overline{CE}$ and/or $\overline{OE}$ can set the output in a High-Z state for additional flexibility in system design and memory expansion.

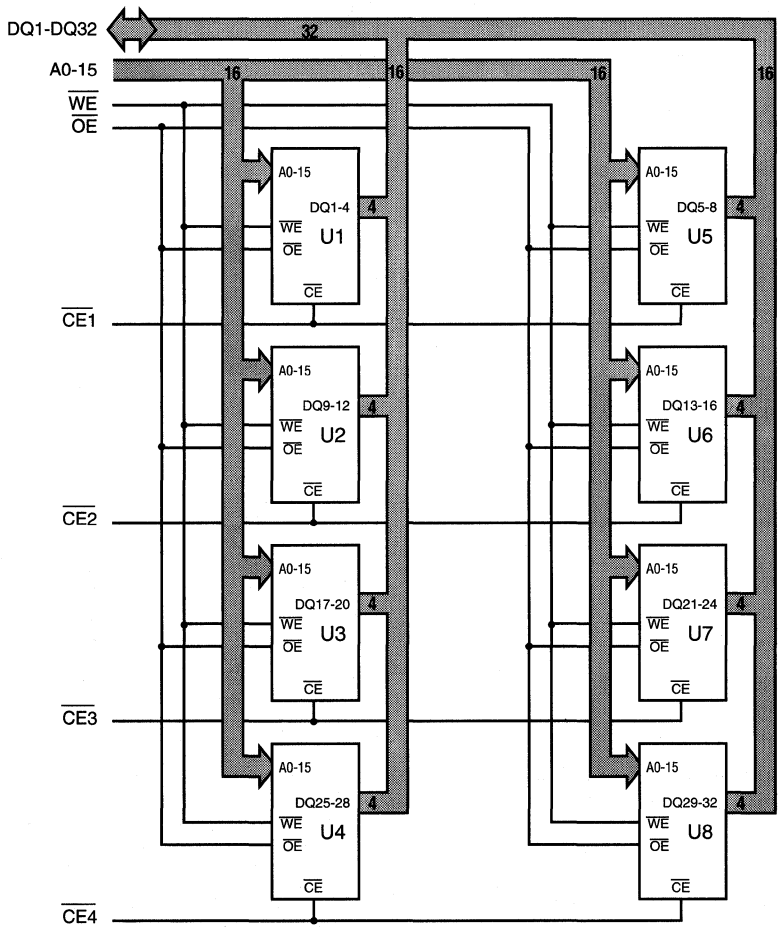
PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry standard modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$) are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +3.3V DC supply and all inputs and outputs are fully TTL-compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

NEW ■ SRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



PRESENCE DETECT
PD0 = No Connect
PD1 = Vss

U1-U8 = MT5LC2565DJ

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to +6.0V
Storage temperature ..... -55°C to +125°C
Power dissipation 8W
Short circuit output current 50mA
Voltage on Any Pin Relative to V_{SS} ..... -1V to V_{CC} +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5V	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-8	8	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

					MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	TYP	-17	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{CC}	STD, L	584	880	860	760	720	mA	3, 13
			LP	312	520	500	440	400	mA	
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX outputs open f = MAX = 1/tRC	I_{SB1}	STD, L	136	240	230	200	200	mA	13
			LP	64	144	140	120	96	mA	13
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD, L	8	24	24	24	24	mA	13
			LP	2.4	2.25	2.25	2.25	2.25	mA	13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A15, $\overline{WE}$, $\overline{OE}$	T_A = 25°C; f = 1 MHz V_{CC} = 3.3V	C_I	55	pF	4
Input Capacitance: $\overline{CE}$1-$\overline{CE}$4		C12	15	pF	4
Input/Output Capacitance: DQ1-DQ32		$C_{I/O}$	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

		-17		-20		-25		-35			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ Cycle											
READ cycle time	^tRC	17		20		25		35		ns	
Address access time	^tAA		17		20		25		35	ns	
Chip Enable access time	^tACE		17		20		25		35	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Output hold from address change	^tOH	4		4		4		4		ns	15
Chip Enable to output in Low-Z	^tLZCE	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	4		4		4		4		ns	15
Chip disable to output in High-Z	^tHZCE		9		9		10		15	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		17		20		25		35	ns	
Output Enable access time	^tAOE		8		8		8		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		7		7		7		12	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	17		20		25		35		ns	
Chip Enable to end of write	^tCW	12		15		15		20		ns	
Address valid to end of write	^tAW	12		15		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	1		1		1		1		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	15
WRITE pulse width	$^tWP1$	12		12		15		20		ns	
WRITE pulse width	$^tWP2$	12		15		15		20		ns	
Data setup time	^tDS	10		10		10		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		10		10		10		15	ns	6, 7

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

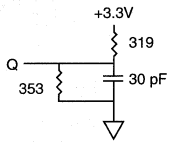


Fig. 1 OUTPUT LOAD EQUIVALENT

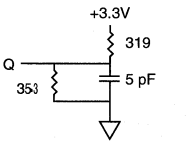


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

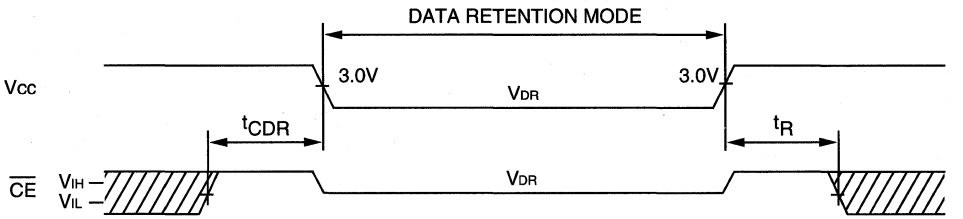
1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \le +6.0$ for $t \le {}^tKC/2$
   Undershoot: $V_{IL} \ge -2.0$ for $t \le {}^tKC/2$
   Power-up: $V_{IH} \le +6.0$ and $V_{CC} \le 3.1V$ for $t \le 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = READ cycle time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
14. Typical currents are measured at 25°C. MAX is over operating temperature range.
15. This timing specification is only valid for P (low power) parts.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

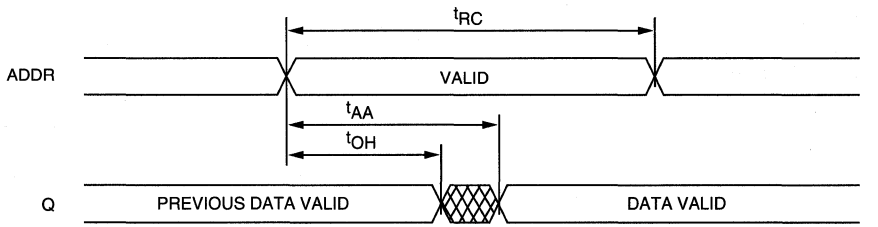
DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current L Version	$\overline{CE} \ge V_{CC}$ -0.2V Other inputs: $V_{IN} \ge V_{CC}$ -0.2V or $V_{IN} \le V_{SS}$+0.2V V_{CC} = 2V	I_{CCDR}		1,560	2,800	µA	14
Data Retention Current LP Version	$\overline{CE} \ge V_{CC}$ -0.2V V_{CC} = 2V	I_{CCDR}		1,560	2,800		
Chip Deselect to Data Retention Time		${}^tCDR$	0			ns	4
Operation Recovery Time		${}^tR$	${}^tRC$			ns	4, 11

NEW SRAM MODULE

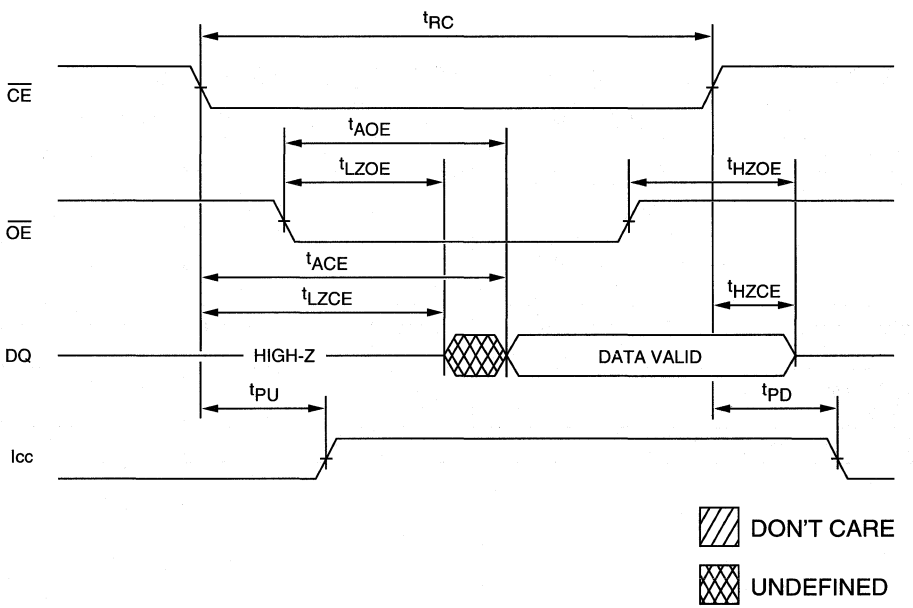
LOW Vcc DATA RETENTION WAVEFORM



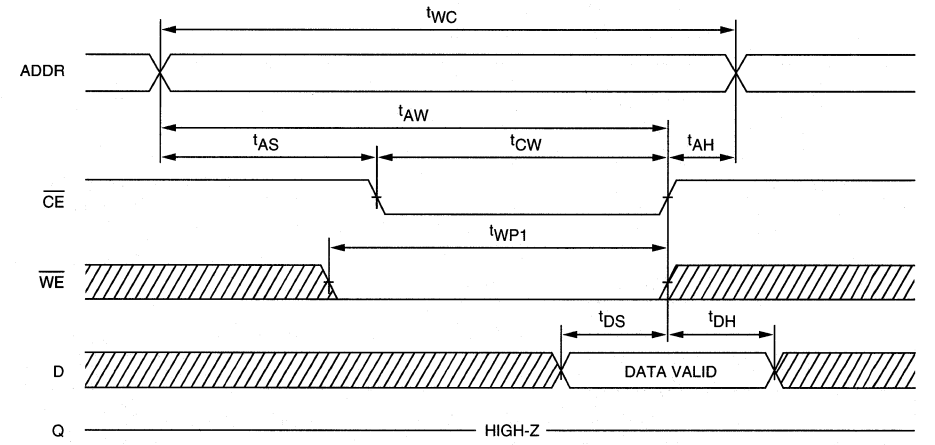
READ CYCLE NO. 1 [8, 9]



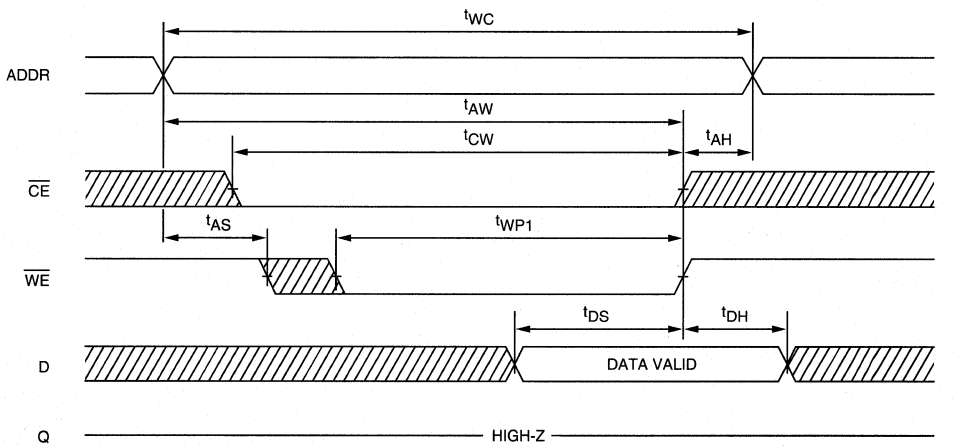
READ CYCLE NO. 2 [7, 8, 10]



WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



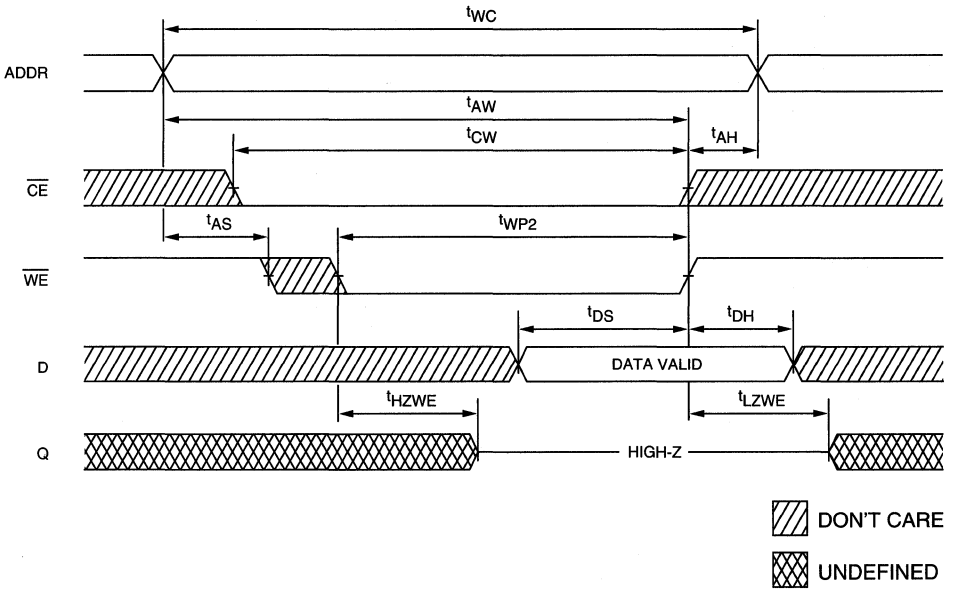
WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

NEW SRAM MODULE

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).