MT83P06N3

P-Channel Enhancement Mode Field Effect Transistor

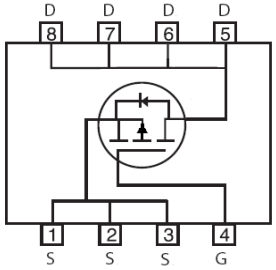
MT Semiconductor®

http://www.mtsemi.com

Product Summary

- V_{DS}= -30V
- I_D= -40A
- $R_{DS(ON)}$ ≦12mΩ@V_{GS}= -10V
- $R_{DS(ON)}$ ≦16.0mΩ@V_{GS}= -4.5V

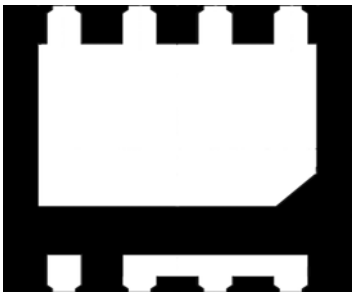
Simplified Schematic



Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low
- On-Resistance.
- Lead free product is acquired.
- RoHS Compliant.

MARKING DIAGRAM & PIN ASSIGNMENT



PIN1

Applications

- Notebook Computer
- Portable Battery Pack

Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Symbol	Parameter	10s	Steady State	Units
V_{DS}	Drain-Source Voltage	-30		V
V_{GS}	Gate-Source Voltage	±20		V
I_D	Continuous Drain Current [1]	-47	-40	A
I_{DM}	Pulsed Drain Current [2]	-50		A
I_S	Continuous Source Current (Diode Conduction) [1]	-2.7	-1.36	A
P_D	Maximum Power Dissipation [1]	3.0	1.5	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150		℃

Thermal Resistance Ratings

Symbol	Parameter		Typical	Maximum	Unit
R_{thJA}	Maximum Junction-to-Ambient [1]	t≦10 Sec	33	42	℃/W
		Steady State	70	82	

Notes:

1. Surface Mounted on 1” x 1” FR4 Board.
2. Pulse width limited by maximum junction temperature.

Electrical Characteristics (T_A=25°C, unless otherwise noted)

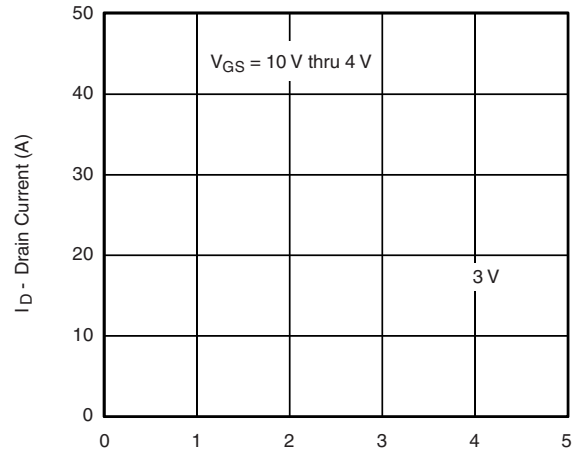
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
● Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250μA	-30	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = -250μA	-1.0	-1.6	-3	V
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24V, V_{GS} = 0V	-	-	-1	μA
		V_{DS} = -24V, V_{GS} = 0V, T_J = 70℃		-	-10	
$R_{DS(on)}$	Drain Source On State Resistance [a]	V_{GS} = -10V, I_D = -10A	-	10	12	mΩ
		V_{GS} = -4.5V, I_D = -8A	-	14	16	
g_{fs}	Forward Transconductance [a]	V_{DS} = -15V, I_D = -9A	-	40	-	S
V_{SD}	Diode Forward Voltage [a]	I_S = -2.7A, V_{GS} = 0V	-	-0.74	-1.1	V
● Dynamic Characteristics [b]						
C_{iss}	Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1MHz	-	3340.0	-	pF
C_{oss}	Output Capacitance		-	577.0	-	
C_{rss}	Reverse Transfer Capacitance		-	426.0	-	
Q_g	Total Gate Charge	V_{DS} = -15V, V_{GS} = -5V, I_D = -13A	-	37.0	-	nC
Q_{gs}	Gate-Source Charge		-	10.0	-	
Q_{gd}	Gate-Drain Charge		-	11.0	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -15V, R_L = 15Ω I_D = -1A, V_{GEN} = -10V, R_G = 6Ω	-	19.5	-	nSec
t_r	Rise Time		-	10.0	-	
$T_{d(off)}$	Turn-Off Delay Time		-	137.5	-	
t_f	Fall Time		-	55.3	-	
R_g	Gate Resistance	V_{GS} = 0, V_{DS} = 0, f = 1MHz	-	3.4	-	Ω
t_{rr}	Source-Drain Reverse Recovery Time	I_F = -2.1A, di/dt = 100A/μs	-	60	100	nSec

Note:

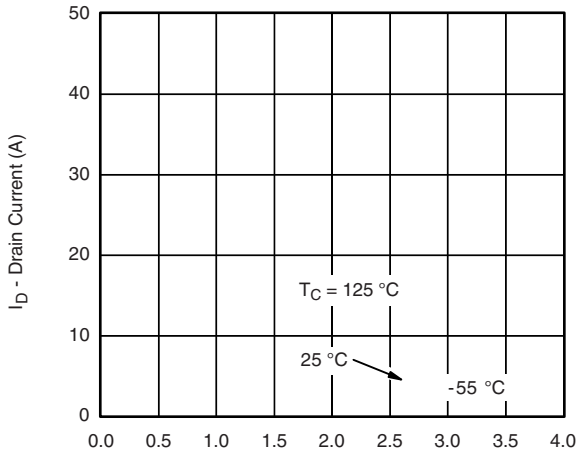
a. Pulse test; pulse width≦300μs, duty cycle≦2%.

b. Guaranteed by design, not subject to production testing.

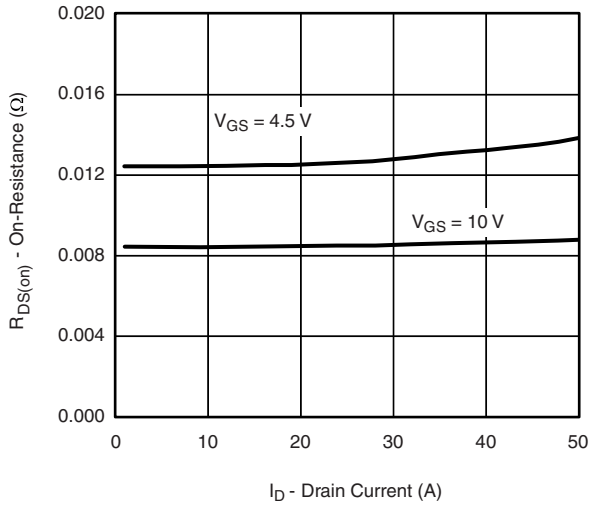
Characteristics Curve (T_A=25°C, unless otherwise noted)



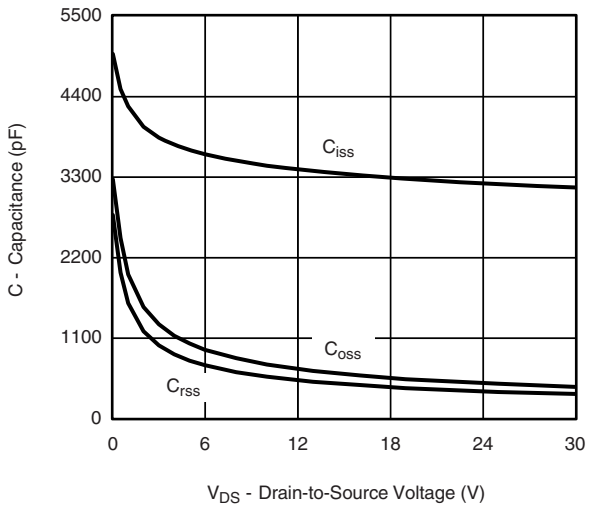
Output Characteristics



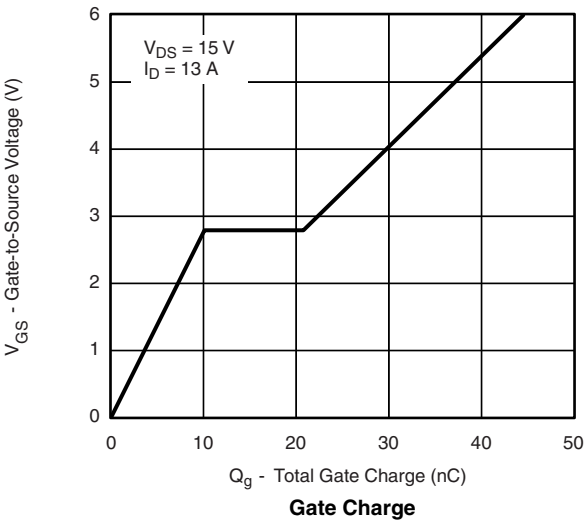
Transfer Characteristics



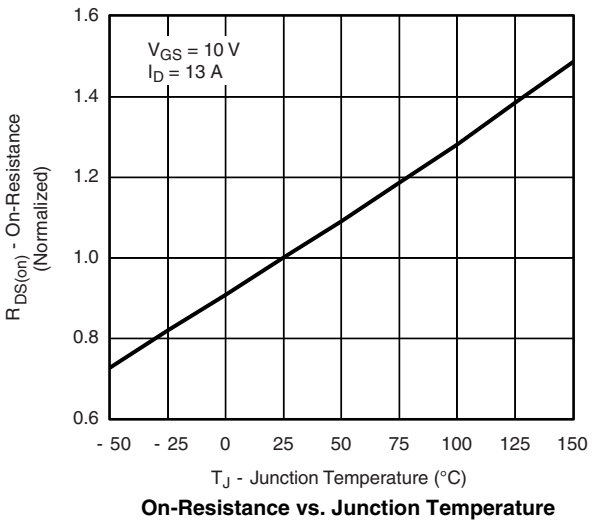
On-Resistance vs. Drain Current



Capacitance

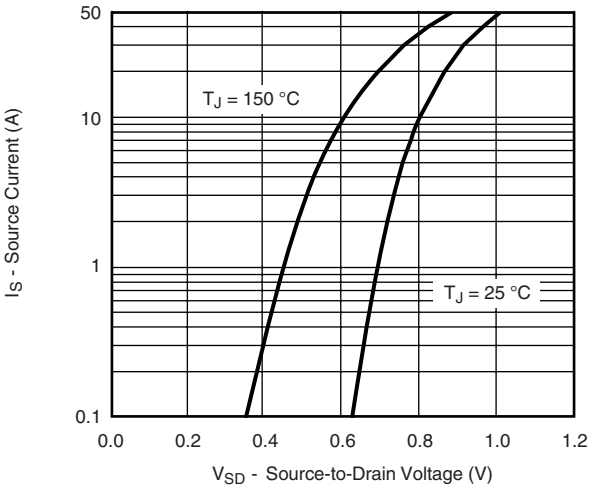


Gate Charge

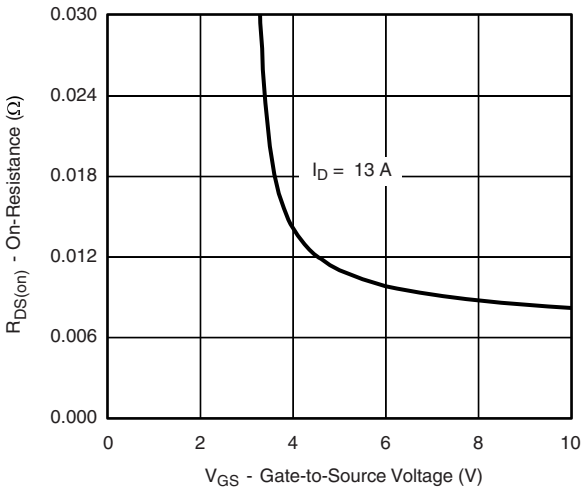


On-Resistance vs. Junction Temperature

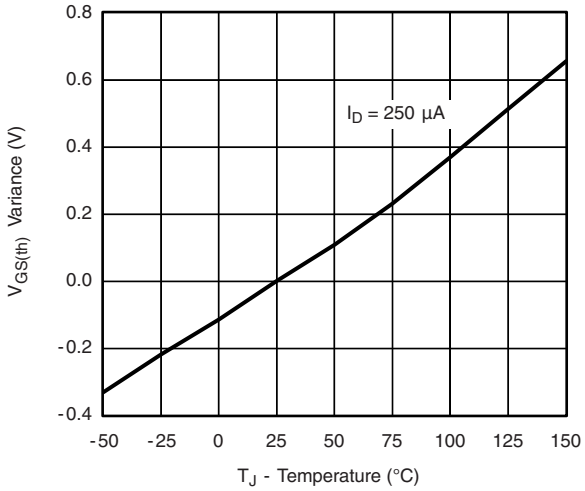
Characteristics Curve (T_A=25°C, unless otherwise noted)



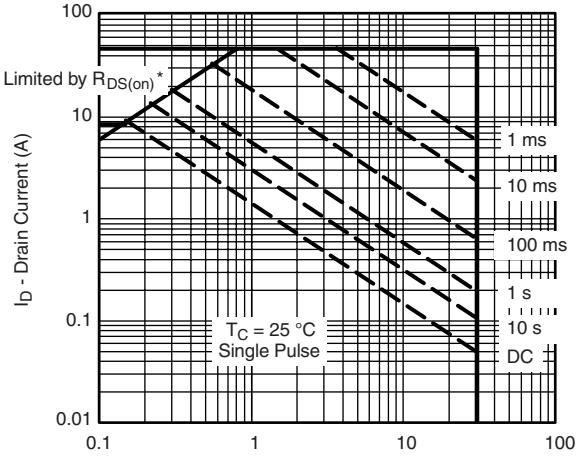
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

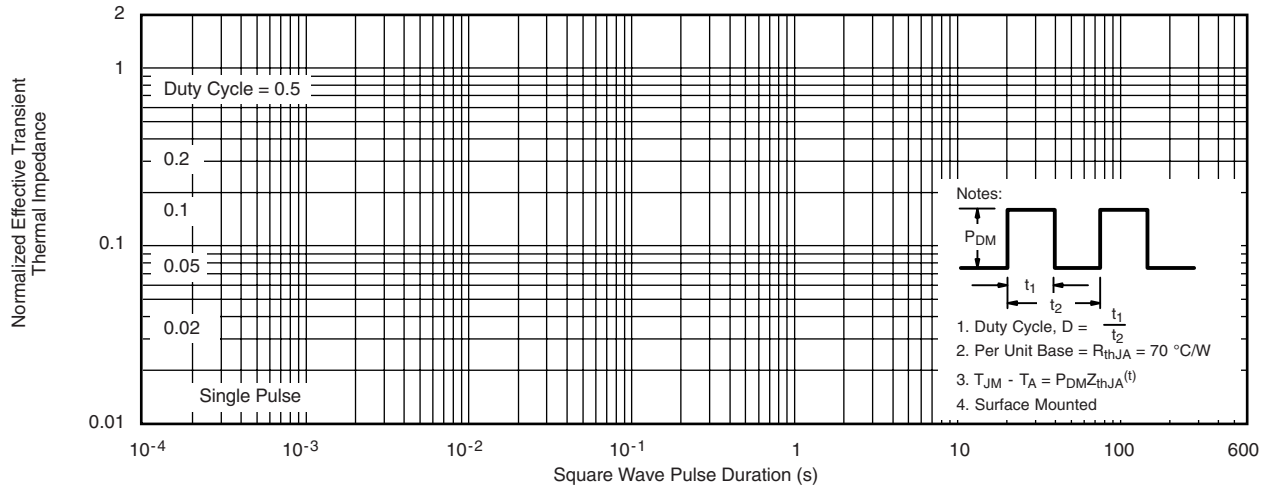


Threshold Voltage



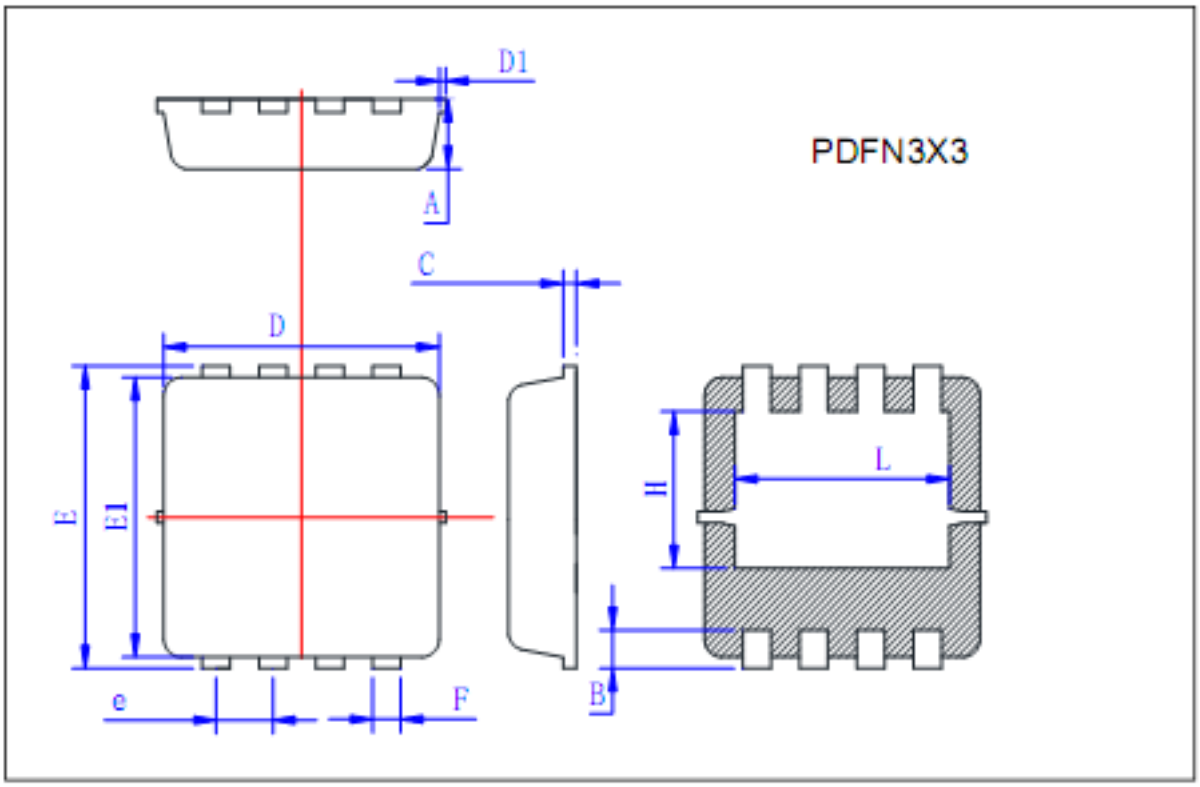
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient

PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	2.35	2.45	2.55

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