MT8362N3

Dual N & P-Channel PowerTrench® MOSFET

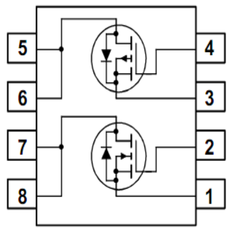
General Description

These dual N and P-Channel enhancement mode power field effect transistors are produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

MT Semiconductor®

http://www.mtsemi.com

Simplified Schematic

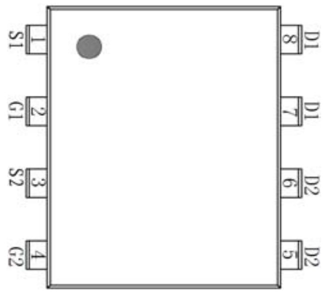


Features

- N-Channel
  30V/10A
  $R_{DS(on)}$ = 0.021Ω @ V_{GS} = 10V
  $R_{DS(on)}$ = 0.033Ω @ V_{GS} = 4.5V
- P-Channel
  -30V/-6A
  $R_{DS(on)}$ = 0.050Ω @ V_{GS} = -10V
  $R_{DS(on)}$ = 0.075Ω @ V_{GS} = -4.5V

MARKING DIAGRAM & PIN ASSIGNMENT

DFN3X3-8L



Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Symbol	Parameter		N-CH	P-CH	Units
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		±20	±20	V
I_D	Drain Current - Continuous	(Note 1a)	10	-6	A
	- Pulsed		30	-18	
P_D	Power Dissipation for Dual Operation		3.5		W
	Power Dissipation for Single Operation	(Note 1a)	2.6		
		(Note 1b)	1.5		
		(Note 1c)	1.2		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	68	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	35	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MT8362N3	MT8362N3	13"	12mm	2500 units

Electrical Characteristics T_A = 25°C unless otherwise noted

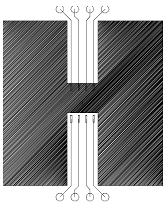
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA V_{GS} = 0 V, I_D = -250 µA	N-CH P-CH	30 -30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = -250 µA, Referenced to 25°C	N-CH P-CH		25 -22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = -24 V, V_{GS} = 0 V	N-CH P-CH			1 -1	µA
I_{GSSF}	Gate-Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA V_{DS} = V_{GS}, I_D = -250 µA	N-CH P-CH	1 -1	1.6 -1.7	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C I_D = -250 µA, Referenced to 25°C	N-CH P-CH		-4.3 4		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 8A V_{GS} = 10 V, I_D = 8A, T_J = 125°C V_{GS} = 4.5 V, I_D = 6A	N-CH		21 30 33	25 35 38	mΩ
		V_{GS} = -10 V, I_D = -8A V_{GS} = -10 V, I_D = -8A, T_J = 125°C V_{GS} = -4.5 V, I_D = -6A	P-CH		50 58 75	54 78 80	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V V_{GS} = -10 V, V_{DS} = -5 V	N-CH P-CH	10 -6			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 5 A V_{DS} = -5 V, I_D =-5 A	N-CH P-CH		19 11		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	N-CH V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz P-CH V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	N-CH P-CH		809 690		pF
C_{oss}	Output Capacitance		N-CH P-CH		163 306		pF
C_{rss}	Reverse Transfer Capacitance		N-CH P-CH		68 77		pF

Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

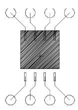
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time	N-CH V_{DD} = 10 V, I_D = 1 A, V_{GS} = 10V, R_{GEN} = 6 Ω P-CH V_{DD} = -10 V, I_D = -1 A, V_{GS} = -10V, R_{GEN} = 6 Ω	N-CH P-CH		2.2 6.7	4.4 13.4	ns
t_r	Turn-On Rise Time		N-CH P-CH		7.5 9.7	15 19.4	ns
$t_{d(off)}$	Turn-Off Delay Time		N-CH P-CH		11.8 19.8	21.3 35.6	ns
t_f	Turn-Off Fall Time		N-CH P-CH		3.7 12.3	7.4 22.2	ns
Q_g	Total Gate Charge	N-CH V_{DS} = 15 V, I_D = 7 A, V_{GS} = 10 V P-CH V_{DS} = -15 V, I_D = -5 A, V_{GS} = -10 V	N-CH P-CH		18 14	26 23	nC
Q_{gs}	Gate-Source Charge		N-CH P-CH		2.5 2.4		nC
Q_{gd}	Gate-Drain Charge		N-CH P-CH		2.6 4.8		nC
Drain–Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-CH P-CH			10 -6	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2) V_{GS} = 0 V, I_S = -1.3 A (Note 2)	N-CH P-CH		0.81 -0.85	1.2 -1.2	V

Notes:

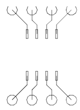
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°/W when mounted on a 0.5 in² pad of 2 oz copper



b) 125°/W when mounted on a .02 in² pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics: N-CH

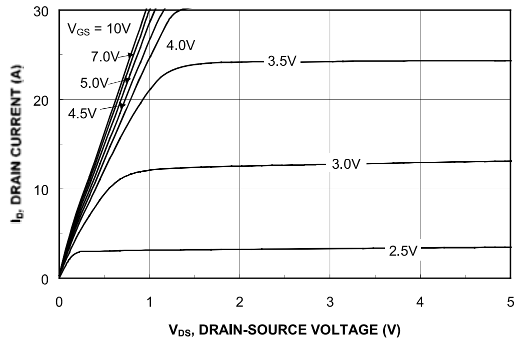


Figure 1. On-Region Characteristics.

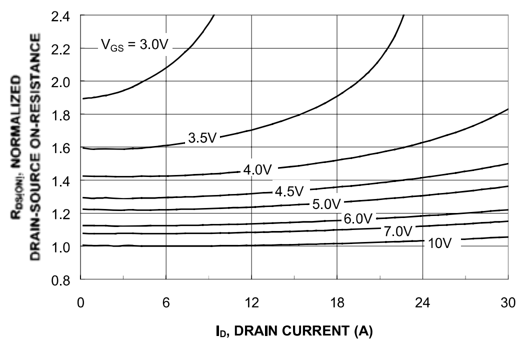


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

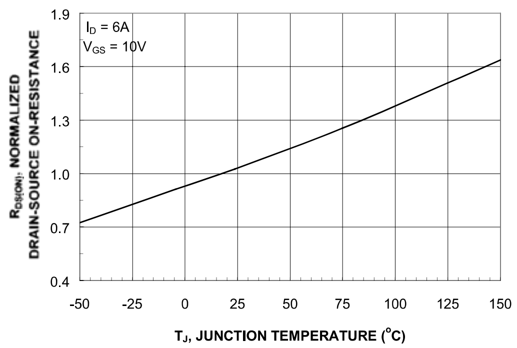


Figure 3. On-Resistance Variation with Temperature.

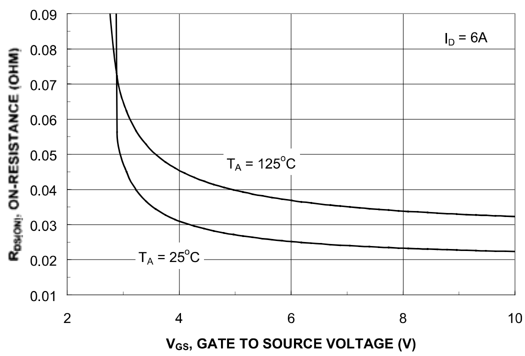


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

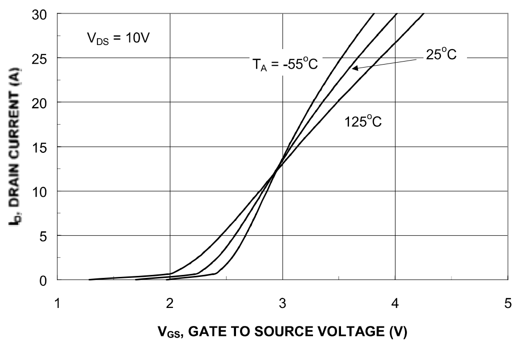


Figure 5. Transfer Characteristics.

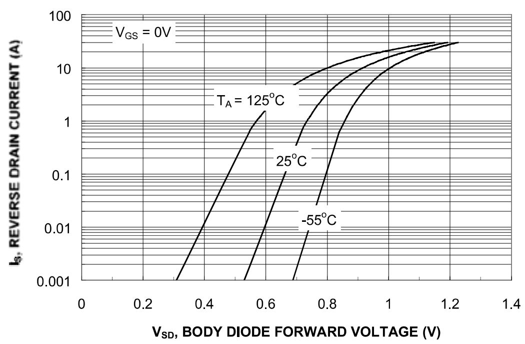


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-CH

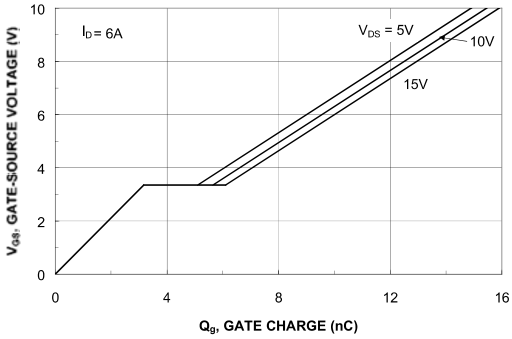


Figure 7. Gate Charge Characteristics.

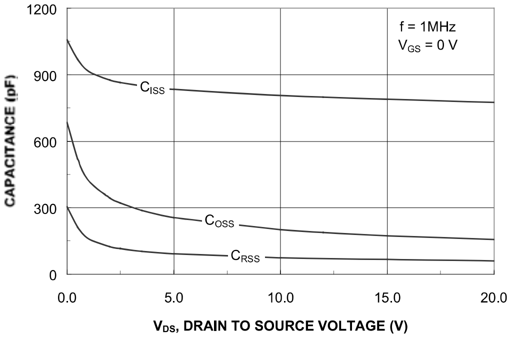


Figure 8. Capacitance Characteristics.

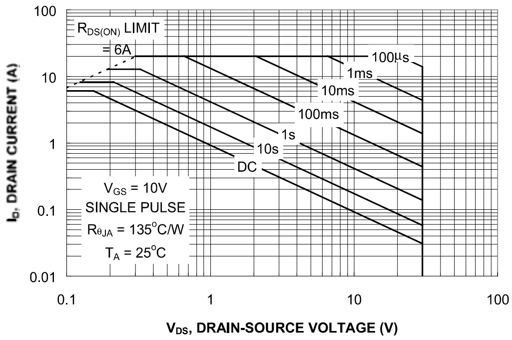


Figure 9. Maximum Safe Operating Area.

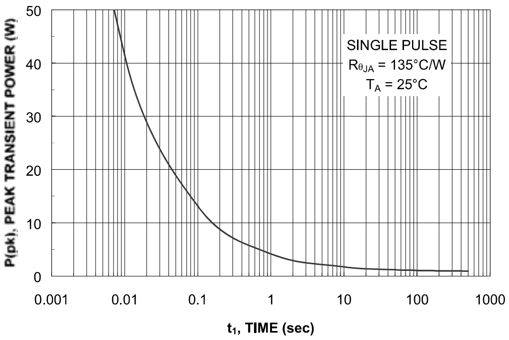


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics P-CH

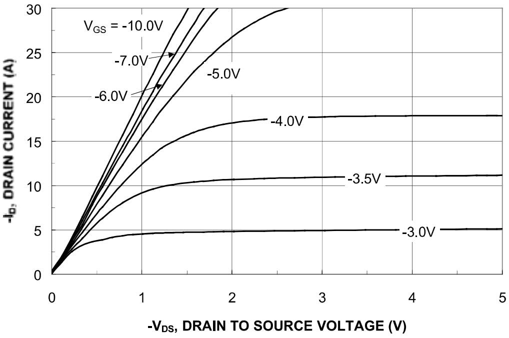


Figure 11. On-Region Characteristics.

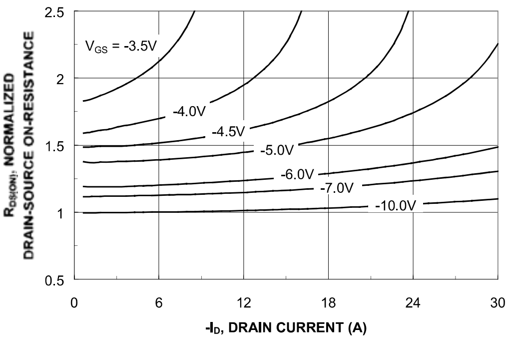


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

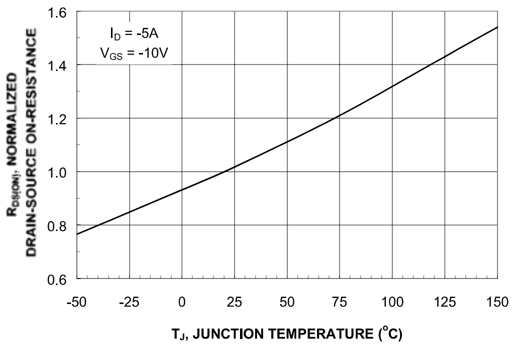


Figure 13. On-Resistance Variation with Temperature.

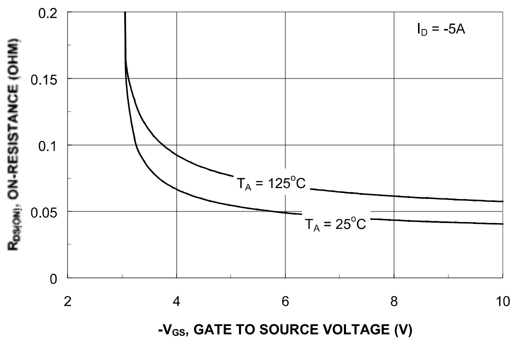


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

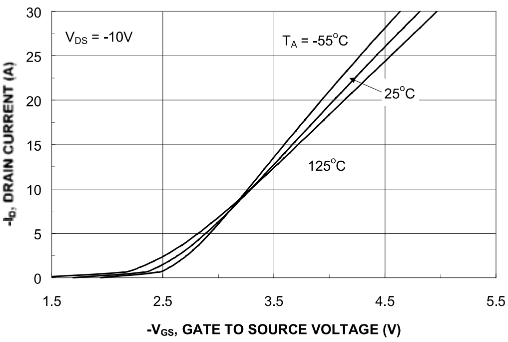


Figure 15. Transfer Characteristics.

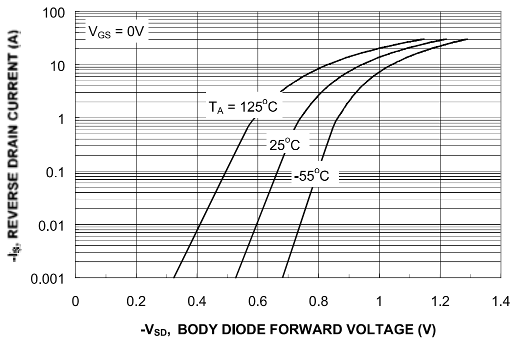


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics P-CH

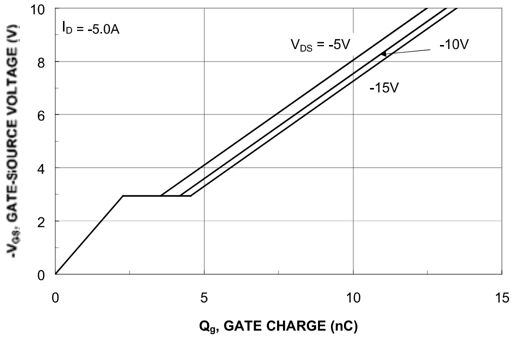


Figure 17. Gate Charge Characteristics.

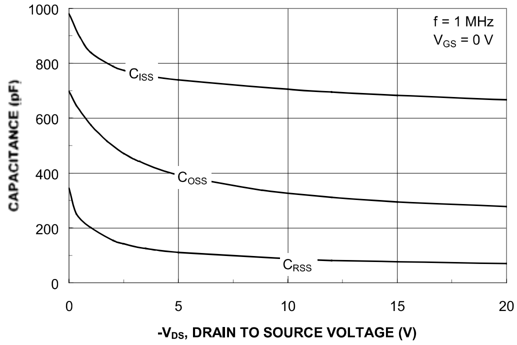


Figure 18. Capacitance Characteristics.

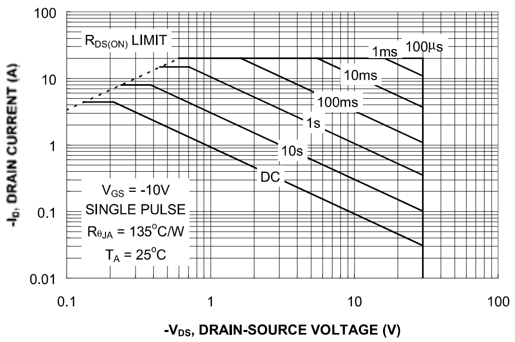


Figure 19. Maximum Safe Operating Area.

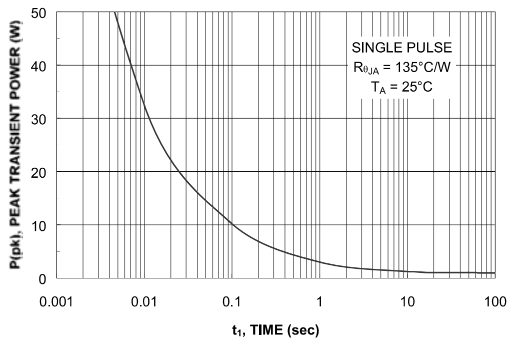


Figure 20. Single Pulse Maximum Power Dissipation.

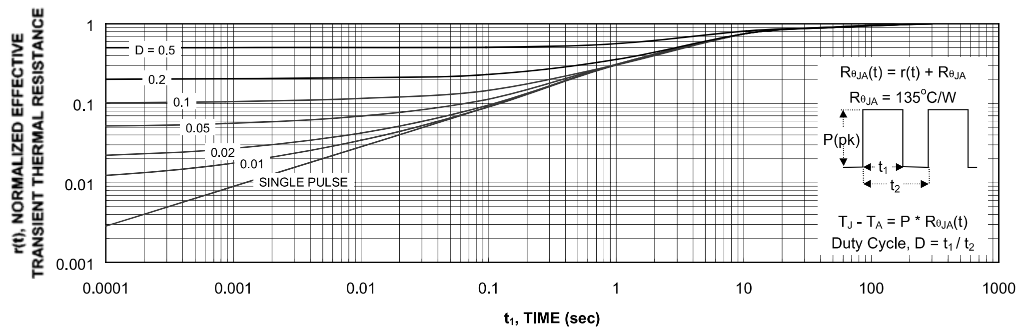
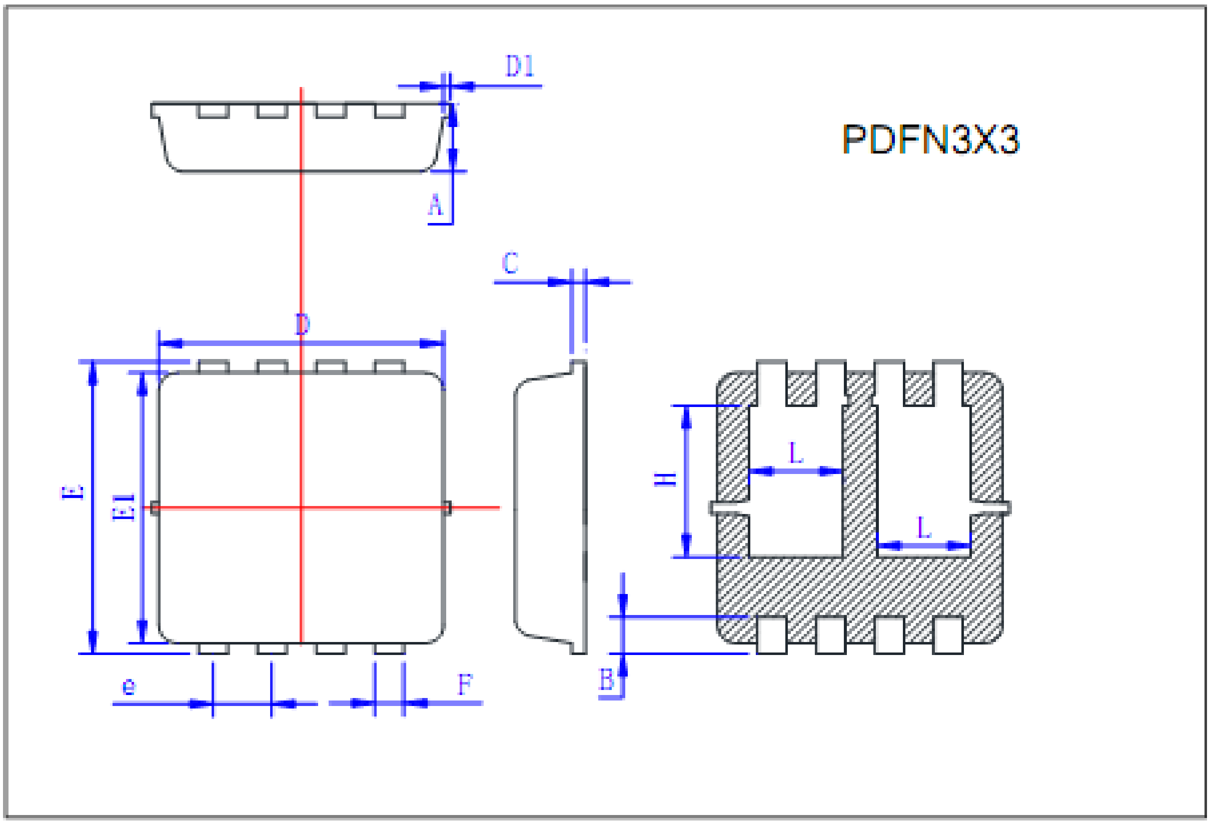


Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	0.93	1.03	1.13

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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.