MT8350

N-Channel Enhancement Mode Field Effect Transistor

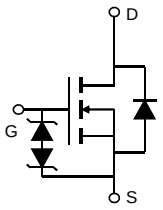
MT Semiconductor®

http://www.mtsemi.com

Product Summary

- V_{DS} = 30V
- I_D = 50A
- $R_{DS(ON)}$ (at V_{GS}=10V) 1.45mΩ
- $R_{DS(ON)}$ (at V_{GS}=4.5V) 1.66mΩ
- $R_{DS(ON)}$ (at V_{GS}=2.5V) 2.35mΩ

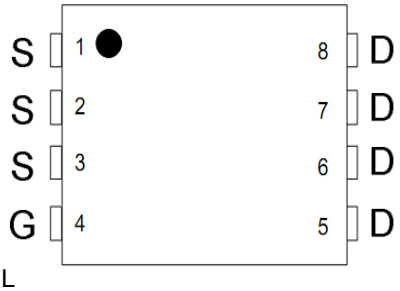
Simplified Schematic



Features

- Advanced Trench Process Technology.
- High Density Cell Design for Ultra Low
- Low Gate Charge
- ESD protection
- RoHS Compliant.

MARKING DIAGRAM & PIN ASSIGNMENT



DFN3.3X3.3-8L

Applications

- Load switch, battery switch in portable devices

Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current[G]	T_C=25℃	I_D	50	A
	T_C=100℃		39	
Pulsed Drain Current [C]		I_{DM}	200	
Continuous Drain Current	T_A=25℃	I_{DSM}	48	A
	T_A=70℃		38	
Avalanche Current [C]		I_{AS}	60	A
Avalanche energy L=0.05mH [C]		E_{AS}	90	mJ
V_{DS} Spike	100ns	V_{SPIKE}	36	V
Power Dissipation [B]	T_C=25℃	P_D	83.3	W
	T_C=100℃		33.3	
Power Dissipation [A]	T_A=25℃	P_{DSM}	6.2	W
	T_A=70℃		4	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	16	20	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		45	55	℃/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1.1	1.5	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	ID=250μA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		T_J=125℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±10V			±10	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250μA	0.5	0.85	1.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		1.45	1.8	mΩ
		T_J=125℃		2.05	2.6	
		V_{GS}=4.5V, I_D=20A		1.66	2.1	
		V_{GS}=2.5V, I_D=20A		2.35	3.1	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		125		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.61	1	V
I_S	Maximum Body-Diode Continuous Current [G]				50	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		4175		pF
C_{oss}	Output Capacitance			1505		pF
C_{rss}	Reverse Transfer Capacitance			300		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.5	1	1.5	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A		77.5	105	nC
Q_g(4.5V)	Total Gate Charge			37	50	nC
Q_{gs}	Gate Source Charge			6		nC
Q_{gd}	Gate Drain Charge			12.5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		6.5		ns
t_r	Turn-On Rise Time			7		ns
$t_{D(off)}$	Turn-Off DelayTime			58.5		ns
t_f	Turn-Off Fall Time			17.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/μs		20.3		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/μs		40.7		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

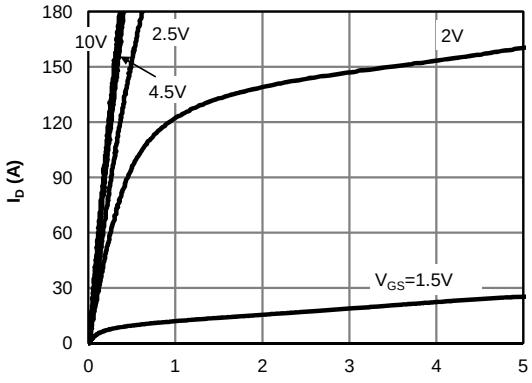


Fig 1: On-Region Characteristics (Note E)

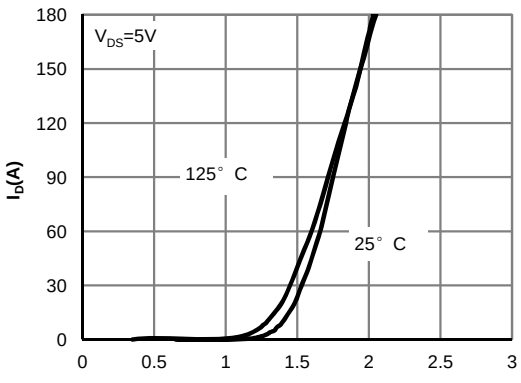


Figure 2: Transfer Characteristics (Note E)

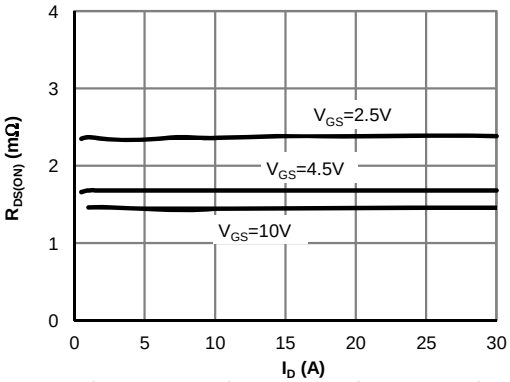


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

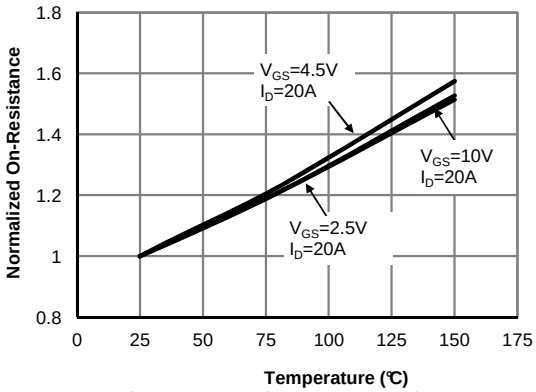


Figure 4: On-Resistance vs. Junction Temperature (Note E)

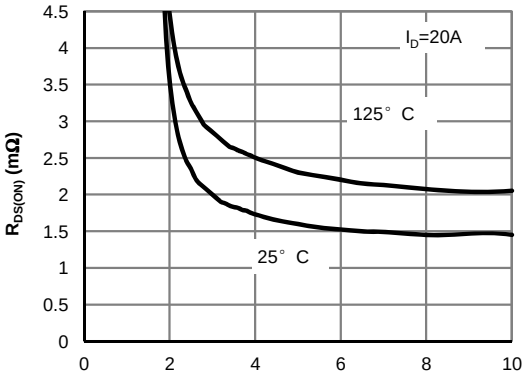


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

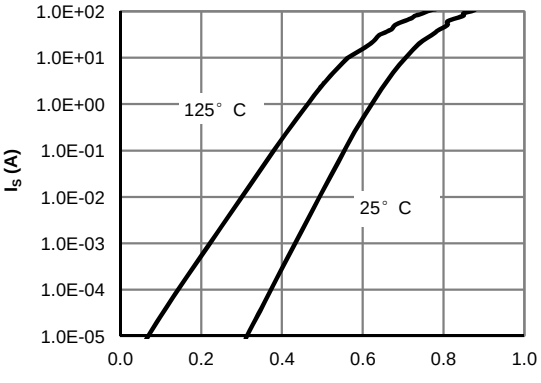


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

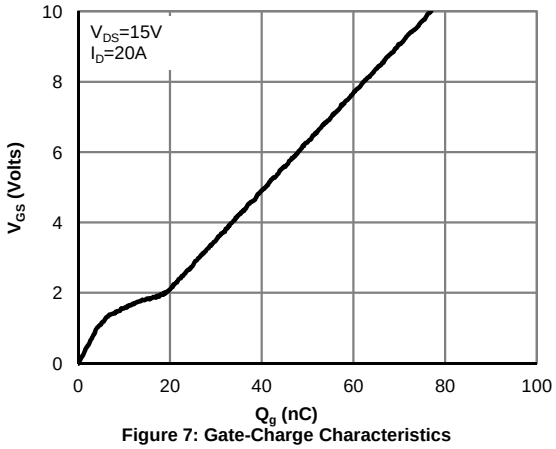


Figure 7: Gate-Charge Characteristics

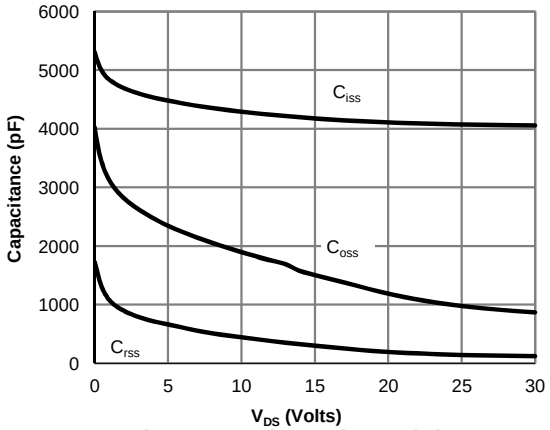


Figure 8: Capacitance Characteristics

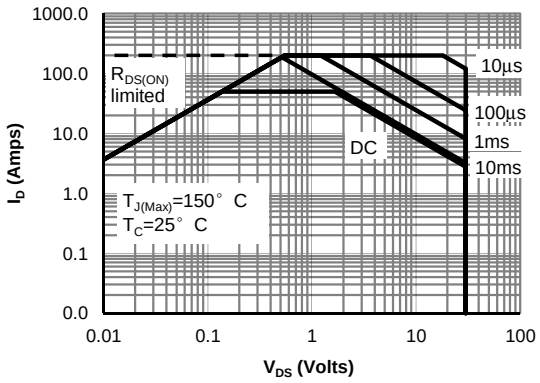


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

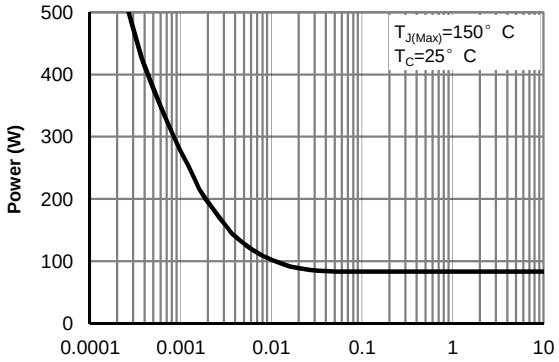


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

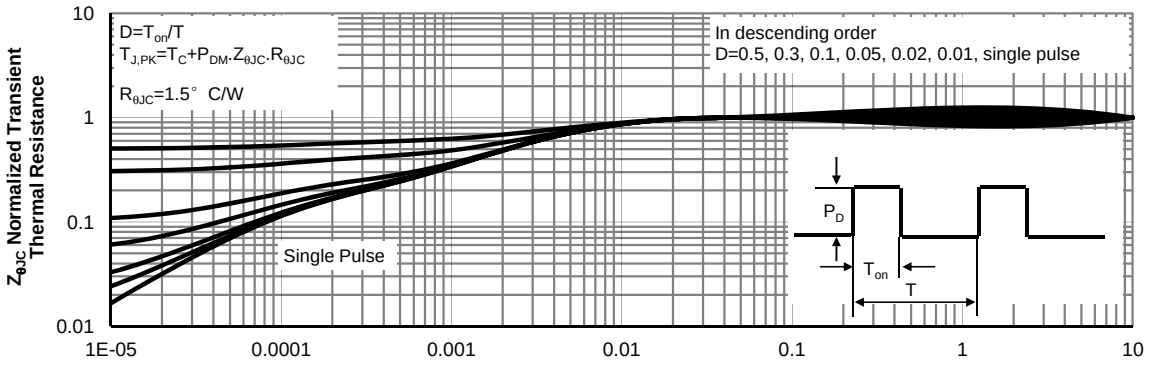


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

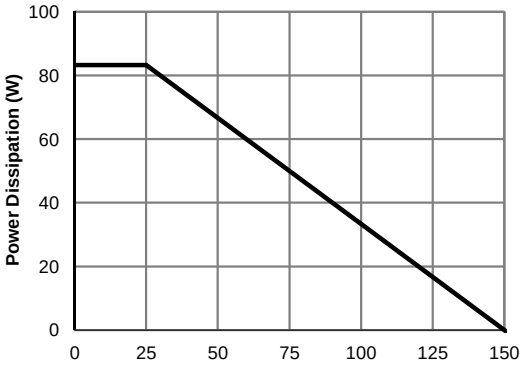


Figure 12: Power De-rating (Note F)

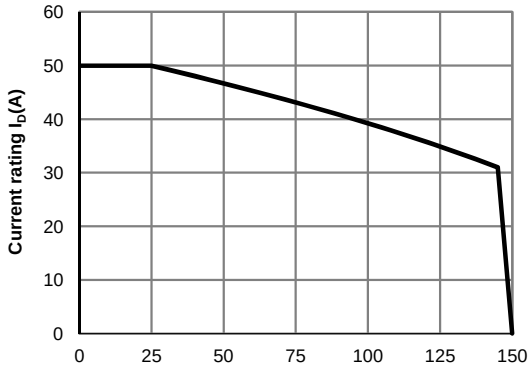


Figure 13: Current De-rating (Note F)

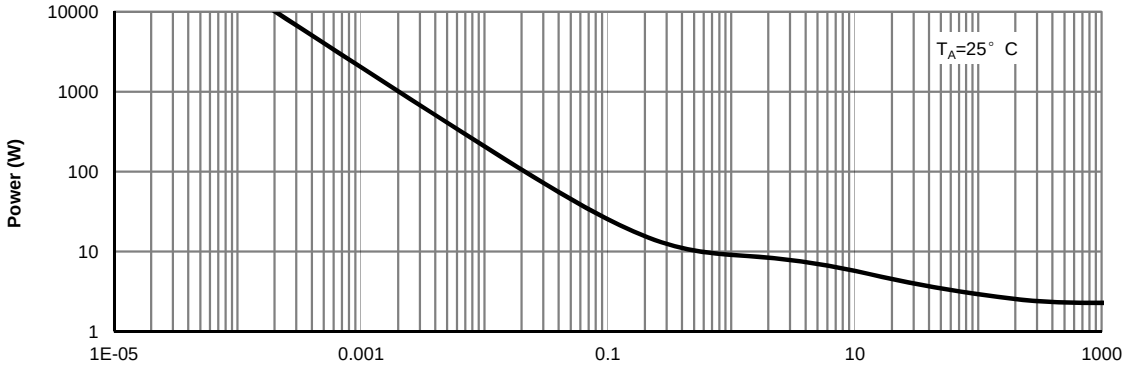


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

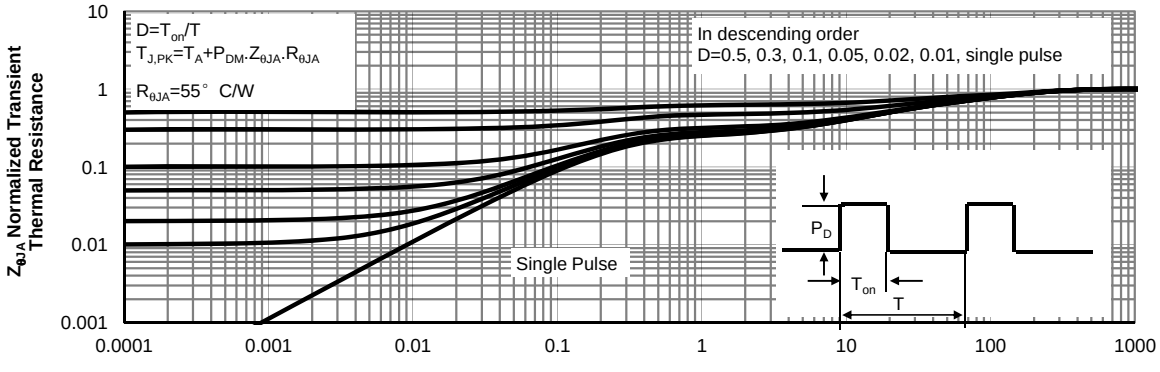
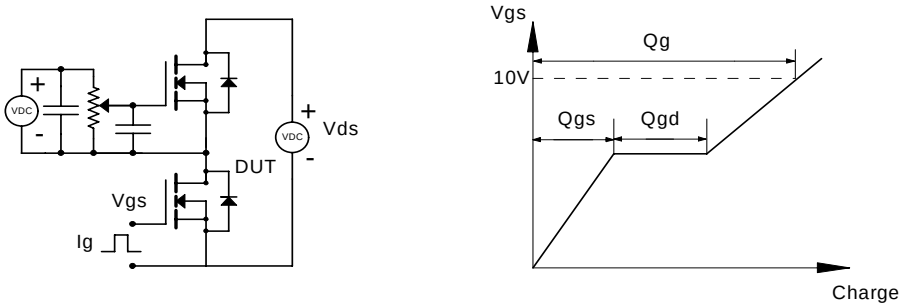
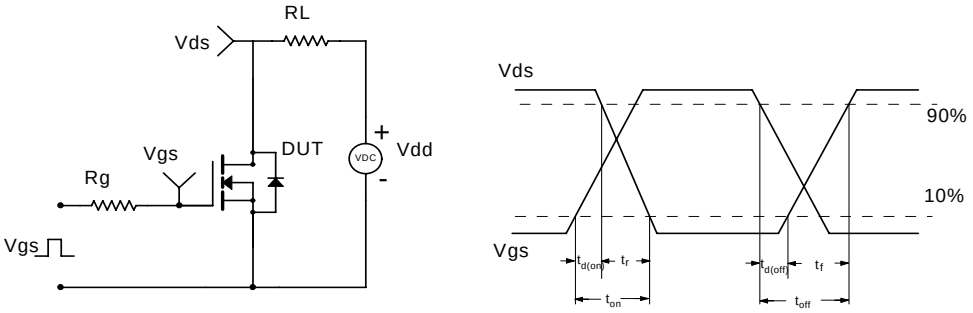


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

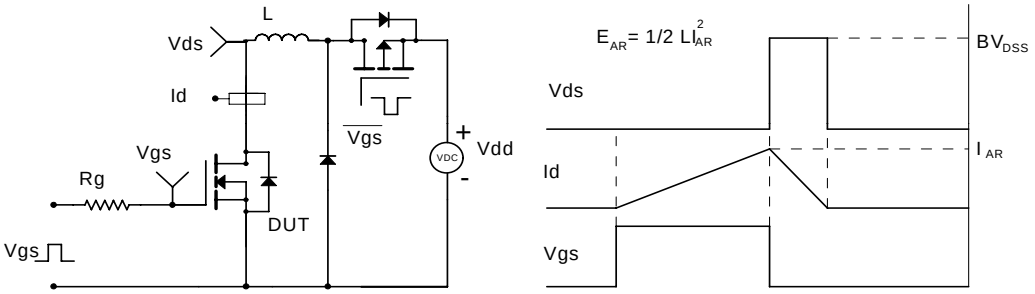
Gate Charge Test Circuit & Waveform



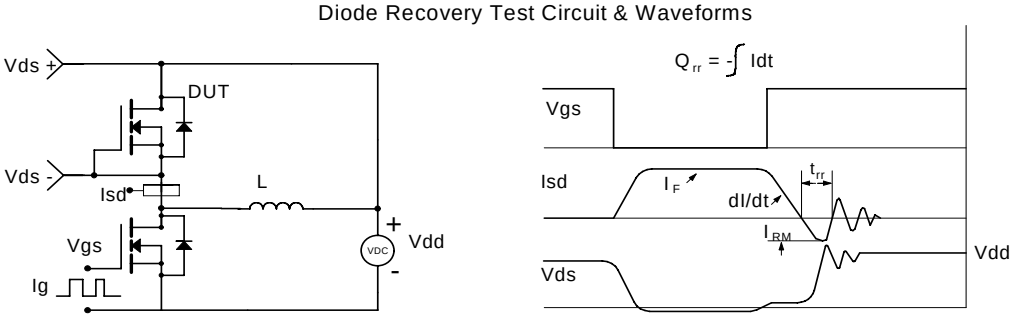
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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Keep safety first in your circuit designs!

1. MOS-TECH Semiconductor Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
   Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.