

MT8332N3

N-Channel Enhancement Mode Field Effect Transistor

Product Summary

PRODUCT SUMMARY		
V _{DSS}	I _D	R _{DS(ON)}
30V	25A	10 mΩ @ V _{GS} =10V
		15 mΩ @ V _{GS} =4.5V

Features

- Supper high dense cell design for low R_{DS(ON)}
- Rugged and reliable
- Simple drive requirement
- DFN3*3 Package

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current-Continuous ^a @T _j =125°C	I _D	25	A
Pulsed Drain Current ^B	I _{DM}	45	A
Maximum Power Dissipation ^a	P _D	1.3	W
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 150	°C

THERMAL CHARACTERISTICS

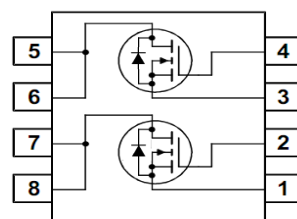
Thermal Resistance, Junction-to Ambient ^a	R _{th JA}	125	°C/W
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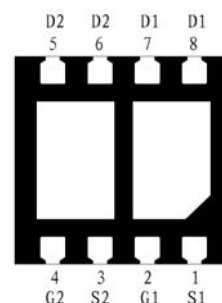
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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V,I _D =250 μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =24V,V _{GS} =0V			1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±24V,V _{DS} =0V			±100	nA
ON CHARACTERITICS						
Gate Threshold Voltage	V _{GS} (th)	V _{DS} =V _{GS} ,I _D =250 μA	1	1.8	3	V
Drain-Source On-State Resistance	R _{DS} (ON)	V _{GS} =10V,I _D =10A		10	14.5	m Ω
		V _{GS} =4.5V,I _D =5A		15	22	
DAYNAMIC CHARACTERISTICS						
Input Capacitance	C _{ISS}	V _{DS} =15V,V _{GS} =0V f=1.0MHz		580		pF
Output Capacitance	C _{OSS}			90		pF
Reverse Transfer Capacitance	C _{RSS}			78		pF
SWITCHING CHARACTERISISTICS						
Turn-On Delay Time	t _D (ON)	V _{DD} =15V I _D =5.3A, V _{GEN} =4.5V R _L =10ohm R _{GEN} =10ohm		9		ns
Rise Time	t _r			10		ns
Turn-Off Delay Time	t _D (OFF)			38		ns
Fall Time	t _f			23		ns
Total Gate Charge	Q _g	V _{DS} =15V,I _D =1A V _{GS} =10V		11.2		nC
Gate-Source Charge	Q _{gs}			2.1		nC
Gate-Drain Charge	Q _{gd}			2.9		nC

Notes

- Surface Mounted on FR4 Board, t ≤ 10sec
- Pulse Test: Pulse Width ≤ 300Us, Duty Cycle ≤ 2%
- Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

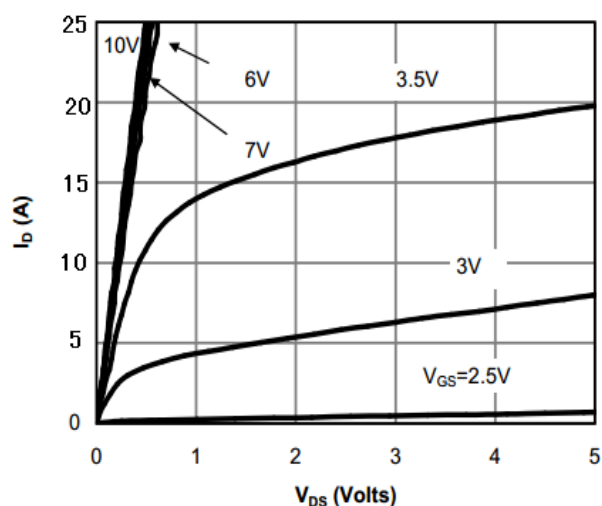


Fig 1: On-Region Characteristics (Note E)

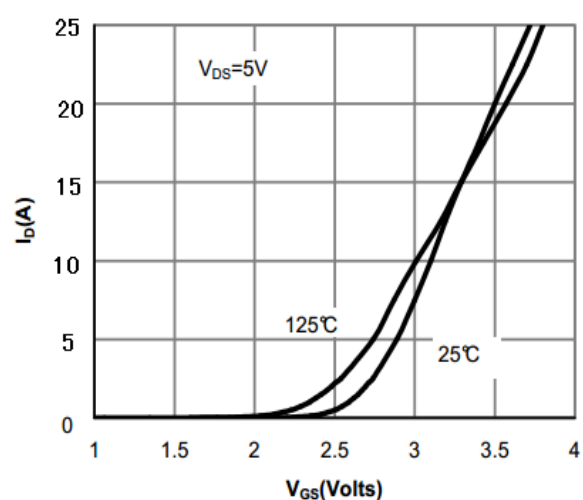


Figure 2: Transfer Characteristics (Note E)

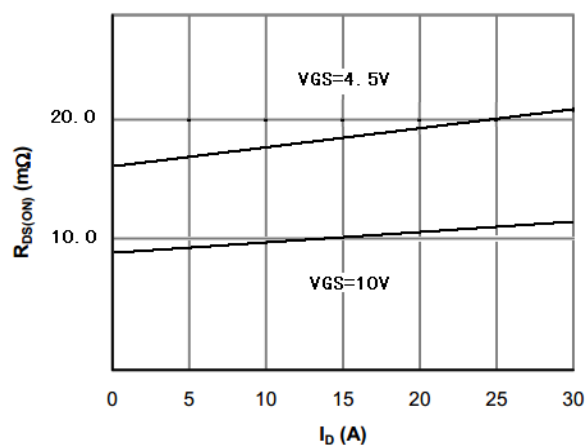


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

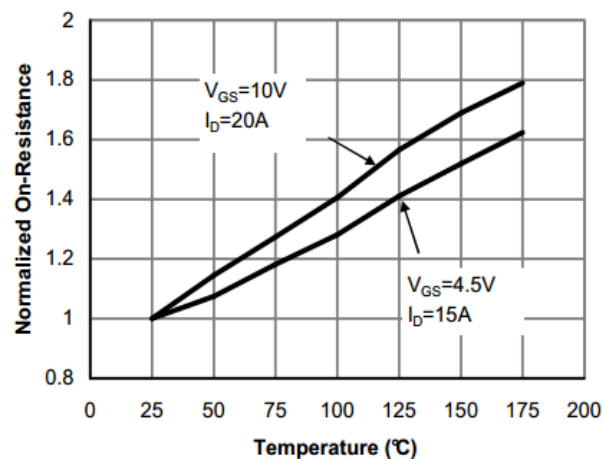


Figure 4: On-Resistance vs. Junction Temperature (Note E)

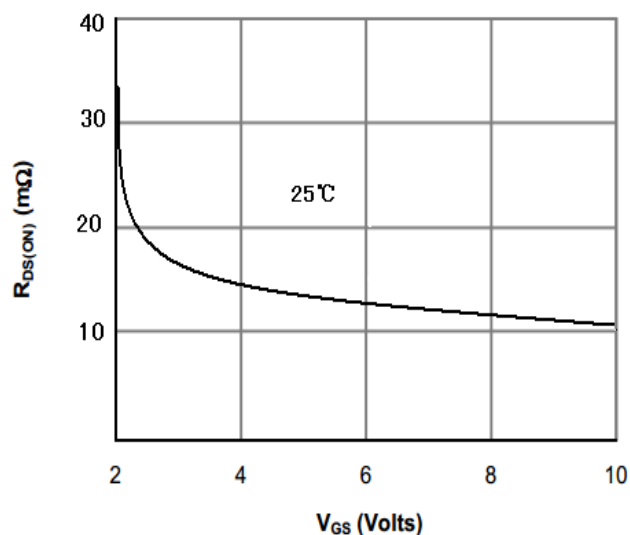


Figure 5: On-Resistance vs. Gate-Source Voltage

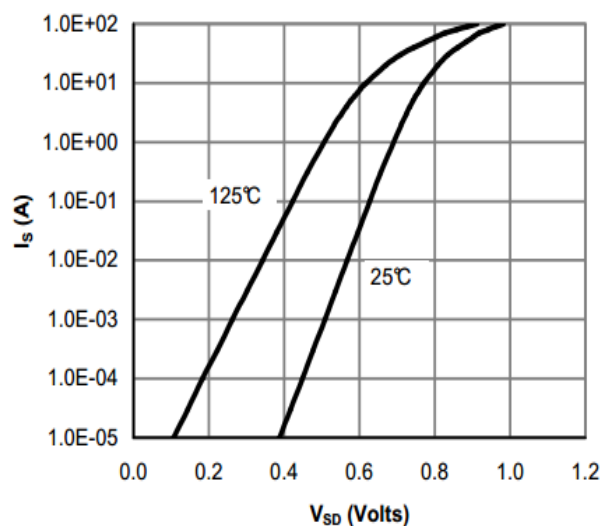


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

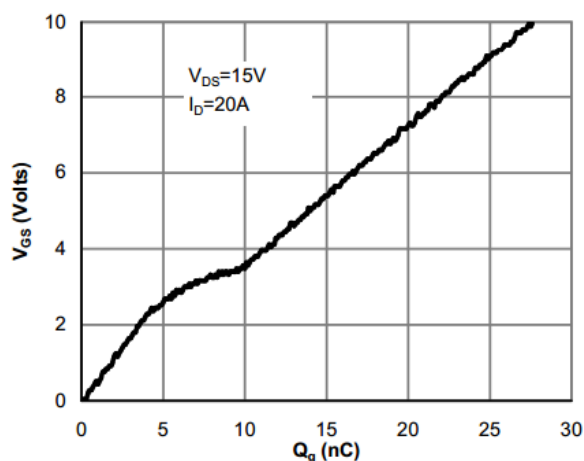


Figure 7: Gate-Charge Characteristics

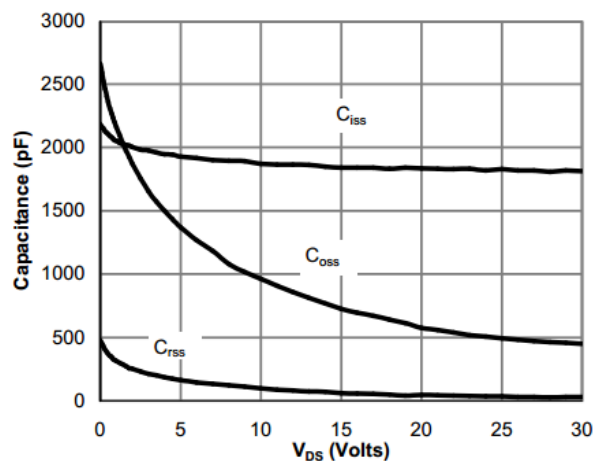


Figure 8: Capacitance Characteristics

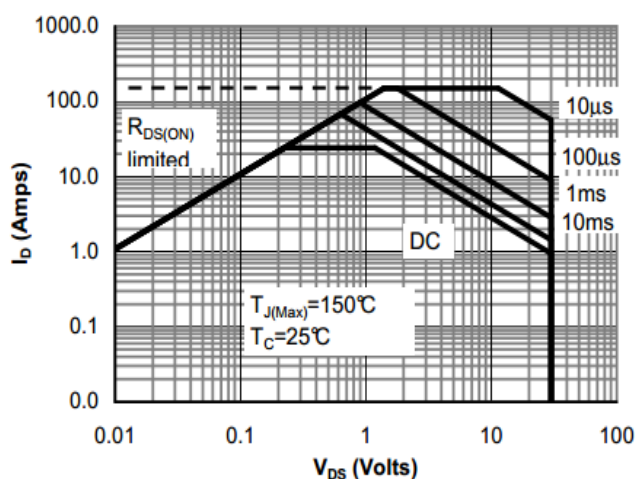


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

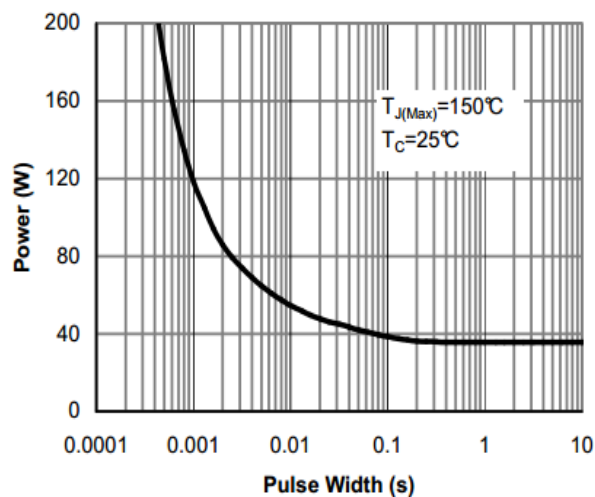


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

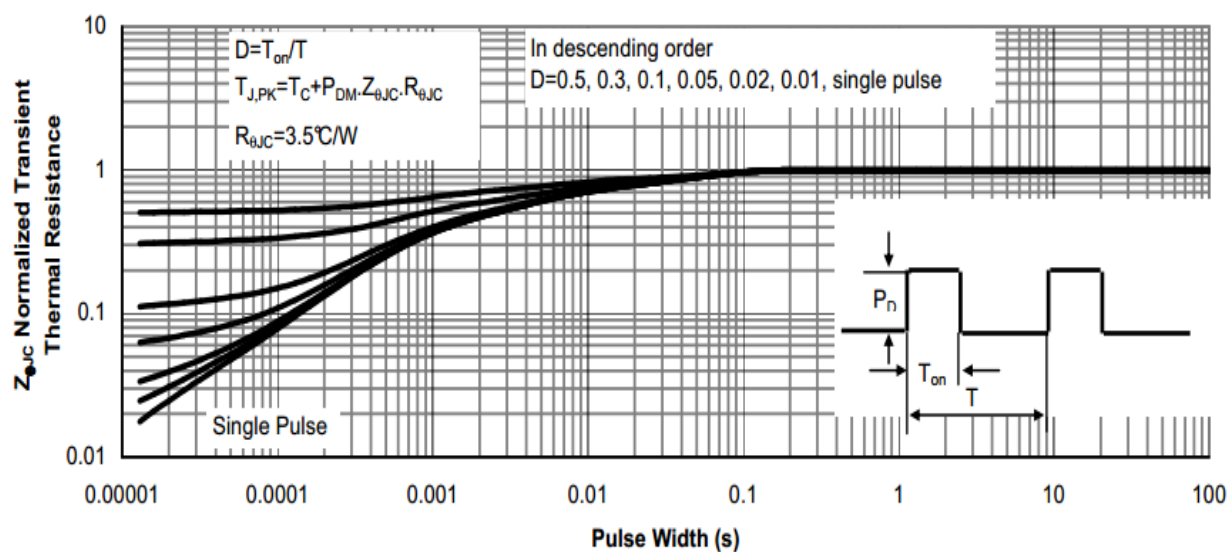
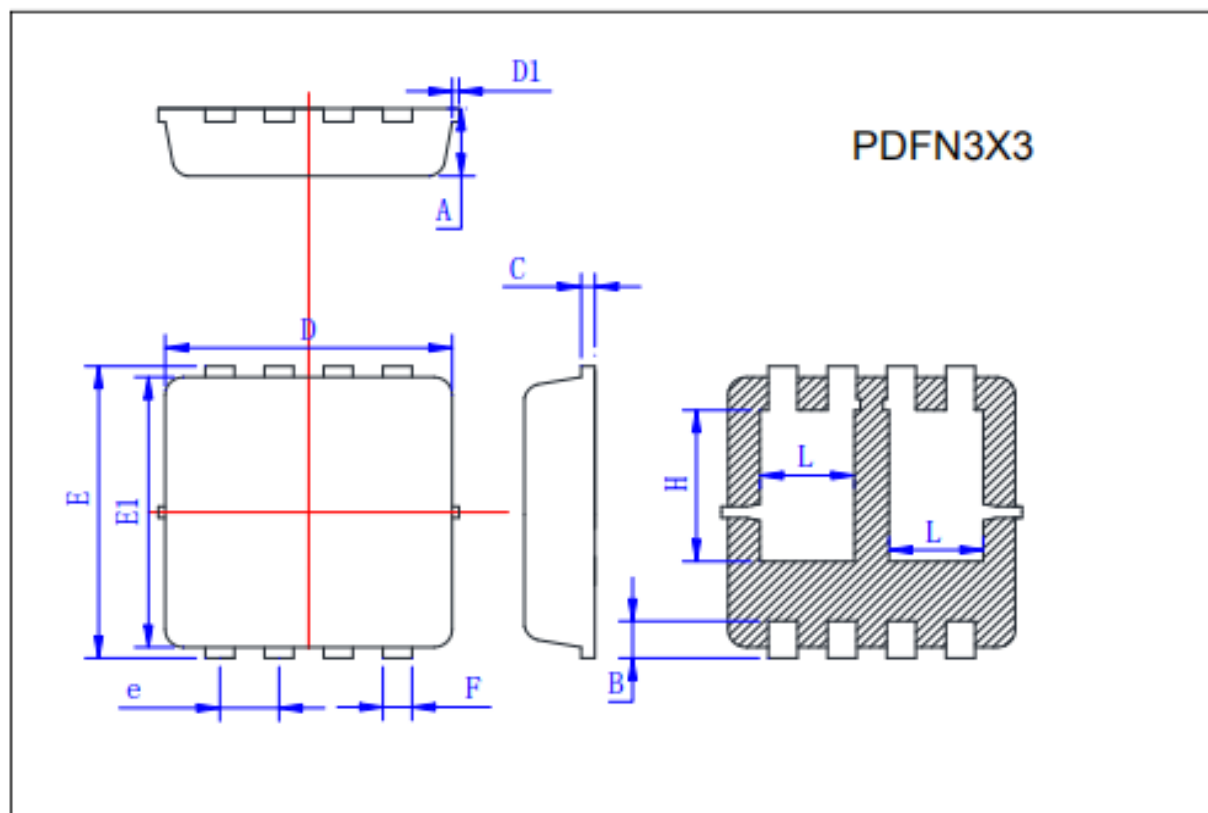


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

PACKAGE OUTLINE DIMENSIONS



Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	0.93	1.03	1.13

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