MT8270

Dual N-Channel Power MOSFET

MT Semiconductor®

http://www.mtsemi.com

General Description

This N-channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain low gate charge for superior switching performance.

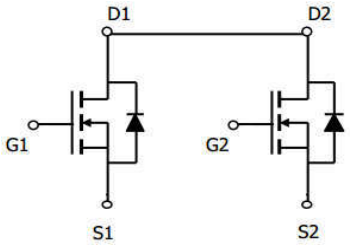
Features

- 20V, 10A $R_{DS(on)}$ = 8.3mΩ @V_{GS} = 4.5V
  $R_{DS(on)}$ = 10.7mΩ @V_{GS} = 2.5V
- Extended V_{GS} range (±10 V) for battery applications
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package

Applications

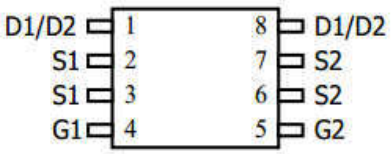
- Load switching
- Battery charge
- Battery disconnect circuits

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT

Top View



TSSOP-8

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current-Continuous	I_D	10	A
Drain Current-Pulsed (Note 1)	I_{DM}	40	A
Maximum Power Dissipation	P_D	1.8	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	83.3	℃/W

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MT8270	MT8270	TSSOP-8	13"	12mm	2500 units

Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=16V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.5	0.7	1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=5A	-	8.3	11	mΩ
		V_{GS}=2.5V, I_D=5A	-	10.7	15.5	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=7A	-	20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=10V,V_{GS}=0V, F=1.0MHz	-	1200	-	PF
Output Capacitance	C_{oss}		-	195	-	PF
Reverse Transfer Capacitance	C_{rss}		-	172	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V,R_L=1.35Ω V_{GS}=5V,R_{GEN}=3Ω	-	5.8		nS
Turn-on Rise Time	t_r		-	15		nS
Turn-Off Delay Time	$t_{d(off)}$		-	51		nS
Turn-Off Fall Time	t_f		-	17		nS
Total Gate Charge	Q_g	V_{DS}=10V,I_D=7A, V_{GS}=4.5V	-	15		nC
Gate-Source Charge	Q_{gs}		-	0.7	-	nC
Gate-Drain Charge	Q_{gd}		-	3.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=1A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	10	A

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

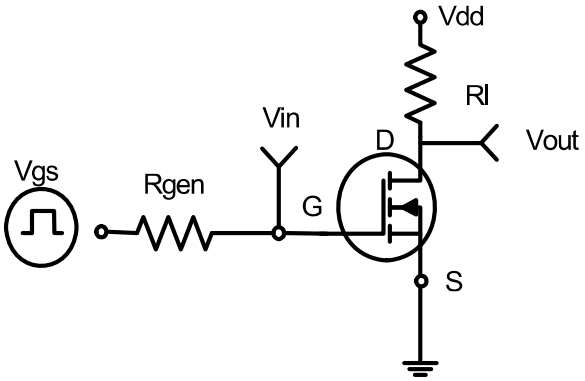


Figure 1:Switching Test Circuit

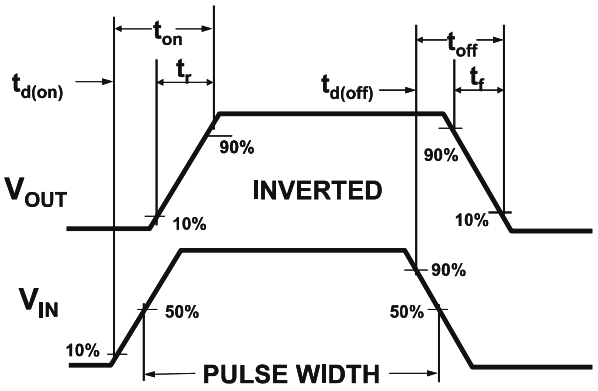


Figure 2:Switching Waveforms

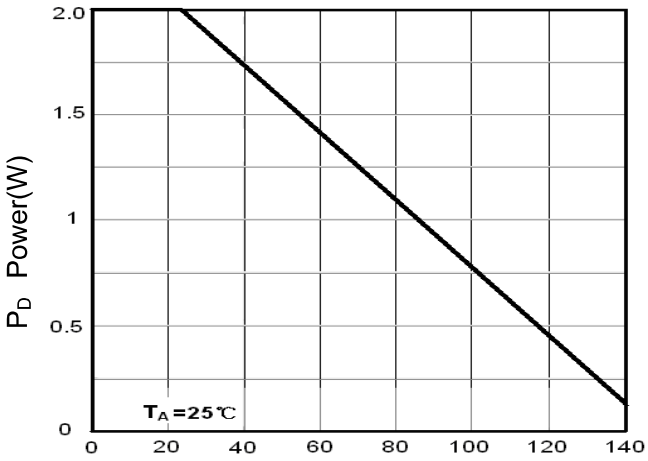


Figure 3 Power Dissipation

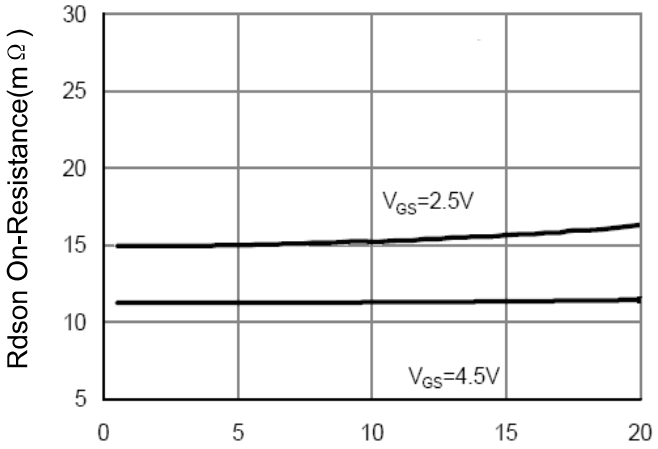


Figure 6 Drain-Source On-Resistance

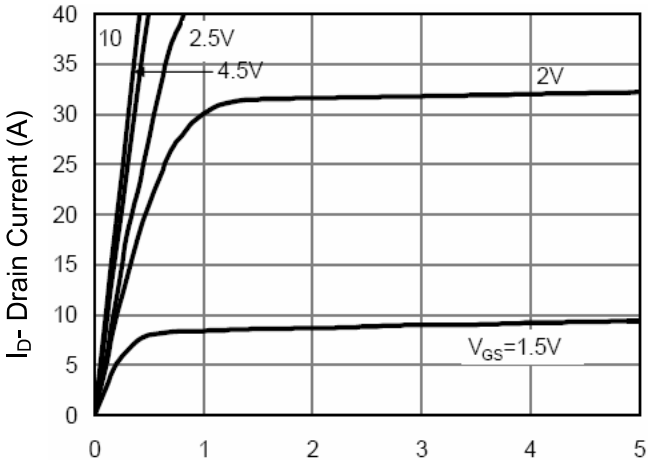


Figure 5 Output Characteristics

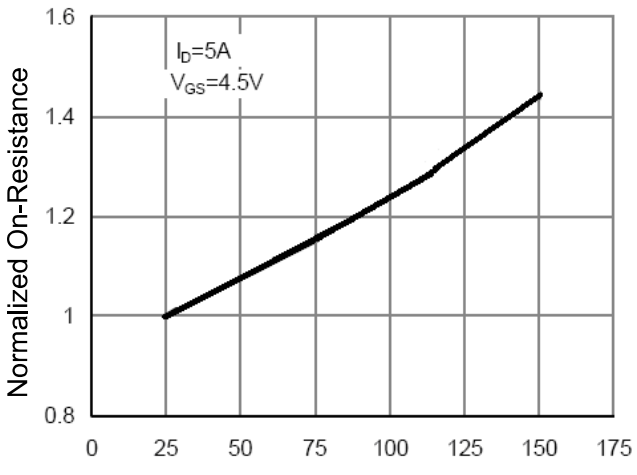


Figure 8 Drain-Source On-Resistance

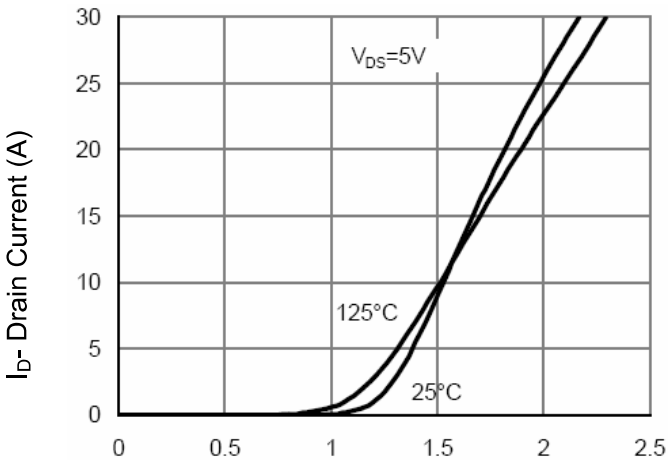


Figure 7 Transfer Characteristics

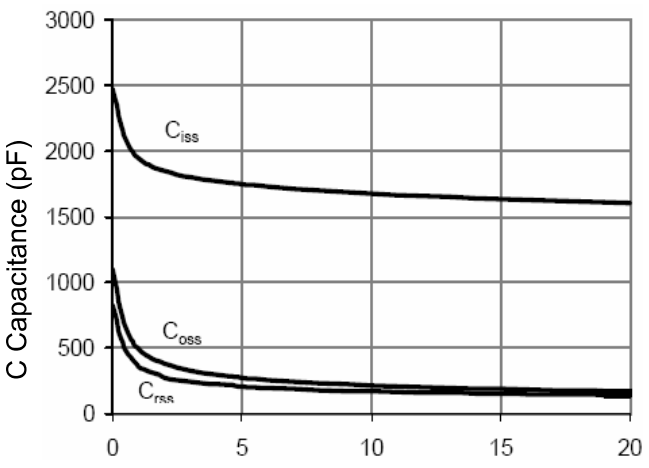


Figure 8 Capacitance vs Vds

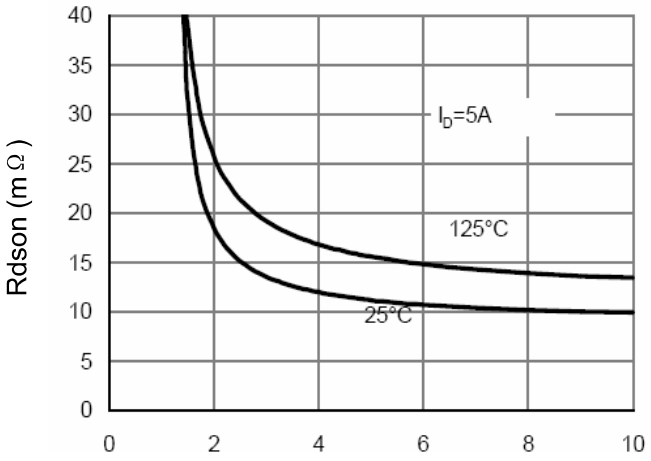


Figure 9 Rdson vs Vgs

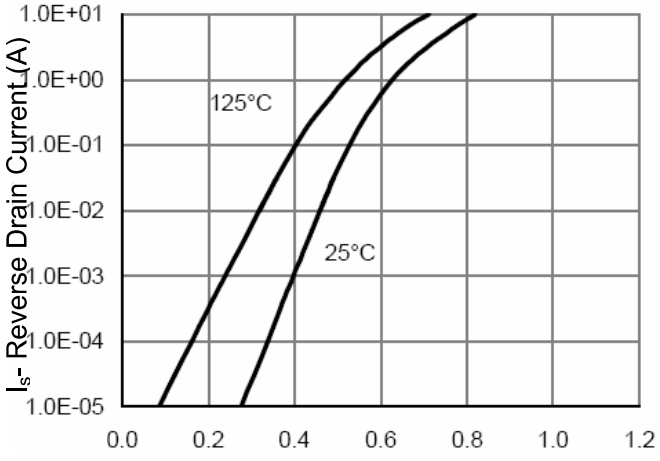


Figure 10Source-DrainDiodeForward

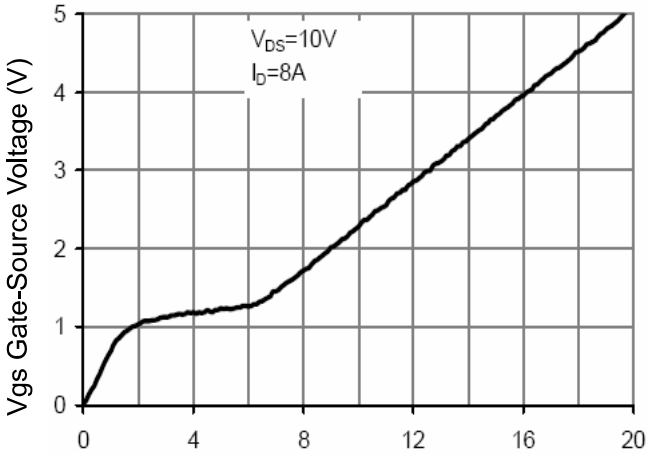


Figure 11 Gate Charge

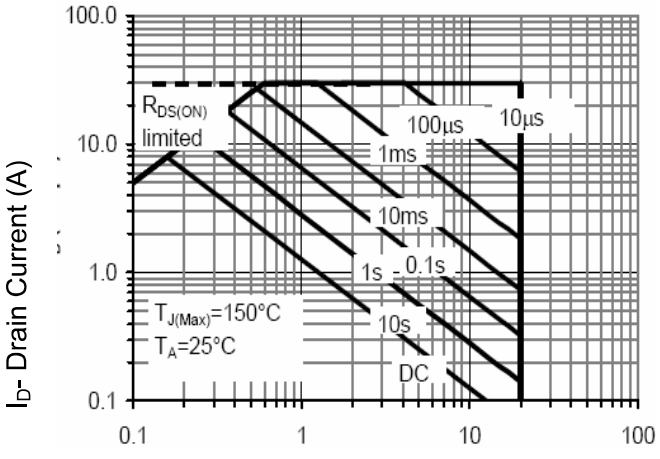


Figure 13 Safe Operation Area

Test Circuits and Waveforms

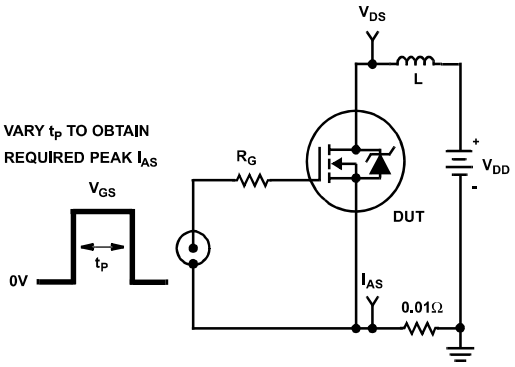


Figure 14. Unclamped Energy Test Circuit

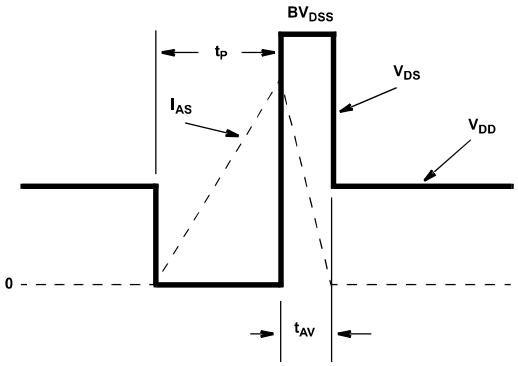


Figure 15. Unclamped Energy Waveforms

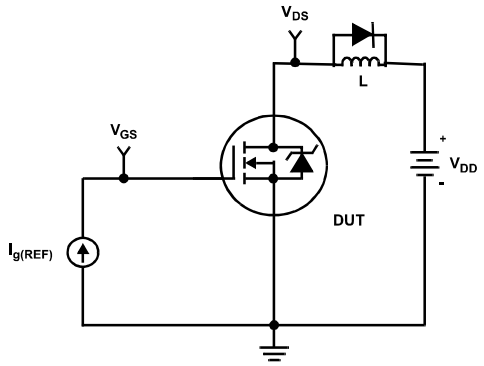


Figure 16. Gate Charge Test Circuit

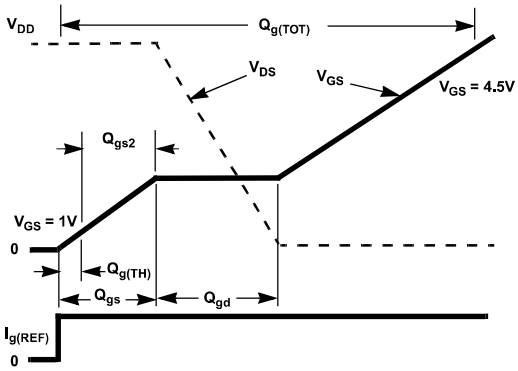


Figure 17. Gate Charge Waveforms

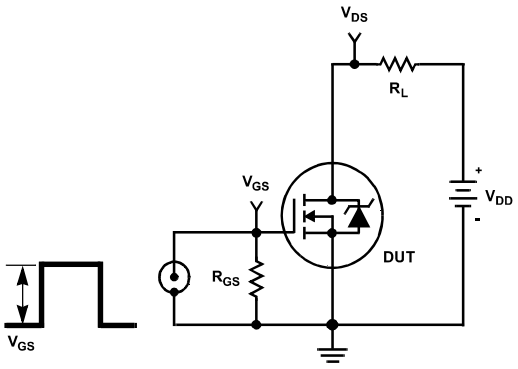


Figure 18. Switching Time Test Circuit

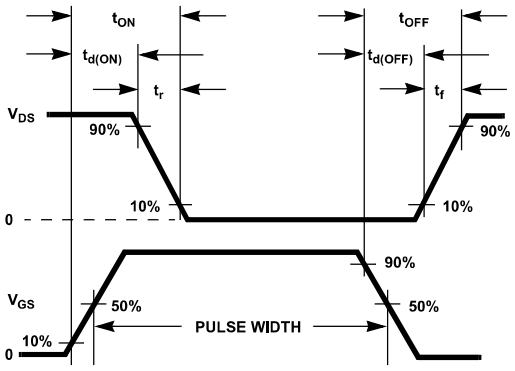
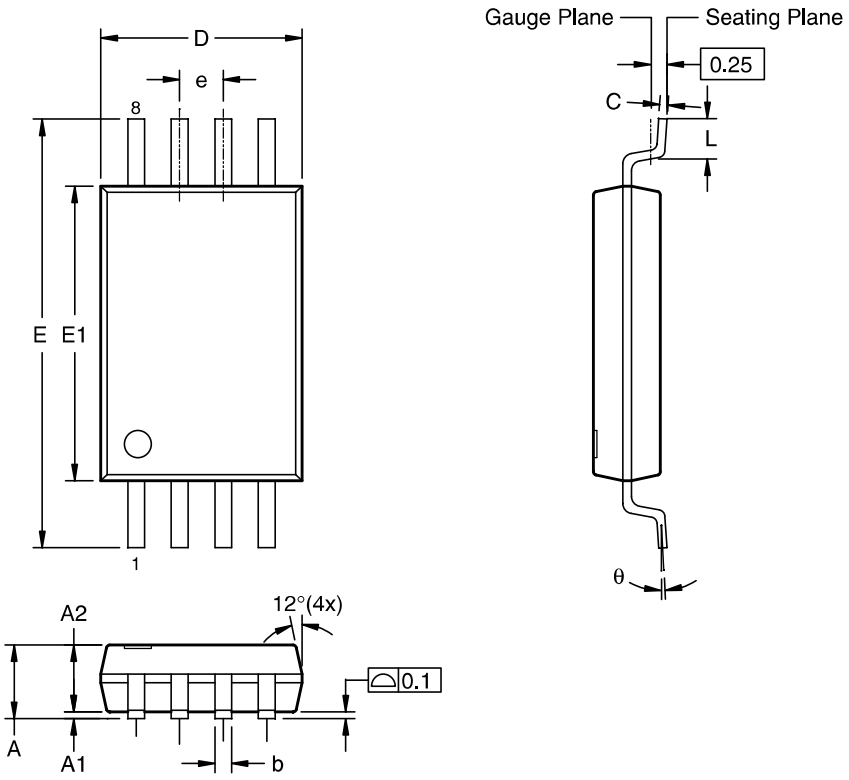
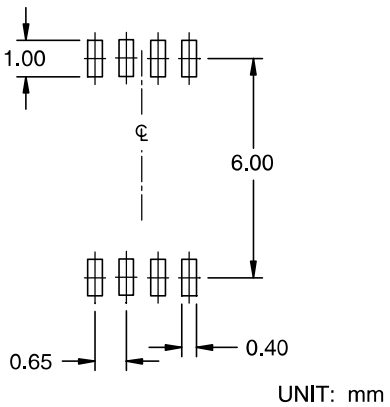


Figure 19. Switching Time Waveforms

TSSOP-8 Package Dimensions



RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	2.90	3.00	3.10
E	6.40 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
L	0.45	0.60	0.75
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	—	—	0.047
A1	0.002	—	0.006
A2	0.031	0.039	0.041
b	0.007	—	0.012
C	0.004	—	0.008
D	0.114	0.118	0.122
E	0.252 BSC		
E1	0.169	0.173	0.177
e	0.026 BSC		
L	0.018	0.024	0.030
θ	0°	—	8°

Notes:

1. All dimensions are in millimeters.
2. Dimensions are inclusive of plating
3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
4. Dimension L is measured in gauge plane.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
6. Refer to JEDEC MO-153(AA).

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