MT8211N3

Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V_{DSS}	I_D	$R_{DS(ON)}$ (mΩ) Typ
20V	8A	14 @ VGS=4.5V
		17 @ VGS=2.5V
		25 @ VGS=1.8V

MT Semiconductor®

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Features

- Super high dense cell design for low RDS(ON).
- Rugged and reliable.
- Suface Mount Package.
- ESD Protected.

General Description

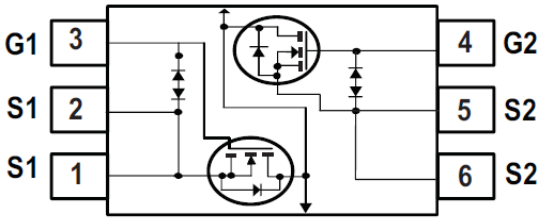
This Dual N-Channel MOSFET is produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Applications

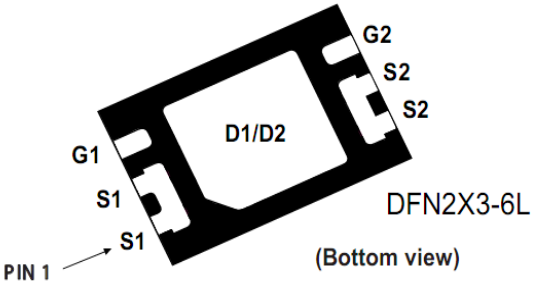
- DC-DC DIVER
- Bank of Power

Simplified Schematic

Bottom Drain Contact (D1/D2)



MARKING DIAGRAM & PIN ASSIGNMENT



DFN2X3-6L

(Bottom view)

ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Symbol	Parameter		Limit	Units
V_{DS}	Drain-Source Voltage		20	V
V_{GS}	Gate-Source Voltage		±12	V
I_D	Drain Current-Continuous [c]	T_A=25°C	8	A
		T_A=70°C	6.4	A
I_{DM}	-Pulsed [a c]		48	A
P_D	Maximum Power Dissipation	T_A=25°C	1.56	W
		T_A=70°C	1.00	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to 150	°C

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	80	°C/W

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V , I_D=250uA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V , V_{GS}=0V			1	uA
I_{GSS}	Gate-Body Leakage Current	V_{GS}= ±8V , V_{DS}=0V			±1	uA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} , I_D=250uA	0.45	0.6	1	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=4.5V , I_D=7.0A		14.0	16.0	m ohm
		V_{GS}=2.5V, I_D=5.5A		17.0	19.0	m ohm
		V_{GS}=1.8V , I_D=5.0A		25.0	30.0	m ohm
g_{FS}	Forward Transconductance	V_{DS}=5V , I_D=4A		35		S
DYNAMIC CHARACTERISTICS [b]						
C_{ISS}	Input Capacitance	V_{DS}=10V,V_{GS}=0V f=1.0MHz		705		pF
C_{OSS}	Output Capacitance			235		pF
C_{RSS}	Reverse Transfer Capacitance			218		pF
SWITCHING CHARACTERISTICS [b]						
$t_{D(ON)}$	Turn-On Delay Time	V_{DD}=10V I_D=1A V_{GS}=4.5V R_{GEN}=6 ohm		25		ns
tr	Rise Time			89		ns
$t_{D(OFF)}$	Turn-Off Delay Time			110		ns
tf	Fall Time			102		ns
Q_g	Total Gate Charge	V_{DS}=10V,I_D=4A,V_{GS}=4.5V		13.4		nC
		V_{DS}=10V,I_D=4A,V_{GS}=2.5V		10.2		nC
Q_{gs}	Gate-Source Charge	V_{DS}=10V,I_D=4A, V_{GS}=4.5V		2		nC
Q_{gd}	Gate-Drain Charge			6		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
V_{SD}	Diode Forward Voltage	V_{GS}=0V,I_S=1A		0.75		V

Notes

a.Pulse Test:Pulse Width ≤ 10us, Duty Cycle ≤ 1%.
b.Guaranteed by design, not subject to production testing.
c.Drain current limited by maximum junction temperature.
d.Mounted on FR4 Board of 1 $inch^2$, 2oz.

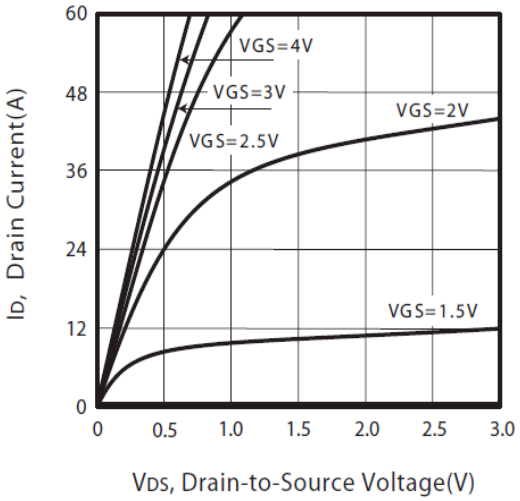


Figure 1. Output Characteristics

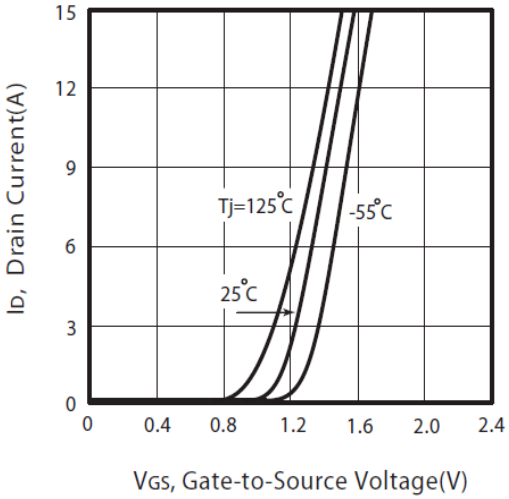


Figure 2. Transfer Characteristics

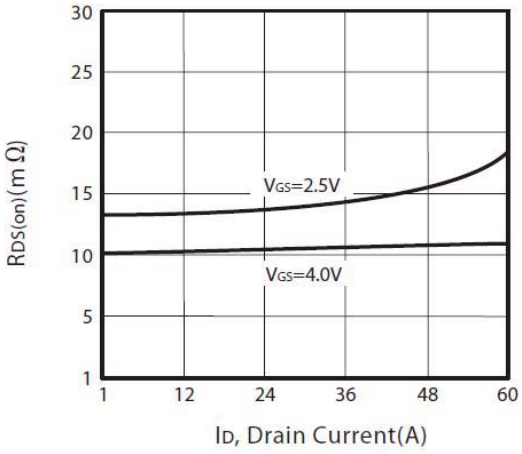


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

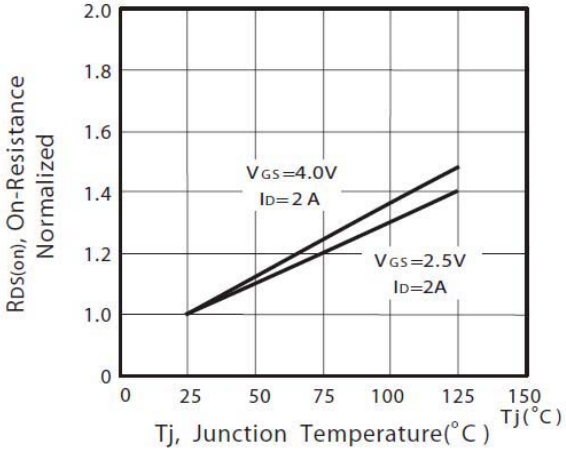


Figure 4. On-Resistance Variation with Drain Current and Temperature

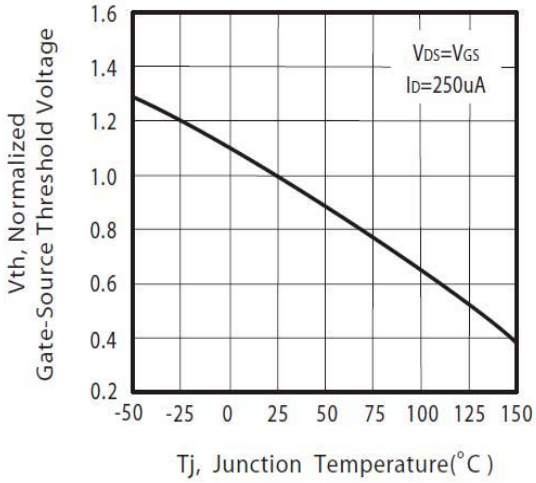


Figure 5. Gate Threshold Variation with Temperature

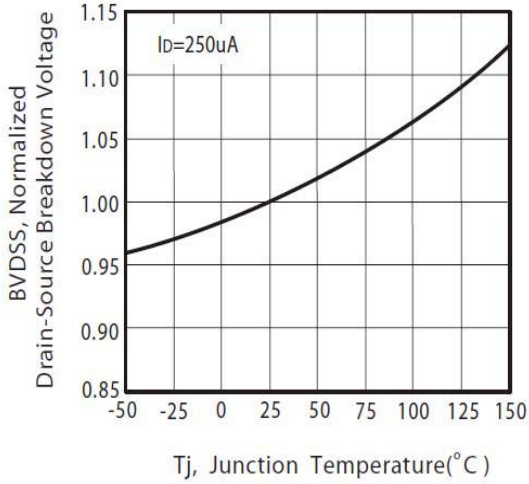


Figure 6. Breakdown Voltage Variation with Temperature

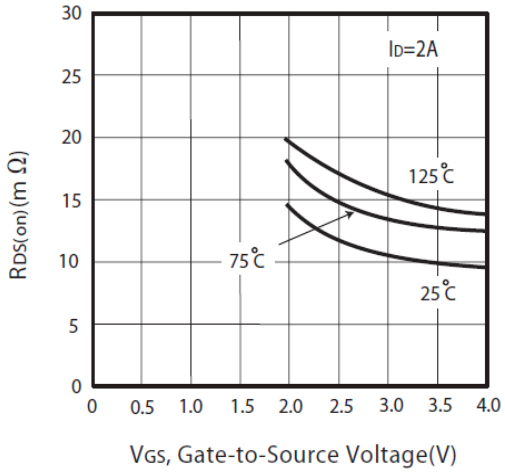


Figure 7. On-Resistance vs. Gate-Source Voltage

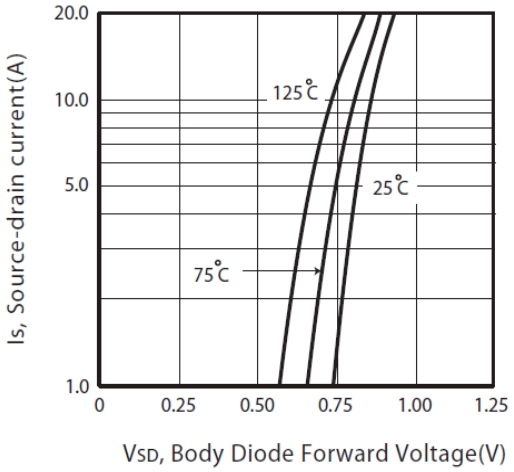


Figure 8. Body Diode Forward Voltage Variation with Source Current

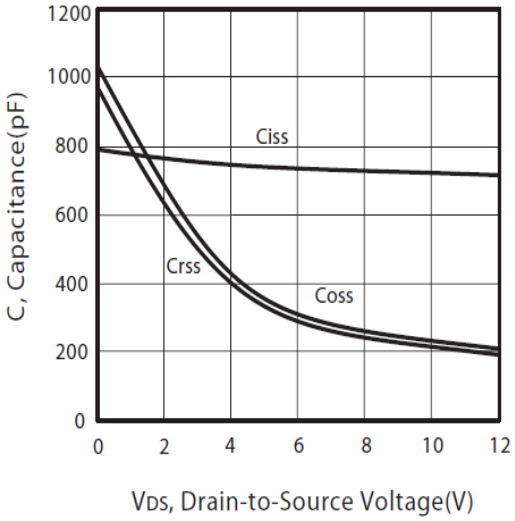


Figure 9. Capacitance

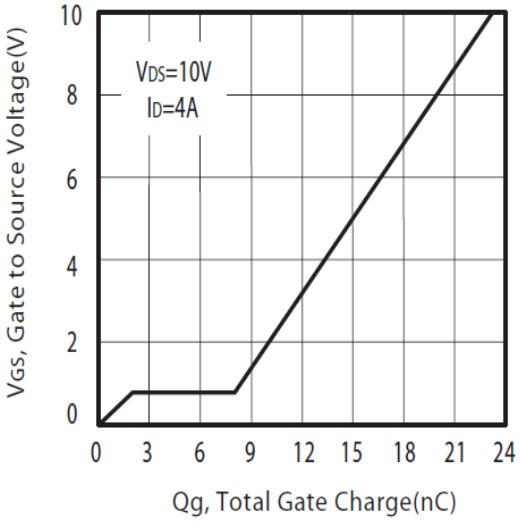


Figure 10. Gate Charge

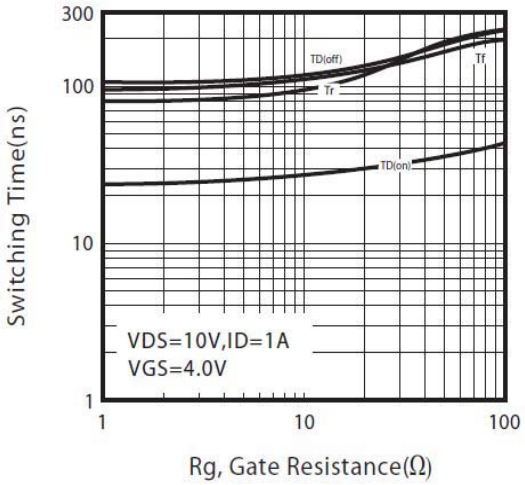


Figure 11. switching characteristics

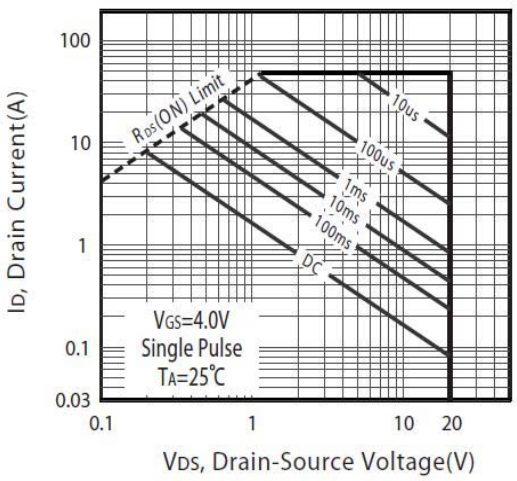
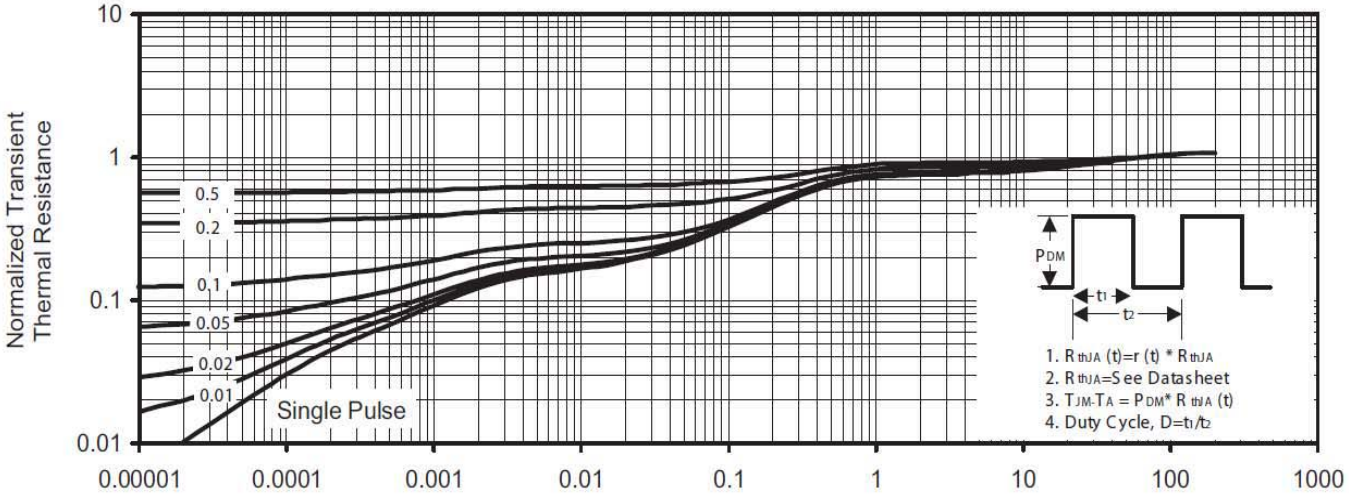


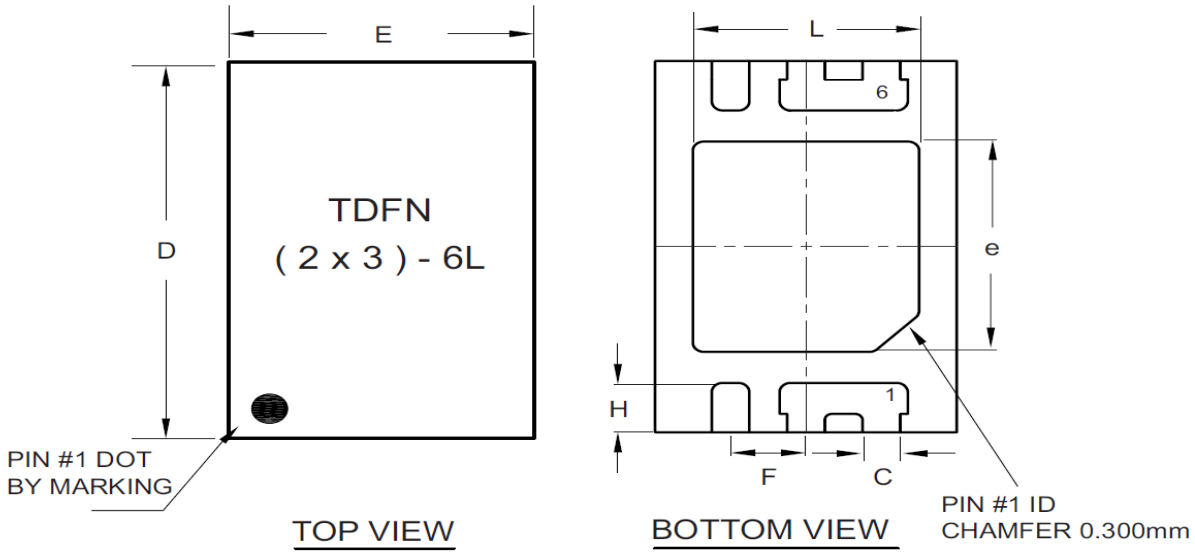
Figure 12. Maximum Safe Operating Area

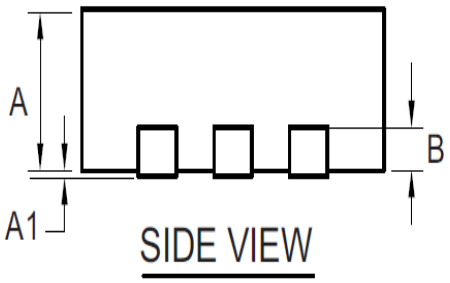


Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS

TDFN





SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
D	2.950	3.050	0.116	0.120
E	1.950	2.050	0.077	0.081
H	0.350	0.450	0.014	0.018
L	1.450	1.550	0.057	0.061
e	1.650	1.750	0.065	0.069
B	0.195	0.211	0.0076	0.008
C	0.200	0.300	0.008	0.012
F	0.500 BSC		0.020 BSC	

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