

# MT8103

## P-Channel Enhancement Mode Field Effect Transistor

### Product Summary

- $V_{DS} = -30V$
- $I_D = -13A$  ( $V_{GS} = -10V$ )
- $R_{DS(ON)} = 10m\Omega$  @  $V_{GS} = -10V$
- $R_{DS(ON)} = 14m\Omega$  @  $V_{GS} = -4.5V$

### Features

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Lead free product is acquired
- RoHS compliant

### Applications

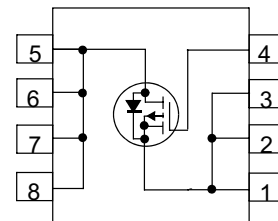
- Notebook computer
- Portable battery backs



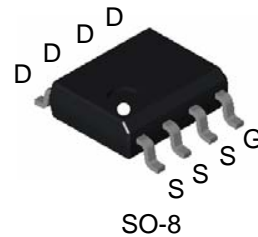
**MT Semiconductor®**

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### Simplified Schematic



### MARKING DIAGRAM & PIN ASSIGNMENT



### Absolute Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	10s	Steady State	Units
$V_{DS}$	Drain-Source Voltage		-30	V
$V_{GS}$	Gate-Source Voltage		$\pm 20$	V
$I_D$	Continuous Drain Current <sup>1</sup>	-13	-9	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>		-50	A
$I_S$	Continuous Source Current (Diode Conduction) <sup>1</sup>	-2.7	-1.36	A
$P_D$	Maximum Power Dissipation <sup>1</sup>	3.0	1.5	W
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range		-55 to 150	$^\circ C$

### Thermal Resistance Ratings

Symbol	Parameter		Typical	Maximum	Unit
$R_{thJA}$	Maximum Junction-to-Ambient <sup>1</sup>	$t \leq 10$ Sec	33	42	$^\circ C/W$
		Steady State	70	82	

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

## Electrical Characteristics (T<sub>A</sub>=25°C, unless otherwise noted)

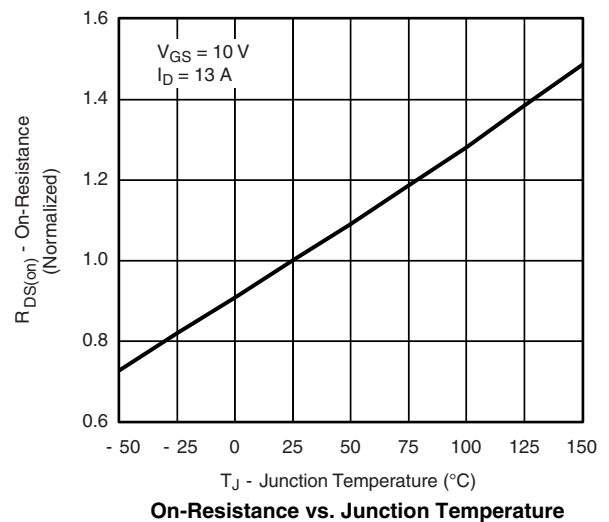
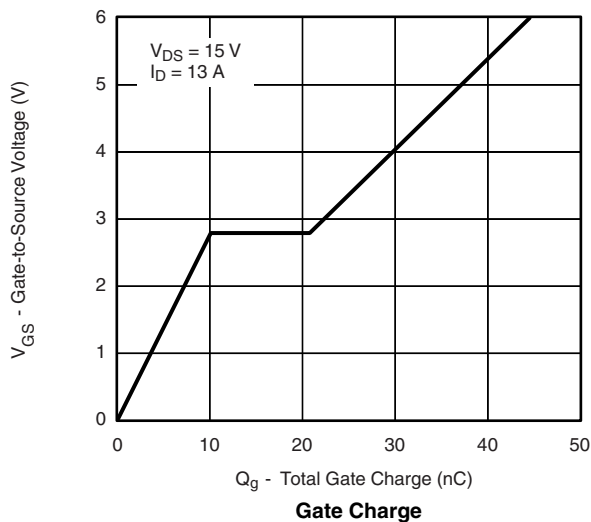
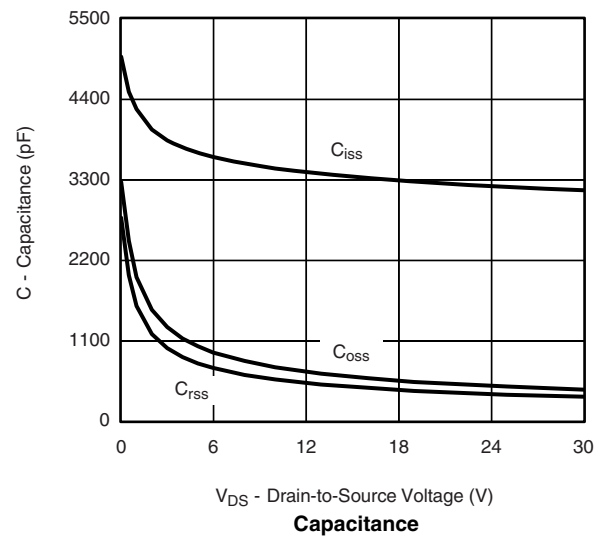
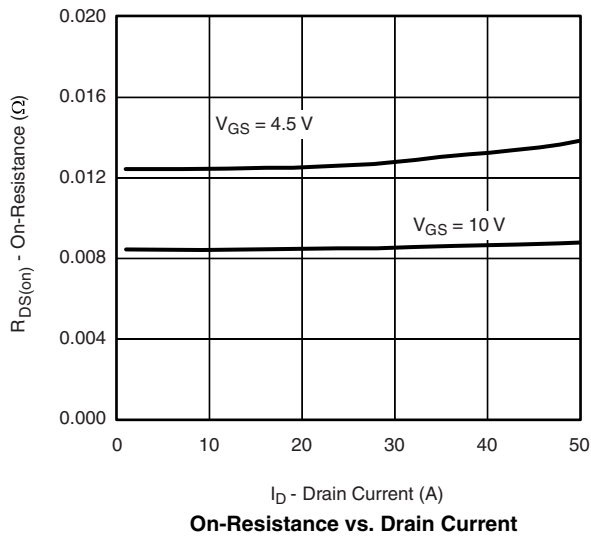
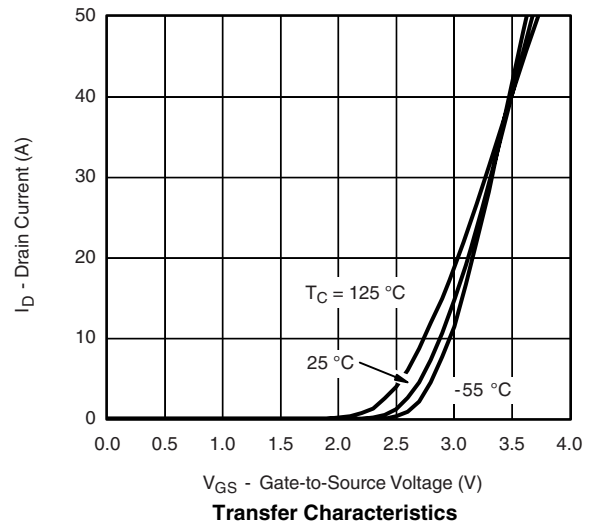
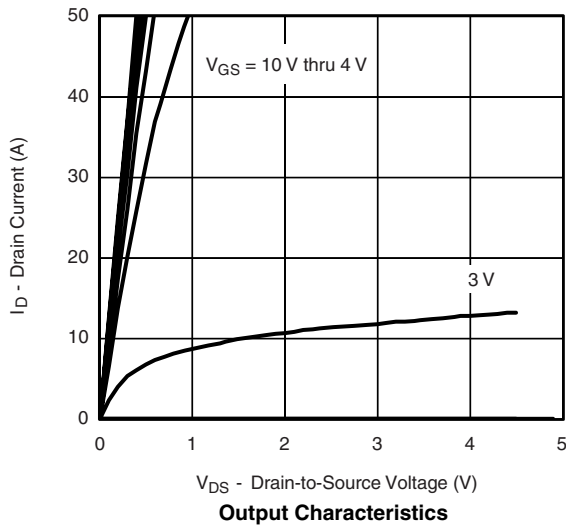
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>● Static Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA	-30	-	-	V
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250μA	-1.0	-1.5	-3.0	V
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V	-	-	±100	nA
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V	-	-	-1	μA
		V <sub>DS</sub> = -24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 70°C		-	-10	
R <sub>DS(on)</sub>	Drain Source On State Resistance <sup>a</sup>	V <sub>GS</sub> = -10V, I <sub>D</sub> = -13A	-	10	12	mΩ
		V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -10A	-	14	16	
g <sub>fs</sub>	Forward Transconductance <sup>a</sup>	V <sub>DS</sub> = -15V, I <sub>D</sub> = -13A	-	40	-	S
V <sub>SD</sub>	Diode Forward Voltage <sup>a</sup>	I <sub>S</sub> = -2.7A, V <sub>GS</sub> = 0V	-	-0.74	-1.1	V
<b>● Dynamic Characteristics <sup>b</sup></b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = -15V, V <sub>GS</sub> = 0V, f = 1MHz	-	3340.0	-	pF
C <sub>oss</sub>	Output Capacitance		-	577.0	-	
C <sub>rss</sub>	Reverse Transfer Capacitance		-	426.0	-	
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = -15V, V <sub>GS</sub> = -5V, I <sub>D</sub> = -13A	-	37.0	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	10.0	-	
Q <sub>gd</sub>	Gate-Drain Charge		-	11.0	-	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = -15V, R <sub>L</sub> = 15Ω I <sub>D</sub> = -1A, V <sub>GEN</sub> = -10V, R <sub>G</sub> = 6Ω	-	19.5	-	nSec
t <sub>r</sub>	Rise Time		-	10.0	-	
T <sub>d(off)</sub>	Turn-Off Delay Time		-	137.5	-	
t <sub>f</sub>	Fall Time		-	55.3	-	
R <sub>g</sub>	Gate Resistance	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0, f = 1MHz	-	3.4	-	Ω
t <sub>rr</sub>	Source-Drain Reverse Recovery Time	I <sub>F</sub> = -2.1A, di/dt = 100A/μs	-	60	100	nSec

Note:

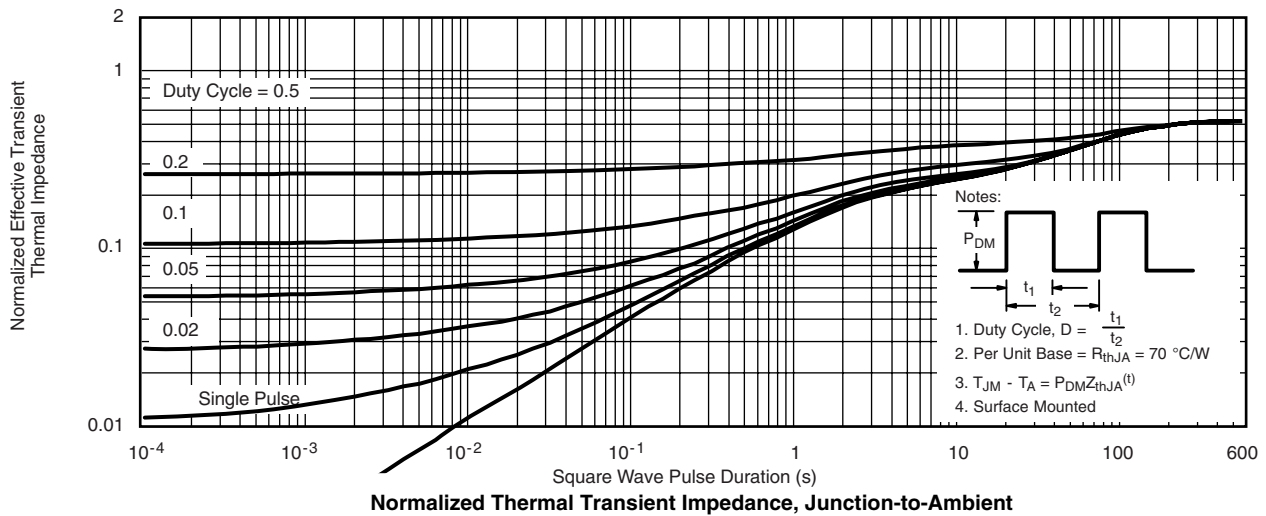
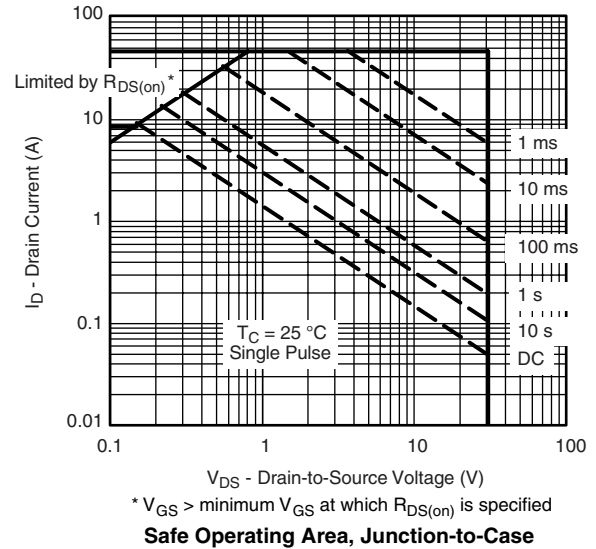
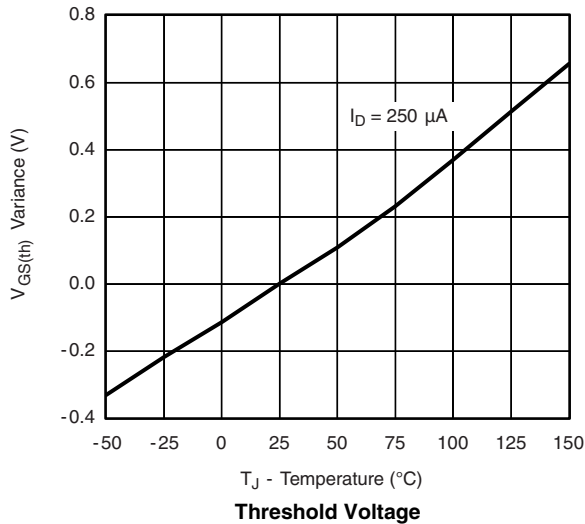
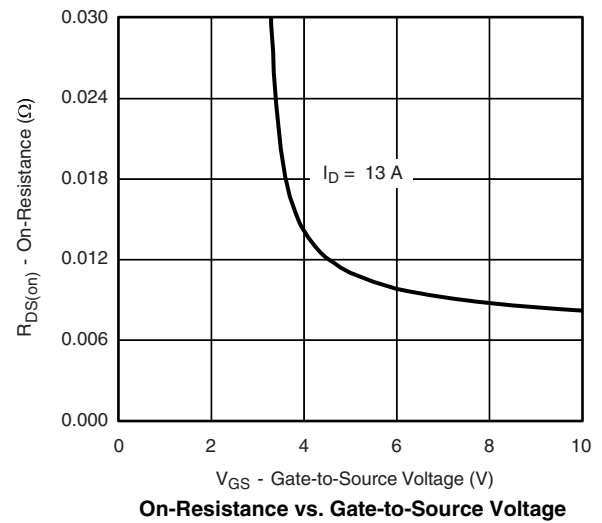
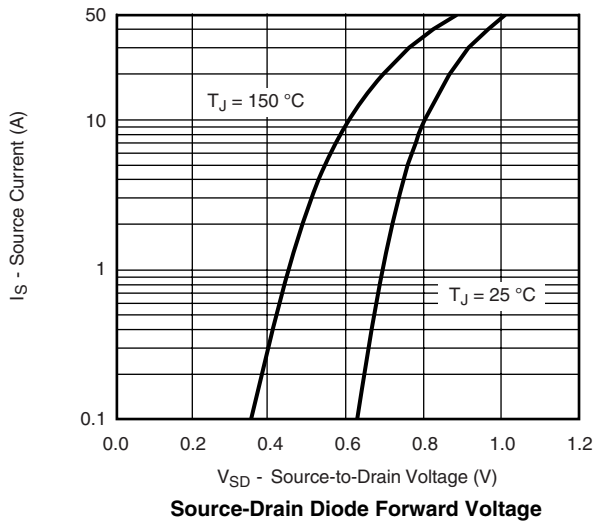
a. Pulse test; pulse width ≤ 300μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

## Characteristics Curve ( $T_A=25^\circ\text{C}$ , unless otherwise noted)



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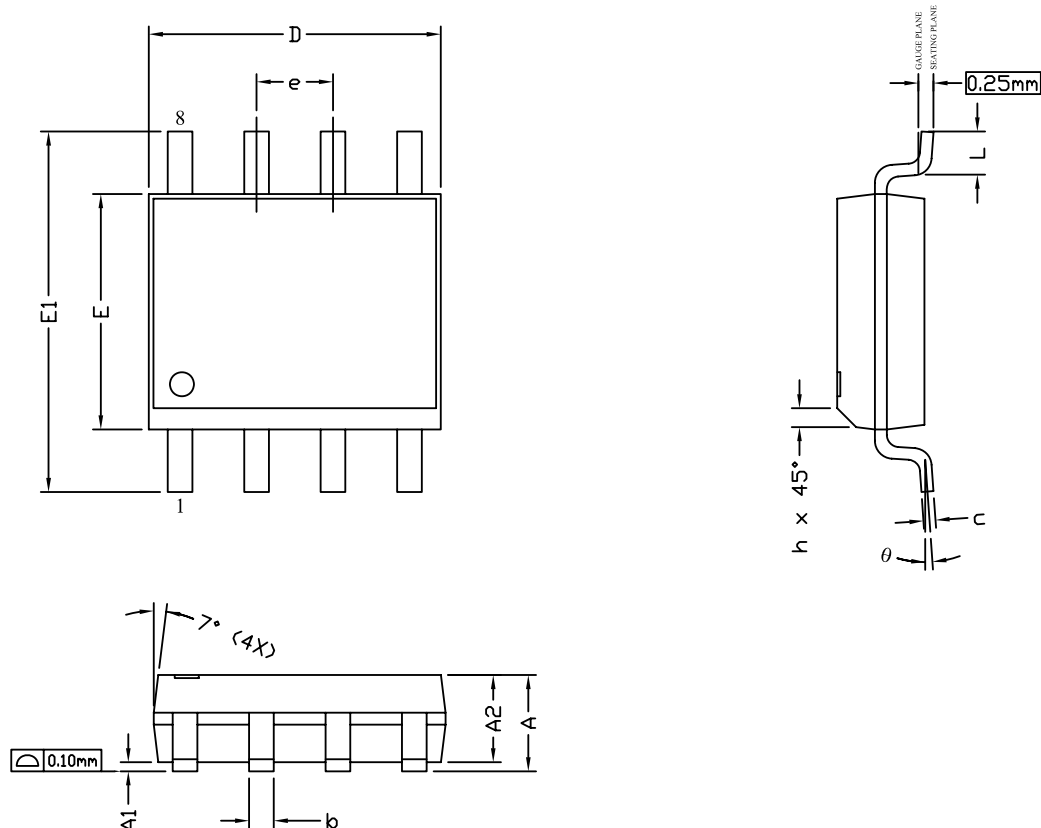
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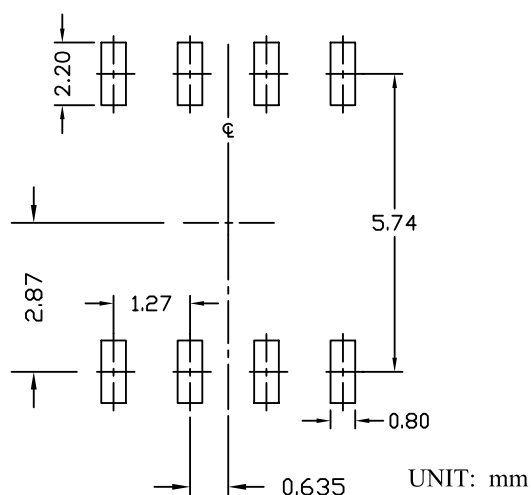
Version

rev H

## S08 PACKAGE OUTLINE



## RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
$\theta$	$0^\circ$	—	$8^\circ$	$0^\circ$	—	$8^\circ$

## NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.  
CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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