MT6605 Data Sheet

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Document Revision History

Revision	Date	Author	Description
0.1	2012-09-07	Chun-Yi Wu	Initial Draft
0.2	2012-09-20	Chun-Yi Wu / Wee Liang Lien	Add pin definition
0.3	2012-09-23	Chee Lee Heng / Mark Choke / Wee Liang Lien	Added sections related to RX, TX and SX
0.4	2012-09-24	Chun-Yi Wu	Update chip diagram, feature section
0.5	2013-03-22	Junwei Lin	Update the chip package and top mark
0.6	2013-04-25	Junwei Lin	Add ordering information
0.7	2013-07-31	Wee Liang Lien / Chee Lee Heng / Mark Choke / Ming Kong	Update chip overall block diagram. Update pin names for consistency.
1.0	2013-08-05	Junwei	Remove “internal use”, ”draft version” from front page. Change some wording in general description.
1.1	2013-09-05	Junwei	Unify the table format. Remove Flash version package.
1.2	2013-11-14	Junwei	Update VABT spec in section 8.2.2

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1 Top Level Overview

1.1 General description

The MediaTek® MT6605 single chip SoC provides full range of 13.56MHz contactless protocols, small footprint, optimized RF performance and power management for variety of NFC applications on mobile, computing and consumer electronics. MT6605 is compliant to NFC Forum, EMVCo, ISO 10373-6, ETSI SWP/HCI and China domestic standards and has been tested with ecosystem key players and infrastructure to ensure interoperability. With highly integrated software package, MT6605 total solution can save design cost, shorten time-to-market and easily customize for differentiation.

MT6605 has 2 unique designs to enable NFC market eco-system. For payment, it can support up to 2 UICC and 1 Micro SD or Embedded Secure Element through the Single-Wire Protocol (SWP) interfaces. For No-payment, its pre-installed application Beam Plus helps the user to easily tap and share information 2 times faster by optimized WiFi / BT and NFC connection handover.

1.2 Features

- Reader Features(106K-848Kbits/s)
  - Support ISO 15693
  - Support ISO 14443A
  - Support ISO 14443B, B'
  - Support ISO 18000-3
  - Support NFC Forum Type1-4 Tag
  - Support Kovio
- Card Emulation Mode(106K-848Kbits/s)
  - Support ISO 14443A
  - Support ISO 14443B, B'
  - Support NFC Forum Type1-4 Tag
  - Support Mifare via CLT
  - Support FeliCa RF
- Near Field Communication(106K-424Kbits/s)
  - Peer to Peer Active/Passive mode
  - ISO18092 compliant
- Reference oscillator
  - Internal 27.12 MHz oscillator to support single pin crystal connection
  - Integrated Frac-N PLL which supports multiple external reference clock frequencies of 19.2, 20, 24, 26, 27.12, 38.4, 40 & 52 MHz
  - Co-clock on MediaTek platform
- Processor
  - 16 bits CPU Core
  - NVM independent power domain
  - RAM:48KB, ROM:75.75KB, NVM: 17.5K
- Serial interface
  - UART: 4800bps~921600bps
  - SPI: 2Mbps
  - I2C: Fast mode (400Kbps) / High Speed Mode (3.4 Mbps)
  - SWP : 1.69Mbps (Release 9.2.0)
- Compliance
  - NFC Forum Wave 1 and Wave 2
  - EMVCo 2.0.1 PICC and PCD
  - Visa Paywave and MasterCard Paypass
  - China UnionPay QuickPass
  - ISO 10373-6
  - ETSI/SCP SWP and HCI
  - GSMA
- Package (QFN32)
  - 4mm x 4mm x 0.8mm

2 Pin Assignment and Descriptions

2.1 Pin assignment (top view)

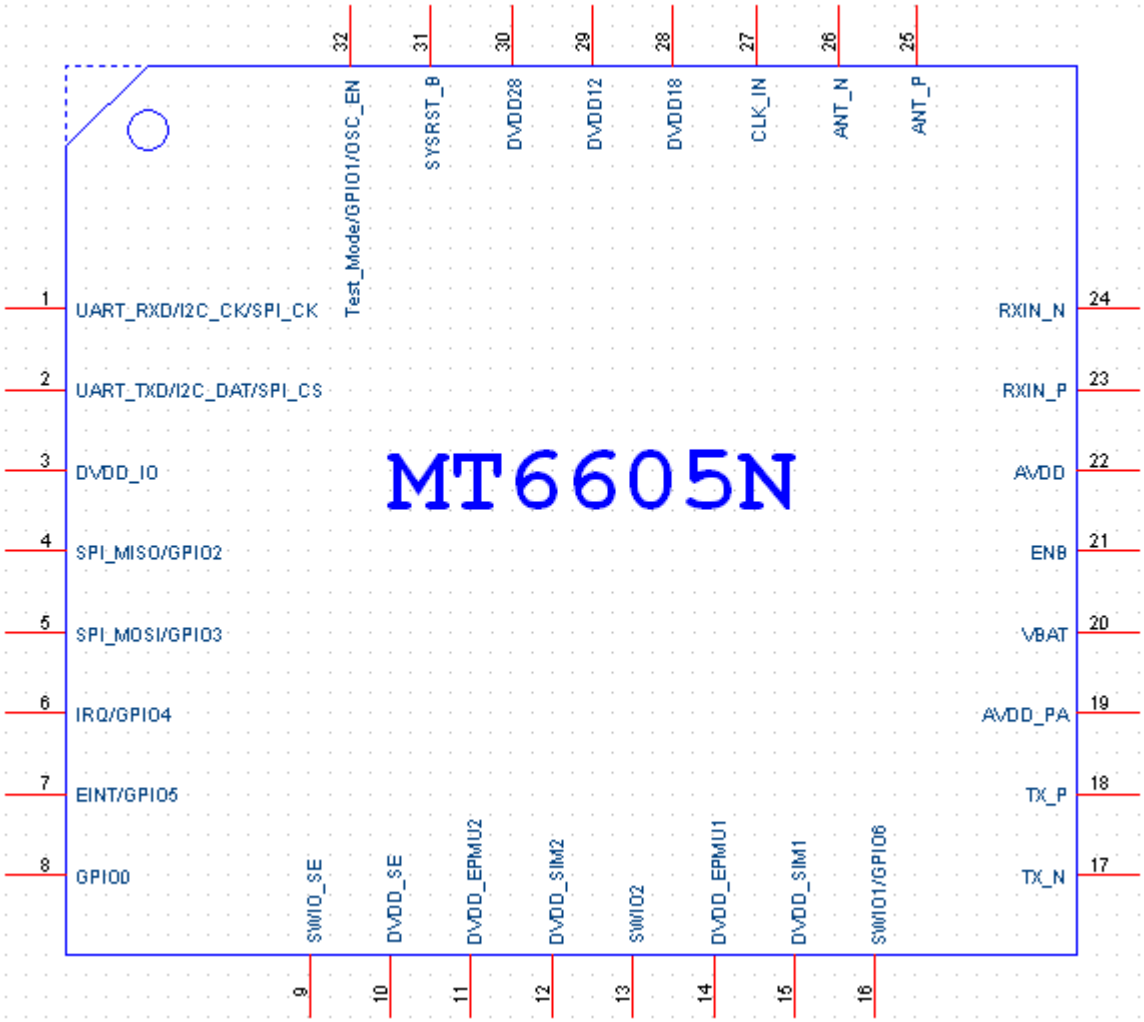


Figure 2-1: MT6605 QFN 4mmx4mm pin-out

2.2 Pin descriptions

Pin#	Name	Type	Description
Digital Peripheral interface (4 pins)			
1	UART_RXD/I2C_CK/SPI_CK	I/O	Serial input for UART/I2C_CK/SPI_CK Default: pull-up Default: 2mA driving
2	UART_TXD/I2C_DAT/SPI_CS	I/O	Serial output for UART/I2C_DAT/SPI_CS Default: pull-up Default: 2mA driving
4	SPI_MISO/GPIO2	I/O	Serial output for SPI_Data Default: pull-down Default: 2mA driving Strap pin : eclk_sel
5	SPI_MOSI/GPIO3	I/O	Serial input for SPI_Data Default: pull-down Default: 2mA driving
Digital system interface (5 pins)			
21	ENB	I/O	System enable. Active low
31	SYSRST_B	input	System reset. Active low Default: pull-up
32	TEST_MODE/GPIO1/OSC_EN	I/O	Test mode enable/GPIO1/OSC_EN 1: test mode. 0: normal mode. Default: pull-down Strap pin osc_en
6	IRQ/GPIO4	I/O	TX request indicator/GPIO4 Default: pull-down Default: 2mA driving Strap pin: host_sel[1]
7	EINT/GPIO5	I/O	External interrupt Default: pull-down Default: 2mA driving
Digital debug interface (1 pins)			
8	GPIO0	I/O	GPIO Default: pull-down Default: 2mA driving Strap pin: host_sel[0]
SWP			
9	SWIO_SE	I/O	SWP IO for SE/microSD
13	SWIO2	I/O	SWP IO 2
16	SWIO1/GPIO6	I/O	SWIO IO 1
PMU			
3	DVDD_IO	Power input	External host VDD (2.8V/1.8V)
10	DVDD_SE	Power output	Output VDD for microSD, eSE (1.8V)
11	DVDD_EPMU2	Power input	External PMU2 VDD (3V/1.8V)
12	DVDD_SIM2	Power output	Output VDD for SIM2 (1.8V)

14	DVDD_EPMU1	Power input	External PMU1 VDD (3V/1.8V)
15	DVDD_SIM1	Power output	Output VDD for SIM1 (1.8V)
19	AVDD_PA	Power output	LDO output for LDO PA
20	VBAT	Power input	Battery voltage (4.3V)
22	AVDD	Power output	Rectifier output (2.6V)
28	DVDD18	Power output	Secure element power supply output (1.8V)
29	DVDD12	Power output	Baseband power supply output (1.2V)
30	DVDD28	Power input	LDO input for SRAM data retention (2.8V)
RF & analog			
17	TX_N	Analog output	Transmitter output negative terminal
18	TX_P	Analog output	Transmitter output positive terminal
23	RX_IN_P	Analog input	Receiver input positive terminal
24	RX_IN_N	Analog input	Receiver input negative terminal (optional)
25	ANT_P	Analog input	Rectifier input positive terminal
26	ANT_N	Analog input	Rectifier input negative terminal
27	CLK_IN	Digital input	27.12MHz XO input or co-clock

Table 2-1: pin description

2.3 Strap function

TEST_MODE	SPI_MISO	IRQ	GPIO0	Function
0		**0**	**1**	UART without baud detect
0		**1**	**0**	UART with baud detect
0		**0**	**0**	I2C
0		**1**	**1**	SPI
0	**0**			Use self clock
0	**1**			Co-clock (26M)

Table 2-2: strap definition

3 Block Diagrams

3.1 Chip overall block diagram

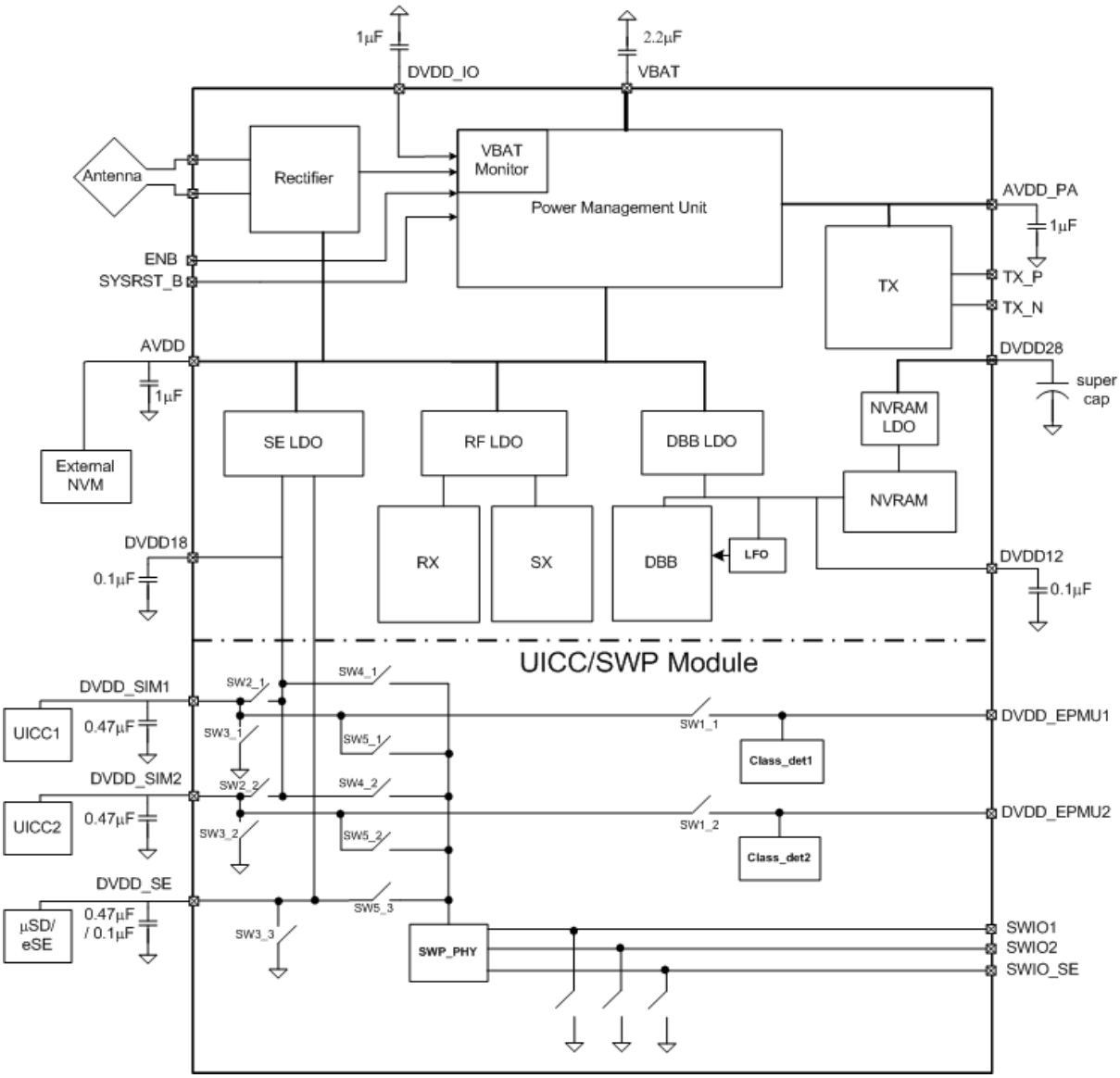


Figure 3-1: MT6605 functional blocks

The block diagram of MT6605 is illustrated in Figure 3-1. MT6605 comprises of 7 main blocks: RX, TX, SX, SWP, Baseband, power harvester and the power management unit (PMU).

This direct conversion RX directly translates the received PCD or PICC signal to base-band frequencies for digital demodulation.

The TX section has a high efficiency PA to provide modulated signals during the PCD mode.

In the SX section, the Low Frequency Oscillator (LFO) will be enabled when AVDD26 is available. The LFO generates 300KHz clock to Digital Baseband (DBB) and is the main clock source during sleep and low power polling. A frac-N PLL generates 13.56MHz clock for RF field generation and DBB during PCD mode. A PLL clock recovery which synchronizes to the clock source from the field generates the 13.56MHz clock to receiver and DBB.

The single-wire protocol (SWP) section provides the infrastructure to support up to 2 UICC cards and 1 microSD or secure element (SE).

The PMU section comprises of various low dropout regulators (LDOs) for power supply noise suppression and voltage regulation.

The Baseband section is the main controller to the RF, PMU and SWP section and also contains the MODEM, coding and decoding functions.

The power harvesting section enables MT6605 to perform card emulation during the absence of battery. The power will be harvested from the field.

3.2 Functional Block Diagram (Digital Part)

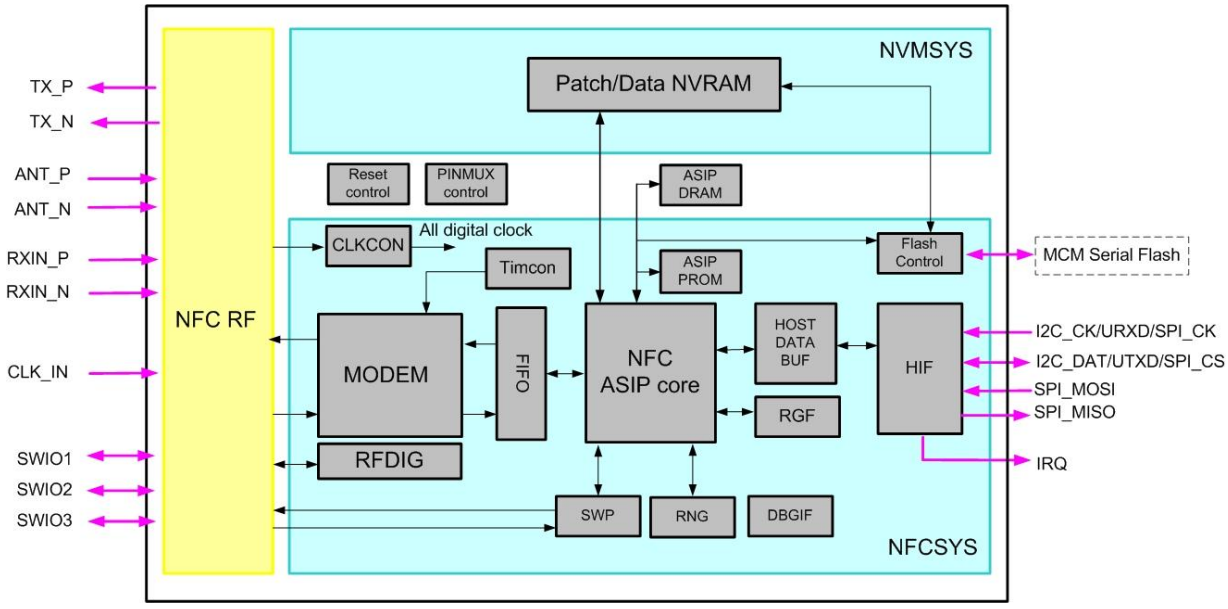


Figure 3-2: MT6605 digital block diagram

3.3 Functional Block Diagram (RF part)

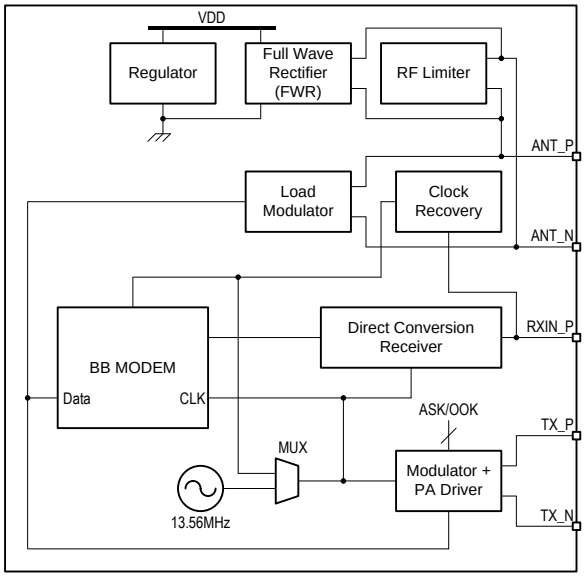


Figure 3-3: RF function block diagram

During PCD mode, the PA Driver will transmit modulated signals and receive the load modulated signals from the PICC through the direct conversion receiver.
During PICC mode, clock is extracted from the field and recovered by the clock recovery circuit. TX is performed through load modulation at the ANT_P and ANT_N pins. The RF limiter circuit prevents the chip from “overharvesting field power” and regulates the voltage through shunting additional currents to ground.

4 Package Description

4.1 Ordering Information

Order #	Marking	Temp. range	Package
MT6605N		-40 ~ +85 °C	QFN32

4.2 Top mark

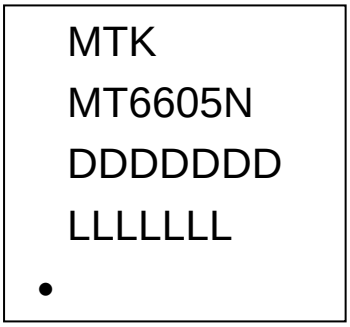
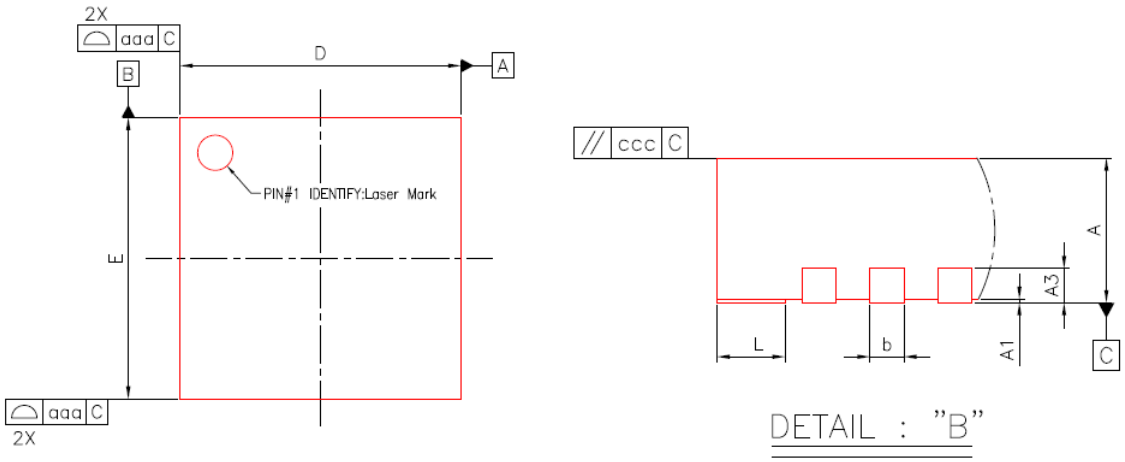
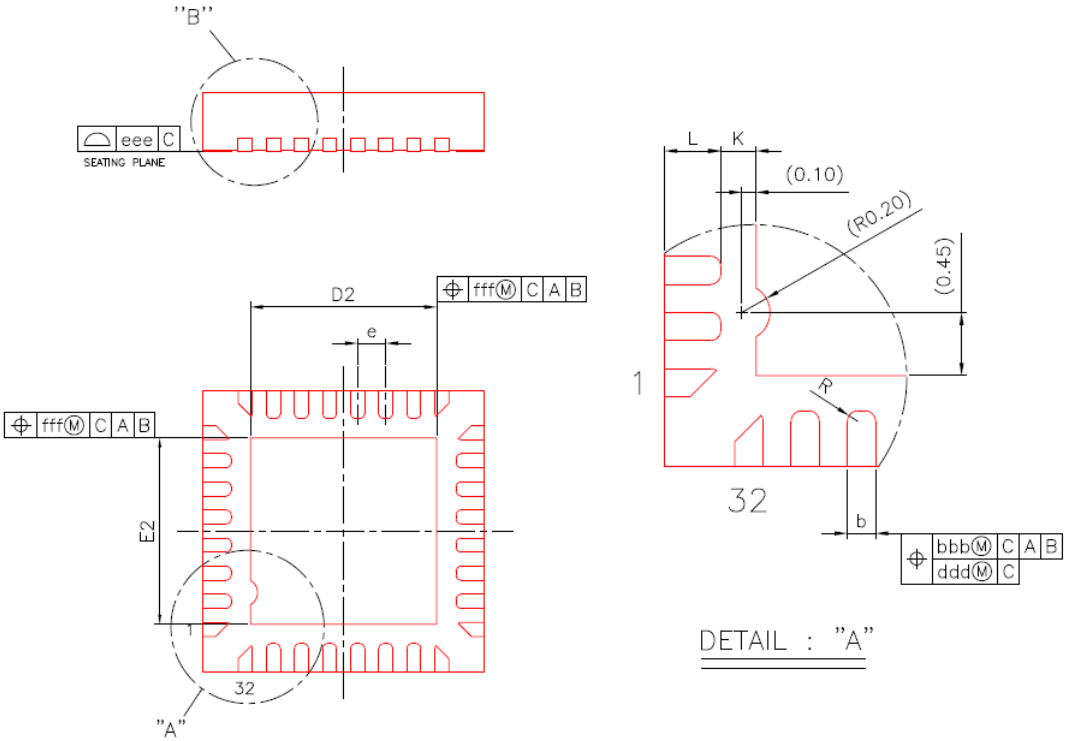


Figure 4-1: MT6605N product marking

N: QFN package
DDDDDDD: Date code
LLLLLLL: Die1 Lot number

4.3 Package dimensions





Exposed Pad Size							Internal Pad Size					
L/F	Dimension in mm			Dimension in inch			Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
D2	2.50	2.65	2.80	0.098	0.104	0.110	2.75	2.90	3.05	0.108	0.114	0.120
E2	2.50	2.65	2.80	0.098	0.104	0.110	2.75	2.90	3.05	0.108	0.114	0.120

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	3.90	4.00	4.10	0.154	0.157	0.161
E	3.90	4.00	4.10	0.154	0.157	0.161
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.220	0.275	0.330	0.009	0.011	0.013
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER

2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 4-2: Package outline and dimension

5 MT6605 RF Part

5.1 Receiver

This direct conversion receiver directly translates the received PCD or PICC signal to base-band frequencies for digital demodulation. It consists of an IQ demodulator, an analog base-band band-pass filter and analog programmable gain amplifier. These circuits are automatically configured according to the receiver mode and received information.

The receiver can be configured to receive differential inputs, or unbalanced input (default mode). In the default mode, the receiver accepts its input through an external RC voltage divider. The values of these external resistor and capacitor are designed to avoid saturating the receiver input under all recommended operating conditions.

5.2 Transmitter

In the default mode, the transmitter consists of a differential PA driver with programmable modulation index. This transmitter can also be configured to provide unbalanced output for the reduction of external Bill of Materials (BoM).

The transmitter is connected to the antenna coil through an external EMI filter and a capacitive matching network. The EMI filter helps to mitigate co-existence issues with other commercial RF system and can be removed if they are not a concern. The external matching network must be designed to present an optimum PA load according to the configured data rate and data type.

5.3 Clock Generation and Management Unit (CGMU)

The CGMU consists of the following clock sources:

a. Full integrated Frac-N PLL to generate 27.12MHz/13.56MHz clock sources
b. Clock Recovery Circuit to recover 13.56MHz clock from Field
c. Internal Oscillator with 27.12 MHz crystal
d. Low Power Oscillator 300KHz

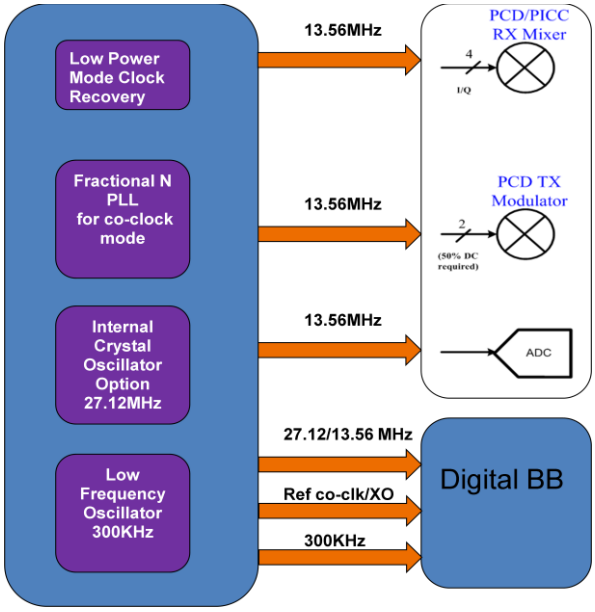


Figure 5-1: Clock generation and Management Unit

5.3.1 Integrated Frac-N PLL

The Frac-N PLL will generate a low noise 27.12/13.56MHz clock for input reference clocks of 19.2M, 20M, 24M, 26M, 38.4M, 40M and 52MHz.

The generated 13.56MHz clock will be supplied to RX and TX for PCD and Peer to Peer Initiator Mode while the 27.12MHz will be provided to DBB in Full Power Mode. The integrated Frac-N will be disabled during Low Power/Power by Field Mode. For 27.12MHz crystal oscillator mode, the Frac-N will be disabled in PCD mode.

5.3.2 Low Power Mode Clock Recovery

The clock recovery circuit will be enabled when the Field is detected. The recovered 13.56MHz clock will be supplied to PICC RX and DBB in Low Power Mode and Power by the Field.

5.3.3 Internal Oscillator with 27.12MHz Crystal

When Internal Oscillator with 27.12MHz crystal option is used, the Frac-N PLL will be disabled. The 27.12MHz clock will be divide-by 2 to generate 13.56MHz clock to the TX. The 27.12MHz clock will be directly supplied to DBB.

5.3.4 Low Power Oscillator 300 KHz

The 300 KHz oscillator will be enabled when 2.6V is available. The DBB will switch to this clock during sleep mode or Low Power Polling Mode.

6 MT6605 digital Part

6.1 Boot ROM

The embedded boot ROM provides a function of loading a set of user code through the host interface into SRAM. The host interface (UART/SPI/I2C) is decided by strap control.

6.2 Pseudo-NVRAM

There is a special V_RTC domain to protect Pseudo-NVRAM data. The power source of V_RTC comes from external capacitor and keeps the Pseudo-NVRAN data when VBAT is off.

6.3 Clock module

Clock module used to generate specific rate clock for all digital module. Two clock domain build in MT6605: One is HIF (host interface) clock domain and another is BB (baseband) clock domain. HIF clock is always from reference clock (crystal or co-clock) and so only work in full power mode. BB clock source and switch from LFO, reference clock, or BB_CK. There are many CG in this clock domain to generate the low rate clock for baseband modem and SWP. Within all generated digital clocks, only DSP clock is always on. Others are default gated and let DSP to choose which need to be turn on.

6.4 Reset scheme

The built-in reset controller generates reset signals for all digital blocks. It has power-on reset feature and hardware trapping function. The software reset function for different circuit blocks are also included for flexible applications.

6.5 Microcontroller

MT6605 has an embedded DSP (Digital Signal Processor). The DSP is a fixed-point processor with 16 bit ALU. The DSP memory includes 56KB ROM for program code storage, 48KB RAM for program code and data usage, and 17.5KB Pseudo NVRAM for program code and data storage. The DSP receives and handles the RF and baseband event interrupt and control the system.

6.6 Host interface

MT6605 supports 3 different host interfaces, which are UART, SPI, and I2C. The interface used as the host interface is determined by strap pins.

6.6.1 UART

UART is the abbreviation of “Universal Asynchronous Receiver/Transmitter”. MT6605 has 1 full duplex serial port. It is used for serial data communication. An UART converts bytes of data to and from asynchronous start-stop bit streams represented as binary electrical impulses.

There are several functions in MT6605 related to UART communication, such as UART data transmission/receive. The receiver (RX) and transmitter (TX) side of every port contains 640 bytes of URAM. The bit rates are selectable and range from 4.8k to 921.6 kbps. UART provides signal or message outputs.

6.6.2 SPI

The serial peripheral interface port manages the communication between digital BB and external devices. MT6605 supports only slave mode and contains with 640-byte URAM for transmitting and receiving data. The clock phase and clock polarity are selectable. MT6605 supports manual or automatic indicator for the notification to the host of data transferring.

6.6.3 I2C

The I2C interface is mainly connected to external devices. MT6605 supports only I2C slave mode and contains with 640-byte URAM for transmitting and receiving data. It also supports both 7-bit and 10-bit address modes up to 400 Kb/s fast mode and 3.4 Mb/s high-speed mode. In additions, MT6605 supports manual or automatic indicator for the notification to the host of data transferring. Device addresses in the slave mode are programmable and support fast mode and high-speed mode data transmission and reception.

6.7 Interrupt control unit

The interrupt control unit manages all internal and external sources of interrupts, which include timer, watch-dog, all interfaces such as UART, I2C and SPI and external user interrupt pins. These interrupt sources can be wake-up events in the power saving mode.

6.8 Baseband unit

The main function of baseband is to realize modulation and demodulation of ISO14443/18092/15693. Three main blocks includes in this part: TX, RX, and TIMCON.
TX part get payload data in byte form FIFO and calculate CRC, convert to serial data, do encoding, and add SOS, SOF, EOS, EOF, parity and subcarrier if necessary. One bit output to RF for TX part to control PA high/low level in PCD mode or load modulation control in PICC mode.

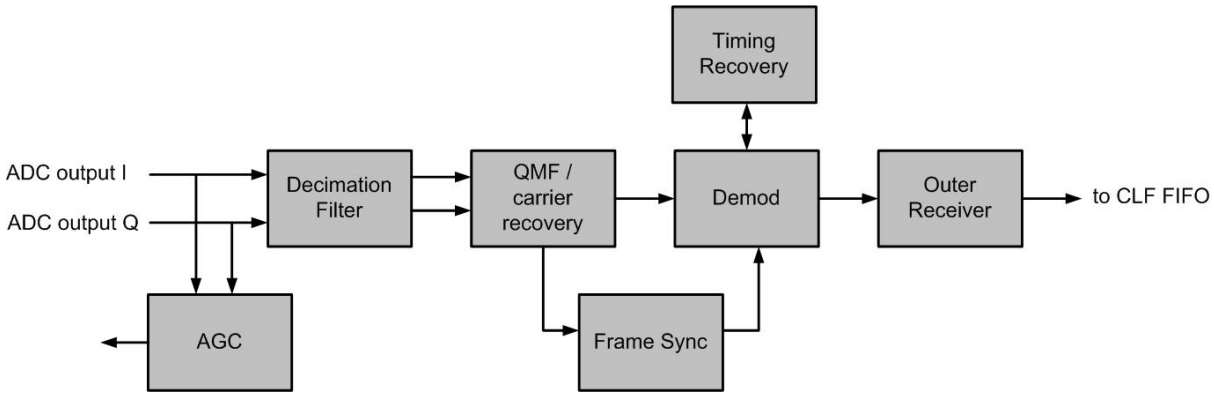


Figure 6-1: Baseband function unit

RX part get I/Q data from ADC output and combine to one date path after carrier recovery of decimation filter output. Specific frame sync for each type of NFC is used to detect the frame boundary and trigger demodulation that generates the data bit stream to outer receiver. Parity and CRC are check at outer receiver and send data in byte to CLF FIFO. An auto gain control also includes in case that ADCs saturate.
TIMCON is designed for TX/RX working period control. It has predefined state transition and programmable timing threshold to control the duration between TX and RX. Continuous TX/RX such as type F SDD is also supported.

6.9 SWP interface

SWP is Single Wire Protocol, and is the interface between the UICC and the CLF. The MT6605 supports three SWP interfaces including UICC and SE. The bit rate is from 106KHz to 1.69MHz and compliant to ETSI TS 102 613 v9.1.0.

7 Power mode

7.1 Power scheme

MT6605 is designed for Near-Field communication without any interference. With sophisticated built-in state control and advanced power management, the operating mode can be changed seamlessly while achieving minimum power consumption.

MT6605's operating modes can be categorized into 7 major modes:

- Full Power mode
- Hard power down mode
- Suspend mode
- Full Power standby mode
- Low power mode
- Low power standby mode
- No power mode

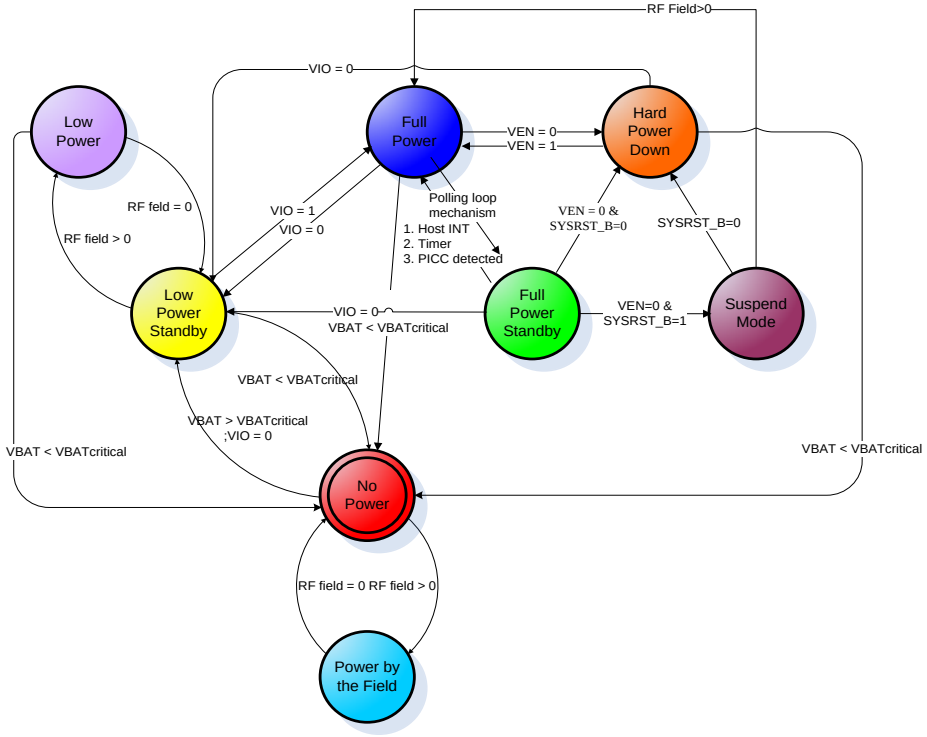


Figure 7-1: Power mode definition

8 Electrical Characteristics

8.1 Typical current consumption

Operating mode	Current consumption	Unit
Full power mode	55	mA
Hard power down mode	10	μA
Suspended mode	10	μA
Full Power standby mode	50	μA
Low power mode	3.8	mA
Low power standby mode	10	μA

Table 8-1: Typical current consumption

8.2 DC characteristics

Parameter	Description	Min	Max	Unit
V_{IL} (VDD28 = 2.8v)	Input logic low voltage	-0.3	0.25*VDD28	V
V_{IH} (VDD28 = 2.8v)	Input logic high voltage	0.75*VDD28	VDD28+0.3	V
V_{OL} (VDD28 = 2.8v)	Output logic low voltage		0.15*VDD28	V
V_{IH} (VDD28 = 2.8v)	Output logic high voltage	0.85*VDD28		V
V_{IL} (VDD28 = 1.8v)	Input logic low voltage	-0.3	0.25*VDD28	V
V_{IH} (VDD28 = 1.8v)	Input logic high voltage	0.75*VDD28	VDD28+0.3	V
V_{OL} (VDD28 = 1.8v)	Output logic low voltage		0.15*VDD28	V
V_{IH} (VDD28 = 1.8v)	Output logic high voltage	0.85*VDD28		V

Table 8-2: DC characteristics of digital IO

8.2.1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
VBAT	Battery regulator supply voltage	-0.3	4.73	V
DVDDIO	I/O supply voltage			V
DVDD28	RTC supply voltage			V
T_{ST}	Storage temperature	-55	+125	°C

Table 8-3: Absolution maximum ratings

8.2.2 Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VBAT	VBAT power supply	2.8*	-	4.3	V
DVDD12	1.2 volts baseband core power	1.08	1.2	1.32	V
DVDDIO	2.8 volts digital I/O power	2.52	2.8	3.08	V
	1.8 volts digital I/O power	1.62	1.8	1.98	V
DVDD28	2.8V pseudo-NVRAM domain	1.2	2.8	4.3	V
DVDD18	1.8V volts supply for common RF block in LDO mode	1.62	1.8	3.08	V
TA	Operating temperature	-40	25	85	˚C
Tj	Commercial junction operating temperature	0	25	115	˚C
	Industry junction operating temperature	-40	25	125	˚C

* Low power mode only. During Full Power Mode operation, VBAT_min=3.4V.

8.2.3 General DC characteristics

Symbol	Parameter	Condition	Min.	Max.	Unit
I_{IL}	Input low current	No pull-up or down	-1	1	uA
I_{IH}	Input high current	No pull-up or down	-1	1	uA
I_{OZ}	Tri-state leakage current		-10	10	uA

8.2.4 DC electrical characteristics for 2.8 volts operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DVDD12	Supply voltage of core power		1.08	1.2	1.32	V
DVDDIO	Supply voltage of IO power		2.52	2.8	3.08	V
V_{IL}	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	40	85	190	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 2.8 V	40	85	190	KΩ

8.2.5 DC electrical characteristics for 1.8 volts operation

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
DVDD12	Supply voltage of core power		1.08	1.2	1.32	V
DVDDIO	Supply voltage of IO power		1.62	1.8	1.98	V
V_{IL}	Input lower voltage	LVTTL	-0.3	-	0.25*VDDIO	V
V_{IH}	Input high voltage		0.75*VDDIO	-	VDDIO+0.3	V
V_{OL}	Output low voltage	VDDIO = min I_{OL} = -2 mA	-	-	0.15*VDDIO	V
V_{OH}	Output high voltage	VDDIO = min I_{OH} = -2 mA	0.85*VDDIO	-	-	V
R_{PU}	Input pull-up resistance	VDDIO = typ Vinput = 0 V	70	150	320	KΩ
R_{PD}	Input pull-down resistance	VDDIO = typ Vinput = 1.8 V	70	150	320	KΩ

8.3 RF related characteristics

8.3.1 Receiver

Parameter	Condition	Min.	Typ.	Max.	Unit
RF input frequency		-	13.56	-	MHz
RX Input Resistance	PCD mode		2000		Ω
	PICC mode		500		
RX Input Capacitance			TBD		pF
Max. Input RF Level				1.5	Vpp
Min. Detectable Field Level			0.1875		A/m

8.3.2 Transmitter

Parameter	Condition	Min.	Typ.	Max.	Unit
RF input frequency		-	13.56	-	MHz
RX Input Resistance	PCD mode		2000		Ω
	PICC mode		500		
RX Input Capacitance			TBD		pF
Max. Input RF Level				1.5	Vpp
Min. Detectable Field Level			0.1875		A/m

8.3.3 Crystal oscillator (XO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{xo}	XO oscillation frequency	27.106	27.12	27.134	MHz
V_{xo}	XO voltage swing	1.5	2.5	3	Vpp

8.3.4 Clock Generation & Management Unit

Parameter	Condition	Min.	Typ.	Max.	Unit
RX LO Clock	PCD/PICC	13.553	13.56	13.567	MHz
TX LO Clock	PCD	13.553	13.56	13.567	MHz
DBB Clock	Full Power Mode	27.106	27.12	27.134	MHz
	Low Power/Power by the Field	13.553	13.56	13.567	MHz
F_{ref} Clock	Fractional-N Mode	19.2	26	52	MHz
V_{ref} Clock	Clock In	0.2	1.2	1.5	Vpp
Lock Time		50u	100	150	us

9 Interface Characteristics

9.1 UART interface timing

Baudrate required (bps)	Programmed baudrate (bps)	Baudrate error (%)
4,800	4,801.699717	-0.04%
9,600	9,603.399433	-0.04%
14,400	14,394.90446	-0.04%
19,200	19,206.79887	-0.04%
38,400	38,413.59773	-0.04%
57,600	57,579.61783	-0.04%
115,200	115,404.2553	-0.18%
230,400	231,794.8718	-0.61%
460,800	467,586.2069	-1.47%
921,600	935,172.4138	-1.47%

Table 9-1: UART baudrate settings

Notes:
1. UART baud-rate settings with UART_CLK frequency = 27.12 MHz (UART_CLK uses the reference clock of the system).
2. The baudrate error is optimized. Each baudrate needs to adjust counter to obtain the optimized error.

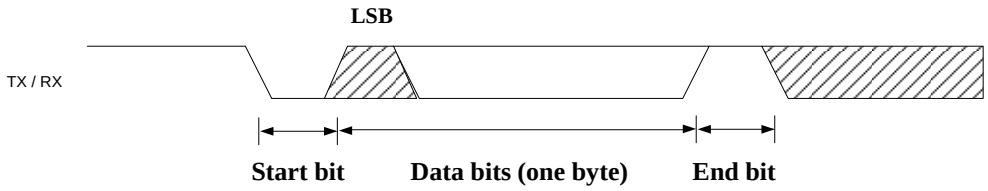


Figure 9-1: Timing diagram of URAT interface

9.2 SPI interface timing

Description	Symbol	Min.	Max.	Unit	Note
SCS# setup time	T1	0.5T	-	ns	1
SCS# hold time	T2	0.5T	-	ns	1
SO setup time	T3	0.5T – 3t	0.5T - 2t	ns	1, 2
SO hold time	T4	0.5T + 2t	0.5T + 3t	ns	1, 2
SIN setup time	T5	3t	-	ns	1, 2
SIN hold time	T6	10	-	ns	1

Table 9-2: SPI interface timing constraint

Notes:

1. The condition of SPI clock cycle (T)
2. t indicates the period of SPI controller clock

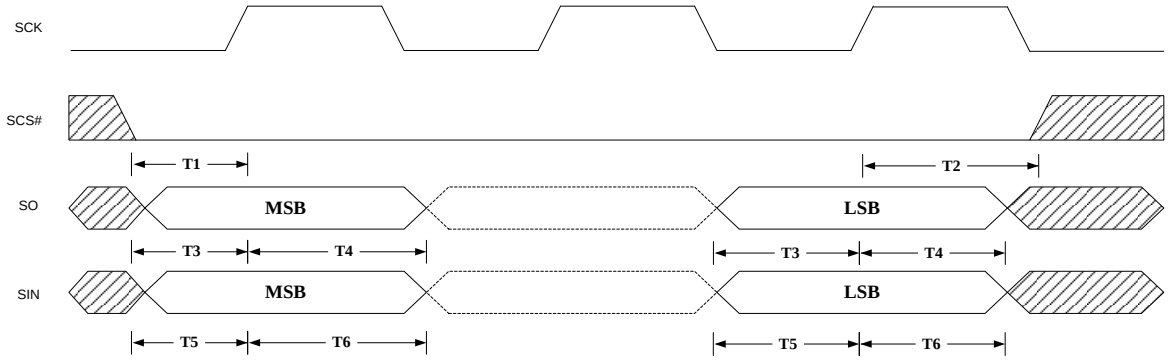


Figure 9-2: Timing diagram of SPI interface

9.3 I2C interface timing

Symbol	Period
T1	Data set-up time > 10ns
T2	LOW period of the SCL clock > 160ns
T3	HIGH period of the SCL clock > 60ns

Table 9-3: I2C timing constraint

Note: The table above is based on 400pF loading.

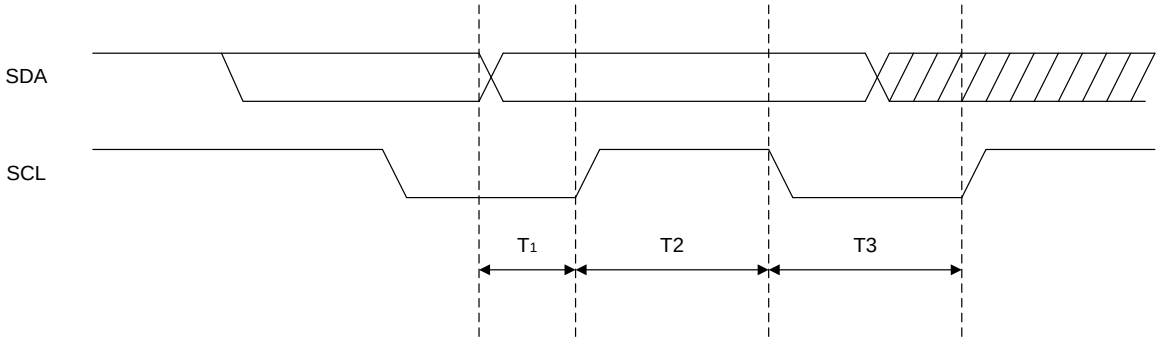


Figure 9-3: Timing diagram of HOST I2C interface

ESD CAUTION

MT6605 is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT6605 is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.