MT6601 Bluetooth Transceiver and Baseband Processor External Data Sheet

Revision 1.00

Sep 13, 2006

Revision History

Revision	Date	Comments
0.90	2006/07/24	Preliminary Release. Some values may still be subject to changes.
1.00	2006/09/13	Add more package dimension information.

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Preface

Acronym for Register Type

R/W	Capable of both read and write access
RO	Read only
RC	Read only. After reading the register bank, each bit which is HIGH(1) will be cleared to LOW(0) automatically.
WO	Write only
W1S	Write only. When writing data bits to register bank, each bit which is HIGH(1) will cause the corresponding bit to be set to 1. Data bits which are LOW(0) has no effect on the corresponding bit.
W1C	Write only. When writing data bits to register bank, each bit which is HIGH(1) will cause the corresponding bit to be cleared to 0. Data bits which are LOW(0) has no effect on the corresponding bit.

1 System overview

1.1 General description

Bluetooth is a low-cost wireless technology used to provide “ad hoc” networking between versatile portable devices such as cell phones, PDAs, digital cameras, headsets, and more.

MT6601 is a highly integrated Bluetooth platform IC. It includes powerful baseband processing capabilities with rich features and a high performance transceiver, all in a compact single package.

1.2 Features

Radio features

- Fully compliant with Bluetooth specification 1.2.
- Low out-of-band spurious emissions supports simultaneous operation with GPS, GSM/GPRS worldwide radio systems.
- Direct conversion architecture with no external channel filter or VCO resonator components.
- Fully integrated RF front-end matching circuits eliminates external balance and T/R switch.

Transmitter features

- Meets class 2 and class 3 transmitting requirement.
- Support Class 1 operation with external PA.

Receiver features

- -85dBm sensitivity with excellent interference rejection performance.
- Hardware AGC dynamically adjusts receiver performance in changing environments.

Baseband features

- eSCO support.
- 3 simultaneous SCO channels.
- Scatternet support.
- Sniff mode, hold mode, and part mode support.
- AFH and PTA collaborative support for WLAN/BT coexistence.
- Lower power mode and deep sleep mode enables ultra low power consumption

Platform features

- On-chip voltage regulation simplifies voltage input requirements.
- Low power consumption in active and standby mode.

- Wide ranges of crystal and external reference clock support.
- PCM interface and built-in transcoders for A-law, μ-law and linear voice.
- Built-in hardware modem engine for access code correlation, header error correction, forward error correction, CRC, whitening, and encryption.
- High speed UART support.
- Built-in RAM and ROM with patch system.

Software features

- Supports standard HCI interface.

1.3 Applications

MT6601 is designed to provide direct interface with existing handset chip as shown in **Figure 1**.

The PCM interface provides master or slave mode operation with programmable data frequency to connect to the voice channel with the GSM baseband. The UART interface supports hardware flow control as well as high-speed baud rate. The PTA interface accommodates different arbitration scheme enabling efficient channel utilization in co-existence environment. The external reference clock interface supports wide ranges of frequencies that the mobile phones use.

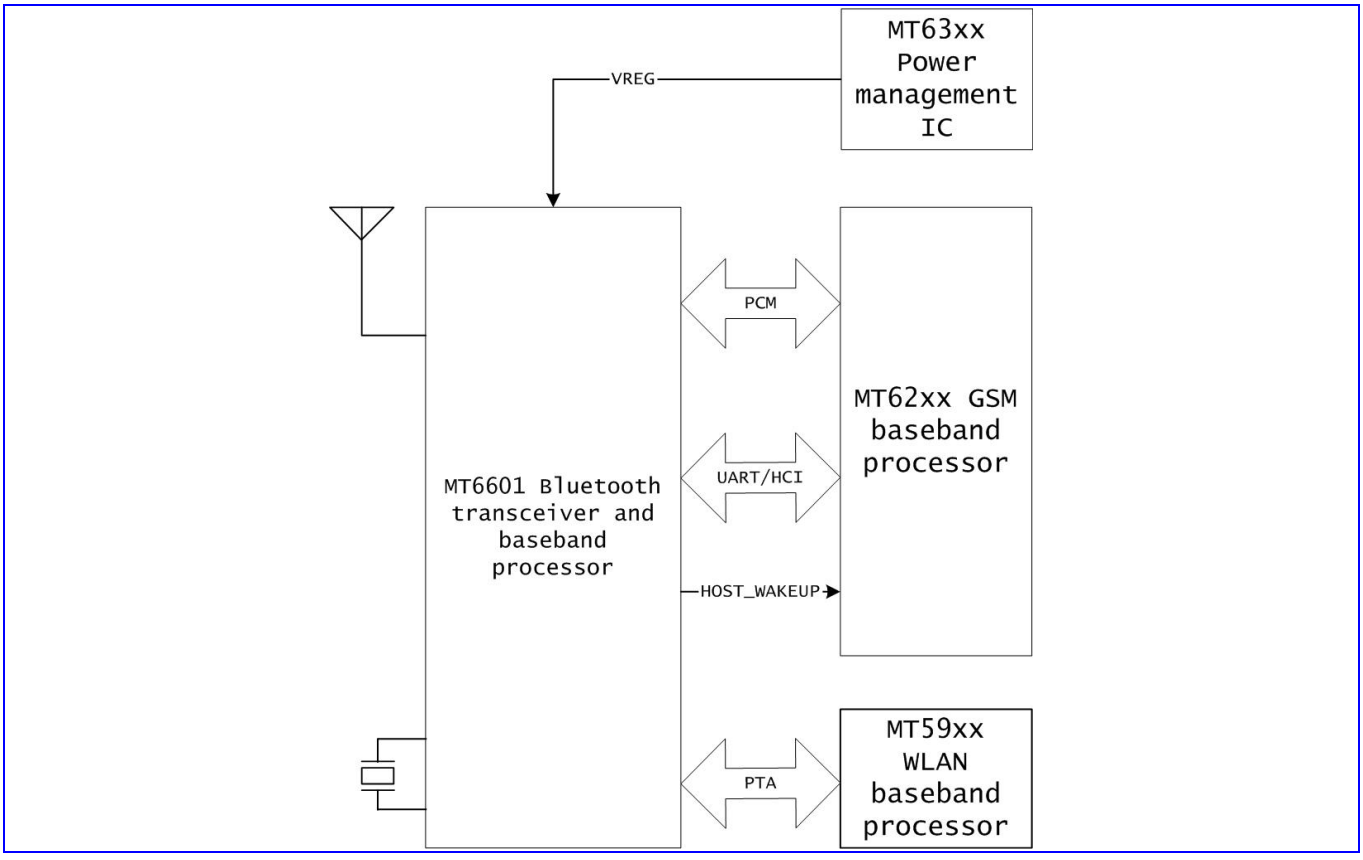

Figure 1 Mobile phone application.

1.4 Block diagram

The internal connection of the major physical blocks and their associated external interfaces are shown in **Figure 2**.

The transceiver section of MT6601 incorporates the complete receive and transmit paths, including PLL, VCO, LNA, PA, modulator, demodulator.

The baseband signal processor incorporates hardware engines performing frequency hopping, error correcting, whitening, encrypting, data packet assembling and de-assembly to offload the embedded ARM7.

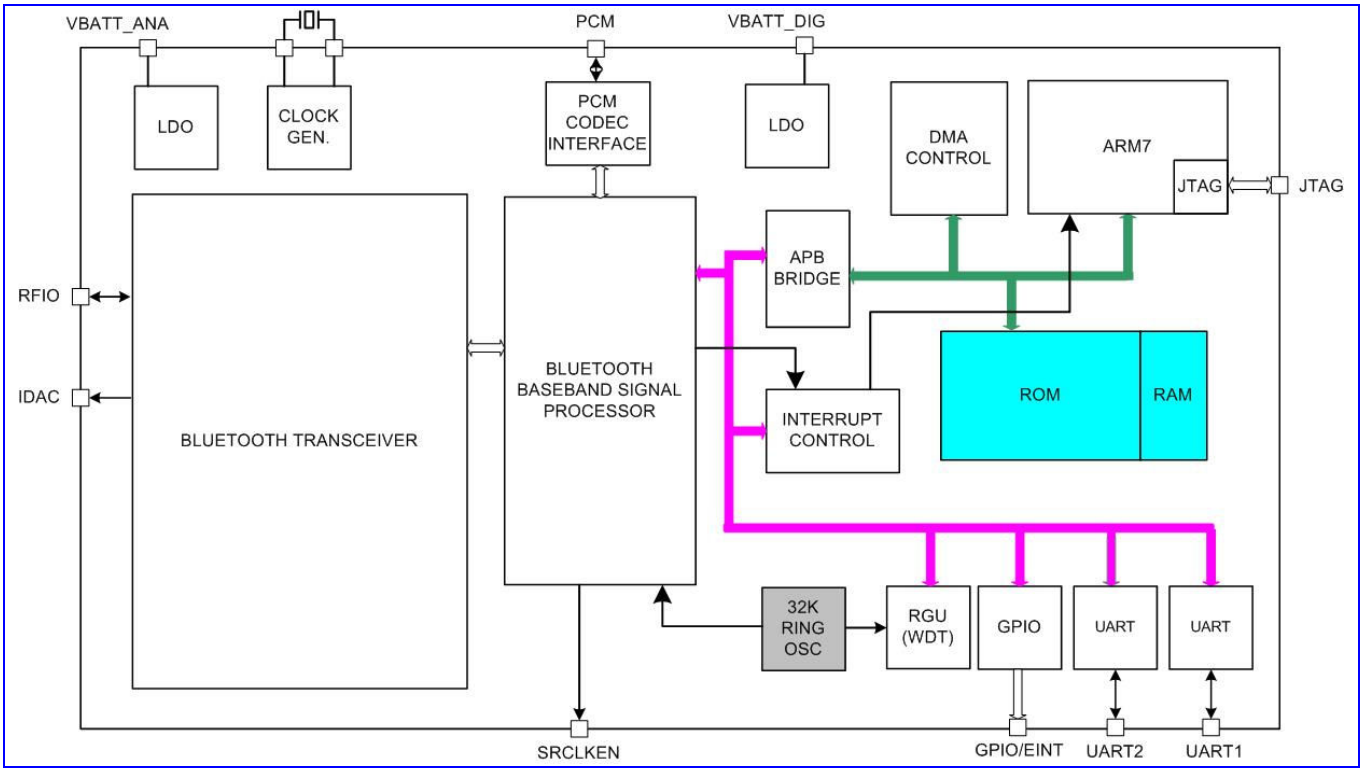

Figure 2 MT6601 functional block diagram

2 Product description

2.1 Pin description

Ball 8x8	Pin Name	I/O	Pin description	GPIO mode				PU/PD/ SW*	Reset
				Mode 0	Mode 1	Mode 2	Mode 3		
			JTAG port						
J2	JTRST_B	I	JTAG interface					PD	Input
H2	JTCK	I	JTAG interface					PU	Input
J3	JTDI	I	JTAG interface					PU	Input
H3	JTMS	I	JTAG interface					PU	Input
H4	JTDO	O	JTAG interface						0
J5	JRTCK	O	JTAG interface						0
			UART port						
G5	URTS1	I	UART1 request to send active low	URTS1	GPIO8	URTS2	IDS8	PU/SW	Input
H5	UCTS1	O	UART1 clear to send active low	UCTS1	GPIO9	UCTS2	IDS9	PU/SW	Input
J6	UTXD1	O	UART1 data output active high	UTXD1					1
H6	URXD1	I	UART1 data input active high	URXD1				PU	Input
H7	URXD2	I	UART2 data input active high	URXD2	GPIO10	SPI_CLK	IDS10	PU/SW	Input
J8	UTXD2	O	UART2 data output active high	UTXD2	GPIO11	SPI_SS	IDS11	PU/SW	Input
			PCM port						
G9	PCMCLK	I	PCM data clock	PCMCLK	GPIO12	BT_LIF_CLK		PU/SW	Input
G8	PCMSYNC	I	PCM data sync	PCMSYNC	GPIO13	BT_1M_CLK		PD/SW	Input
F9	PCMOUT	O	PCM synchronous data out	PCMOUT	GPIO14	AHB_CLK	PCM_LOOPBACK	PD/SW	Input
F8	PCMIN	I	PCM synchronous data in	PCMIN	GPIO15	MCU_CLK		PD/SW	Input
			GPIO port						
H9	GPIO0/EINT0	I/O	Programmable input/output & external interrupt	GPIO0	EINT0	SPI_D2A	IDS0	PU/SW	Input
H8	GPIO1/EINT1	I/O	Programmable input/output & external interrupt	GPIO1	EINT1	SPI_A2D	IDS1	PU/SW	Input
C9	GPIO2	I/O	Programmable input/output	GPIO2	GIO_IRQ	RESET_N	IDS2	PD/SW	Input
C8	GPIO3	I/O	Programmable input/output	GPIO3	SRCLKENA_IN	TAB_IRQ	IDS3	PD/SW	Input
B8	GPIO4	I/O	Programmable input/output	GPIO4	BT_ACT	HOP_STROBE	IDS4	PD/SW	Input
A9	GPIO5	I/O	Programmable input/output	GPIO5	WL_ACT	CD_TXEN	IDS5	PD/SW	Input
A8	GPIO6	I/O	Programmable input/output	GPIO6	BT_PRI	RX_TX_DATA	IDS6	PD/SW	Input
A7	GPIO7	I/O	Programmable input/output	GPIO7	BT_FREQ	BB_CLOCK	IDS7	PD/SW	Input
			Clock/Reset/Test mode						
H1	TESTMODE	I	Test mode enable	TESTMODE				PD	Input
J1	SYSRST_B	I	System reset active low	SYSRST_B					Input
J7	SRCLKENA	O	Source clock enable to the host or the oscillator.	SRCLKENA					0
B9	EXT32K	I	External low power clock input	EXT32K	GPIO16	LPO_CK	IRQ_B		Input

			Digital supply						
J4	**VDDP**	P	2.8V I/O power supply						
D9	**VDDP**	P	2.8V I/O power supply						
G2	**VDDK**	P	1.8V core power supply						
B7	**VDDK**	P	1.8V core power supply						
G1	**VSS**	P	I/O ground						
J9	**VSS**	P	I/O ground						
C7	**VSS**	P	I/O ground						
E5	**VSS**	P	I/O ground						
E6	**VSS**	P	I/O ground						
F4	**VSS**	P	I/O ground						
F5	**VSS**	P	I/O ground						
			Digital regulator						
F6	**VSS**	P	I/O ground						
E8	**VSS**	P	I/O ground						
C6	**VSS**	P	I/O ground						
E9	**VDD_CORE**	P	Regulator 1.8V output						
D8	**VBATT_DIG**	P	Regulator input						
			RF signals						
A1	**IDAC**	A	Power control to the external power amplifier. The output provides a variable current source that can be used to control the external power amp.						
B1	**VREFP_CAP**	A	Decoupling capacitor for voltage reference for the internal A/D converter						
B2	**VREFN_CAP**	A	Decoupling capacitor for voltage reference for the internal A/D converter						
F1	**CHG_PUMP**	A	Pin for RF PLL loop filter						
G3	**TX_RX_N**	A	Tx/Rx switch. Used to control the direction of the external device.						
D6	**VBBRDY**	A	Digital regulator output ready						
A6	**XTAL_N**	A	Drive for crystal						
B6	**XTAL_P/CLK**	A	For crystal or external clock input						
B5	**MCG_CHG**	A	Pin for reference PLL loop filter						
B4	**TX_OUT**	A	Bias for output driver, or TX output for class 1						
A3	**RX_IN**	A	Combined 50Ohm input and output pin						
			Analog regulator						
D1	**VBATT_ANA**	P	Analog regulator voltage input						
C2	**GND_BB**	P	Analog regulator ground						
C1	**VDD_BB**	P	Analog regulator output						
			Analog power/ground						
D2	**VDD_VCODIG**	P	RF power supply						
E1	**VDD_VCO**	P	RF power supply						
A5	**VDD_MCG**	P	RF power supply						
A4	**VDD_TX**	P	RF power supply						
A2	**VDD_RX**	P	RF power supply						
E2	**AVSS**	P	Analog ground						
F2	**AVSS**	P	Analog ground						
C5	**AVSS**	P	Analog ground						
E4	**AVSS**	P	Analog ground						
D4	**AVSS**	P	Analog ground						
B3	**AVSS**	P	Analog ground						
D5	**AVSS**	P	Analog ground						

*SW means S/W configurable.

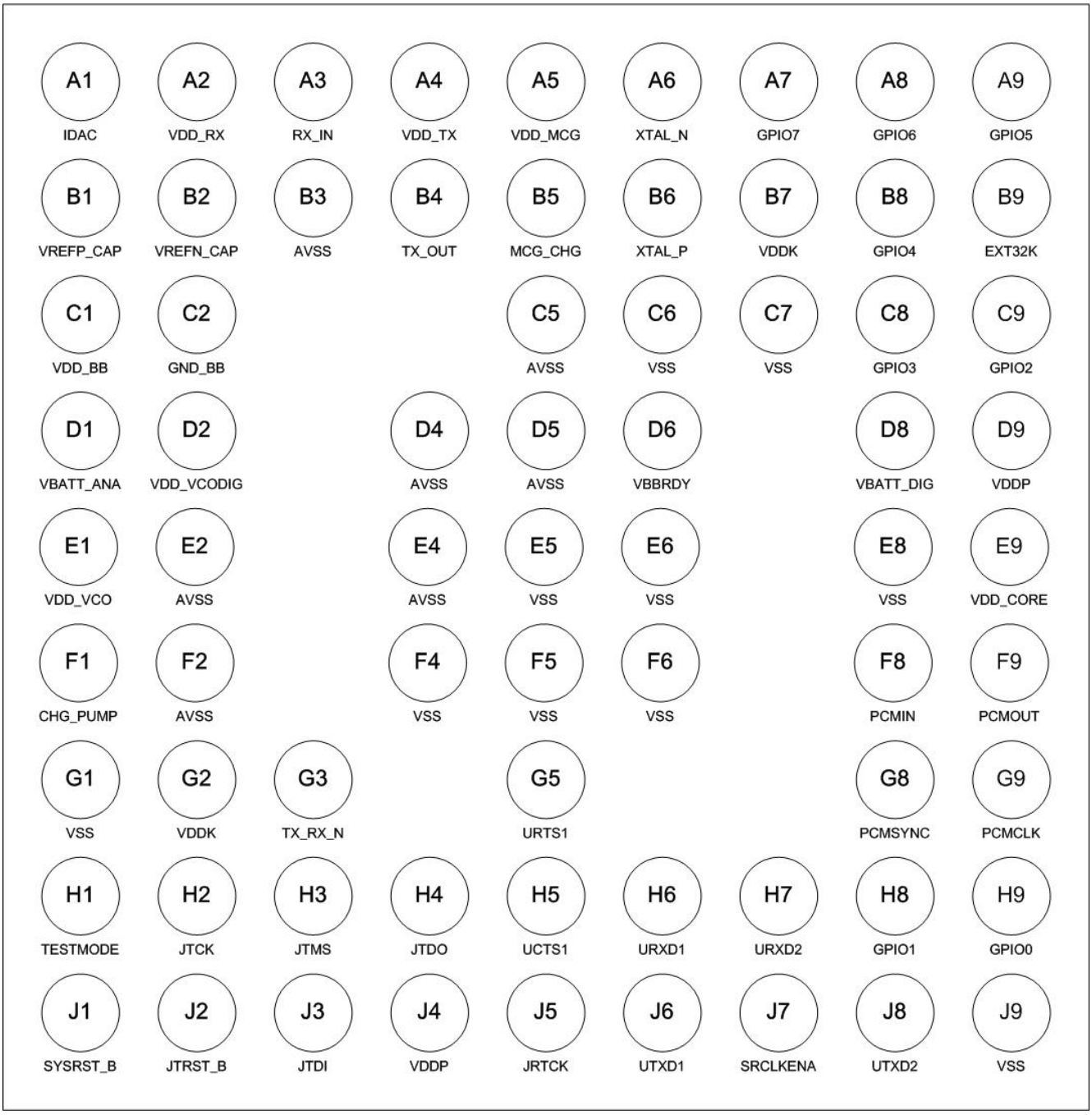

Figure 3 Top view of MT6601 pin-out.

2.2 DC characteristics

2.2.1 Absolute maximum ratings

Parameter	Description	Min	Max	Unit
V_{DDP}	I/O supply voltage	-0.3	3.63	V
V_{BATT_ANA}	Analog regulator supply voltage	-0.3	3.63	V
V_{BATT_DIG}	Digital regulator supply voltage	-0.3	3.63	V
V_{CC}	Regulated analog circuit supply voltage	-0.3	3.63	V
V_{DDK}	Regulated supply voltage directly into digital circuits	-0.3	3.63	V
T_{ST}	Storage temperature	-55	+125	°C
RF_{MAX}	Maximum RF input level	-	+5	dBm

2.2.2 Recommended operating range

Parameter	Description	Min	Max	Unit
V_{DDP}	I/O supply voltage	1.62	3.63	V
V_{BATT_ANA}	Analog regulator supply voltage	2.3	3.63	V
V_{BATT_DIG}	Digital regulator supply voltage	2.3	3.63	V
V_{CC}	Regulated analog circuit supply voltage	1.71	1.89	V
V_{DDK}	Regulated supply voltage directly into digital circuits	1.62	1.98	V
T_{OP}	Operating temperature	-20	+80	°C

2.3 Receiver specifications

Tests are performed under the normal conditions defined in Bluetooth test specification.

Parameter	Description	Min	Typ.	Max	Unit
Receiver sensitivity	BER<0.1%	-	-80	-78	dBm
Maximum usable signal	BER<0.1%	-10	-	-	dBm
C/I co-channel (BER<0.1%)	Co channel selectivity	-	9	11	dB
C/I 1MHz (BER<0.1%)	Adjacent channel selectivity	-	-3	0	dB
C/I 2MHz (BER<0.1%)	2^{nd} adjacent channel selectivity	-	-38	-35	dB
C/I≥3MHz (BER<0.1%)	3^{rd} adjacent channel selectivity	-	-45	-40	dB
Out of band blocking	30MHz to 2000MHz	-10	-	-	dBm
	2000MHz to 2399MHz	-27	-	-	dBm
	2498MHz to 3000MHz	-27	-	-	dBm
	3000MHz to 12.75GHz	-10	-	-	dBm
Inter-modulation	Max interference level to maintain 0.1% BER, interference signals at 3MHz and 6MHz offset.	-39	-30	-	dBm

2.4 Transmitter specifications

Tests are performed under the normal conditions defined in Bluetooth test specification.

Parameter	Description	Min	Typ.	Max	Unit
Output RF transmit power	At maximum power output level		+2		dBm
Modulation characteristics	$\Delta f1_{avg}$	140	155	175	kHz
	$\Delta f2_{max}$ (For at least 99.9% of all $\Delta f2_{max}$)	115	-	-	kHz
	$\Delta f1_{avg} / \Delta f2_{avg}$	0.8	-	-	kHz
Initial carrier frequency accuracy		-75.0	-	+75.0	kHz
Carrier frequency drift	One slot packet	-25.0	-	+25.0	kHz
	Two slot packet	-40.0	-	+40.0	kHz
	Five slot packet	-40.0	-	+40.0	kHz
	Max drift rate	-	-	400	Hz/us
20dB occupied bandwidth	Bluetooth specification	-	800	1000	kHz
In-band spurious emission	±2MHz offset	-	-	-45	dBm
	±3MHz offset	-	-	-55	dBm
Output-of-band spurious emission	30MHz to 1GHz, operating mode	-	-	-36	dBm
	1GHz to 12.75GHz, operating mode	-	-	-30	dBm
	1.8GHz to 1.9GHz	-	-	-47	dBm
	5.15GHz to 5.3GHz	-	-	-47	dBm

2.5 Current consumption

Operating mode	Average	Max	Unit
Deep sleep mode	TBD		uA
Standby	TBD		uA
Continuous transmit	TBD		mA
Continuous receive	TBD		mA
ACL connection, sniff mode, 40ms interval	TBD		mA
ACL data transfer, DM1	TBD		mA
SCO connection, HV3 packets	TBD		mA
Sniff mode	TBD		mA
Inquire scan	TBD		mA
Page scan	TBD		mA

2.6 External Reference Requirements

The following frequencies (in MHz) can be used: 13MHz, 16MHz, 26MHz, and 32MHz.

Parameter	Description	Min	Max	Unit
Phase noise	100Hz	-	-100	dBc/Hz
	1KHz	-	-120	dBc/Hz
	10KHz	-	-140	dBc/Hz
Drive level	AC coupled amplitude	0.5	Vcc	Vp-p
	DC coupled low peak voltage	0	0.3	V

	DC coupled high peak voltage	Vcc-0.3	Vcc	V

2.7 Package dimensions

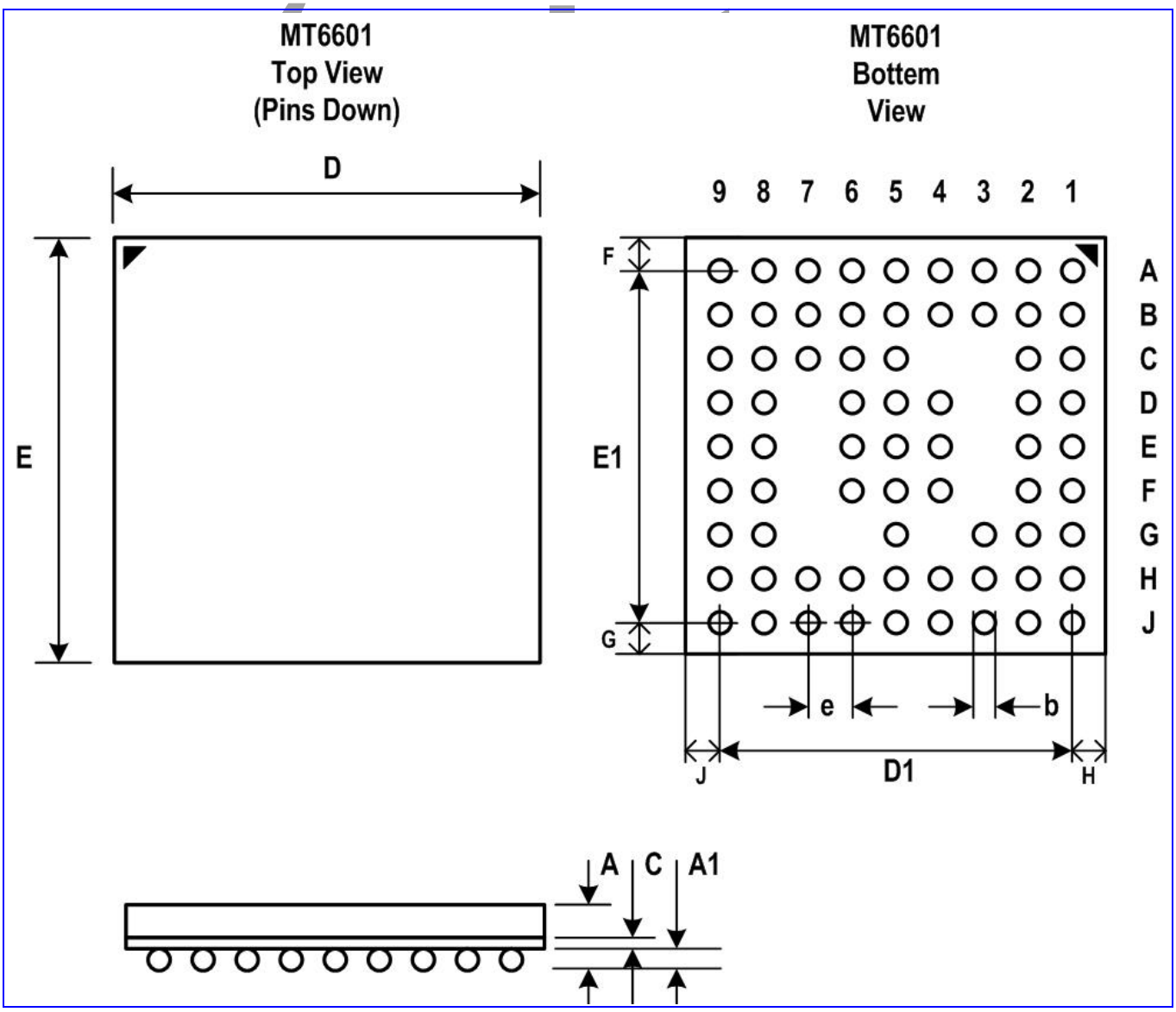

Figure 4 Package outline and dimensions of TFBGA 5mm x 5mm, 70-ball, 0.5mm pitch Package

Body Size		Ball Count	Ball Pitch	Ball Diameter	Package Thickness	Stand Off	Substrate Thickness
D	E	N	e	b	A (Max.)	A1	C
5	5	70	0.5	0.3	1.2	0.21	0.21
D1	E1	F	G	H	J		
4	4	0.5	0.5	0.5	0.5		

Table 1 Definition of TFBGA 5*5, 70-ball, 0.5 pitch Package (Unit: mm)

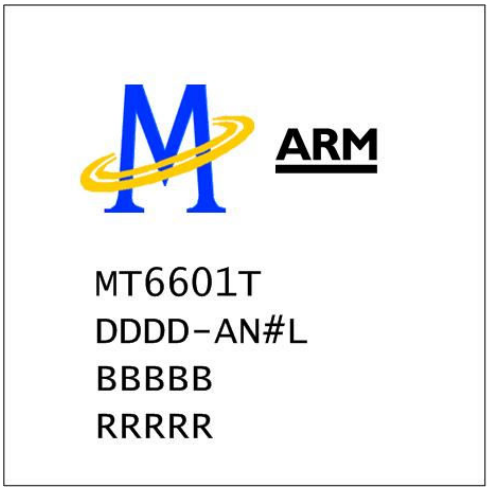

Figure 5 Product marking