MT6339N3

60V/8A Complementary Enhancement Mode Field Effect Transistor

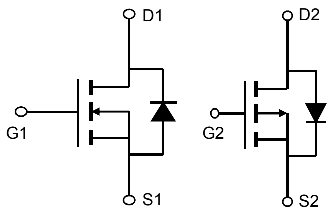
MT Semiconductor®

http://www.mtsemi.com

General Description

The MT6339N3 uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

Simplified Schematic



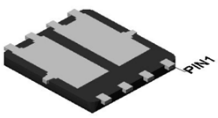
Features

N-channel	P-channel
V_{DS} (V) = 60V	-60V
I_D = 8A (V_{GS} =10V)	-8A (V_{GS} = -10V)
$R_{DS(ON)}$	$R_{DS(ON)}$
=35m Ω (V_{GS}=10V)	=64mΩ (V_{GS} = -10V)
=40m Ω (V_{GS}=4.5V)	=75mΩ (V_{GS} = -4.5V)

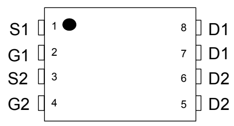
100% Rg tested

MARKING DIAGRAM & PIN ASSIGNMENT

DFN3X3-8L



Top View



Absolute Maximum Ratings T_A=25°C unless otherwise noted					
Parameter		**Symbol**	**Max Q1**	**Max Q2**	**Units**
Drain-Source Voltage		V_{DS}	60	-60	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C=25°C	I_D	8	-8	A
	T_C=100°C		8	-8	
Pulsed Drain Current		I_{DM}	24	-24	
Continuous Drain Current	T_A=25°C	I_{DSM}	4.4	-3.2	A
	T_A=70°C		3.5	-2.5	
Avalanche Current		I_{AS}	10	8	A
Avalanche energy	L=0.1mH	E_{AS}	18	12	mJ
Power Dissipation	T_C=25°C	P_D	10	8	W
	T_C=100°C		4	3.5	
Power Dissipation	T_A=25°C	P_{DSM}	2.5	1.8	W
	T_A=70°C		2	1.4	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		°C

Thermal Characteristics							
Parameter		**Symbol**	**Typ Q1**	**Typ Q2**	**Max Q1**	**Max Q2**	**Units**
Maximum Junction-to-Ambient	t ≤ 10s	$R_{\theta JA}$	25	20	35	30	°C/W
Maximum Junction-to-Ambient	Steady-State		50	48	70	65	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	7	3.5	10	4.2	°C/W

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV	Drain-Source Breakdown Voltage	ID=250μA, VGS=0V	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=48V, V_{GS}=0V			1	μA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=250μA	1.0	1.4	2.0	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=5A		35	38	mΩ
		T_J=125°C		50	56	
		V_{GS}=4.5V, I_D=5A		40	43	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=5A		43		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				10	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		760		pF
C_{oss}	Output Capacitance			125		pF
C_{rss}	Reverse Transfer Capacitance			70		pF
R_g	Gate resistance	f=1MHz	0.8	1.6	2.4	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=6A		14	20	nC
Q_g(4.5V)	Total Gate Charge			6.6	10	nC
Q_{gs}	Gate Source Charge			2.4		nC
Q_{gd}	Gate Drain Charge			3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.25Ω, R_{GEN}=3Ω		4.4		ns
t_r	Turn-On Rise Time			9		ns
$t_{D(off)}$	Turn-Off DelayTime			17		ns
t_f	Turn-Off Fall Time			6		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, di/dt=500A/μs		7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, di/dt=500A/μs		8		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

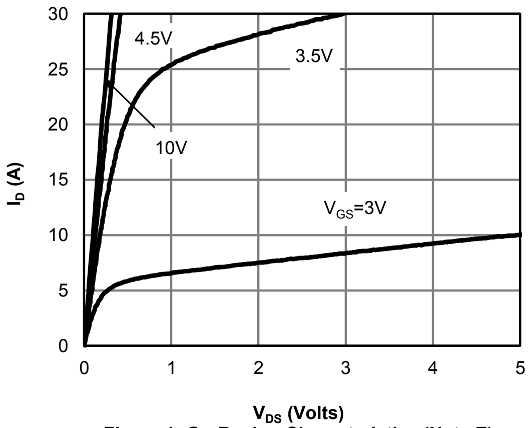


Figure 1: On-Region Characteristics (Note E)

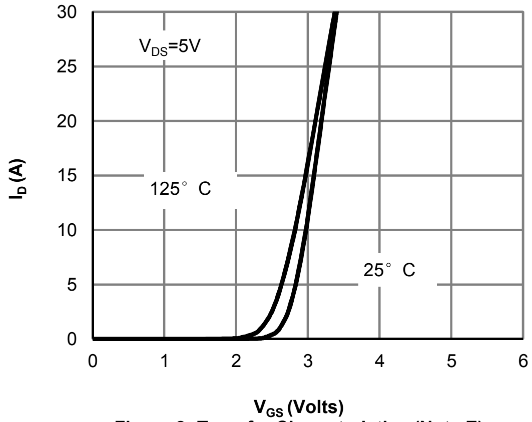


Figure 2: Transfer Characteristics (Note E)

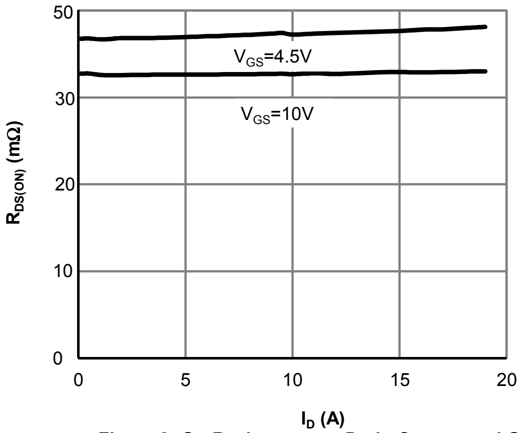


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

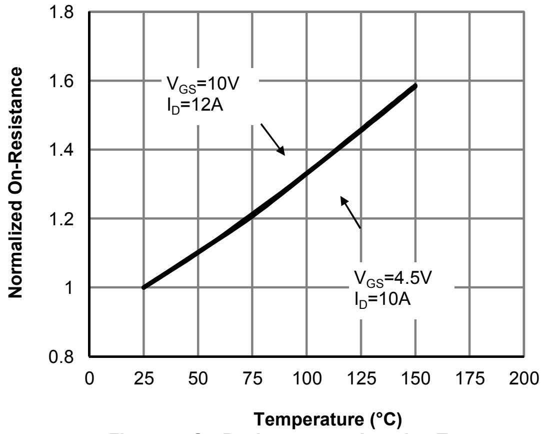


Figure 4: On-Resistance vs. Junction Temperature (Note E)

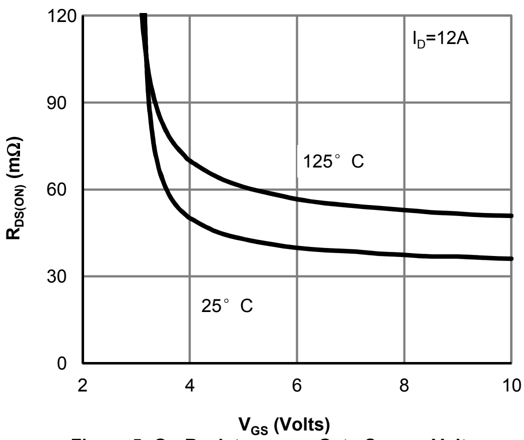


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

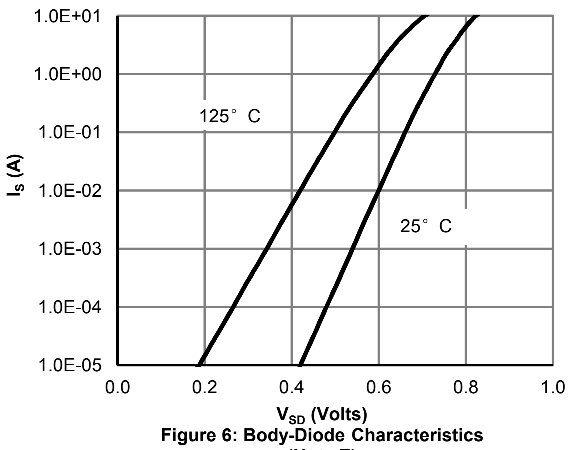


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

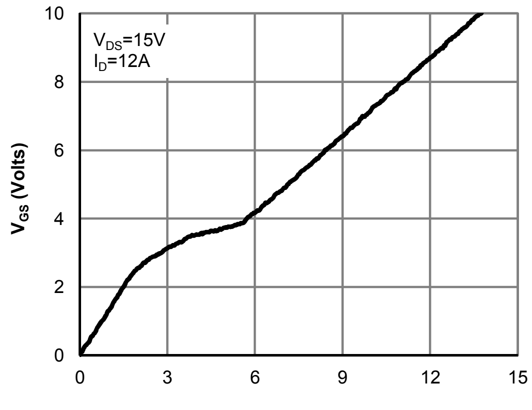


Figure 7: Gate-Charge Characteristics

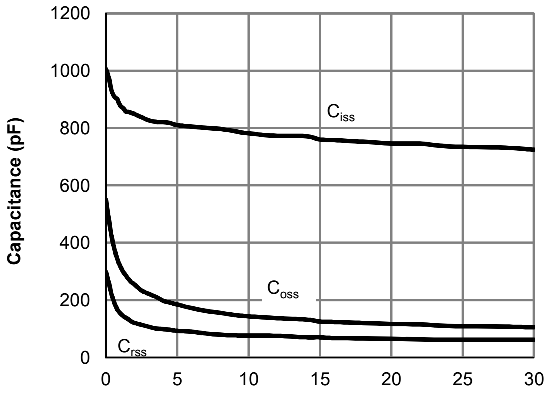
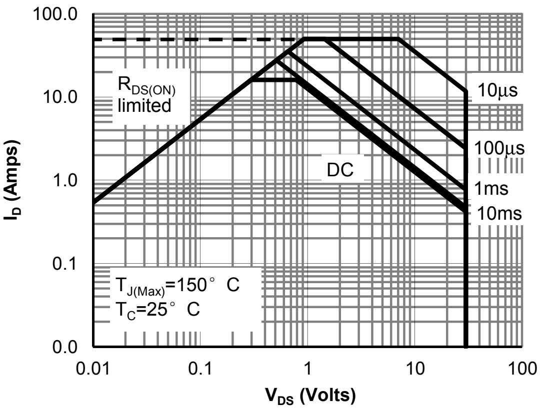


Figure 8: Capacitance Characteristics



V_{GS}> or equal to 4.5V
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

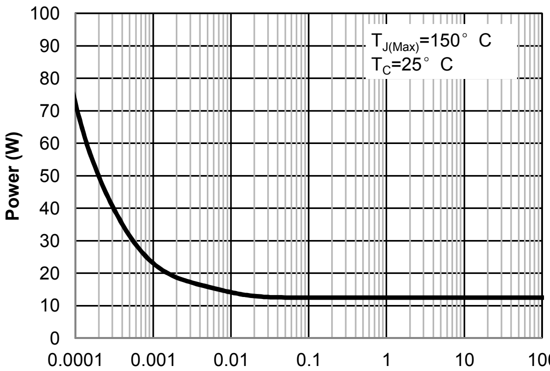


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

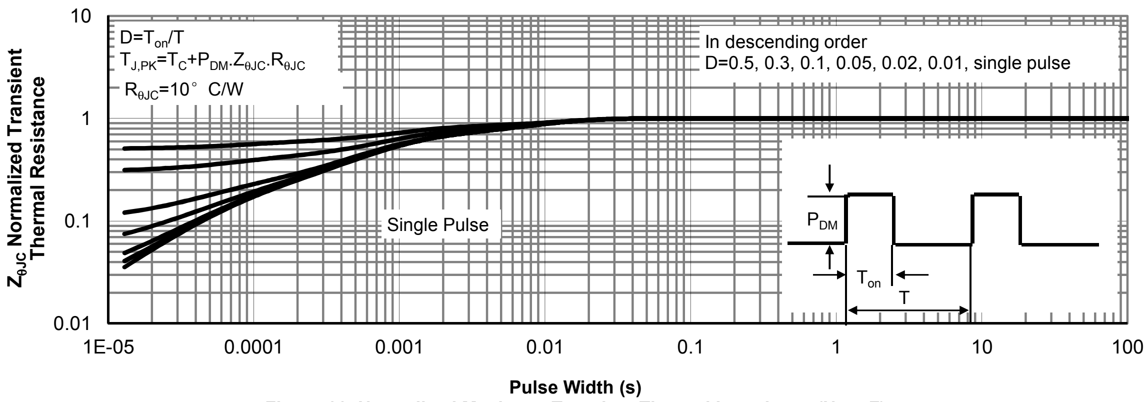


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

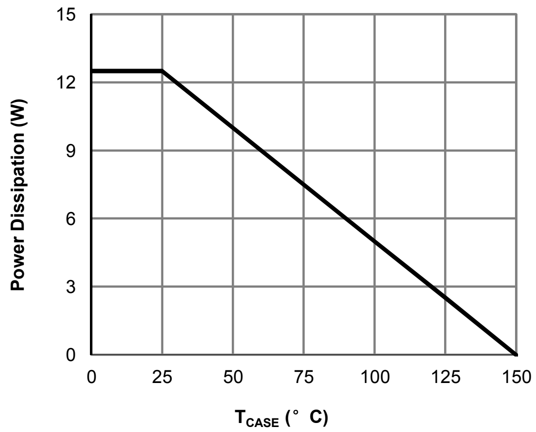


Figure 12: Power De-rating (Note F)

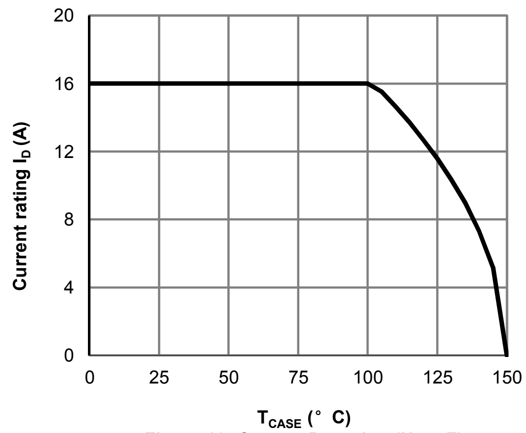


Figure 13: Current De-rating (Note F)

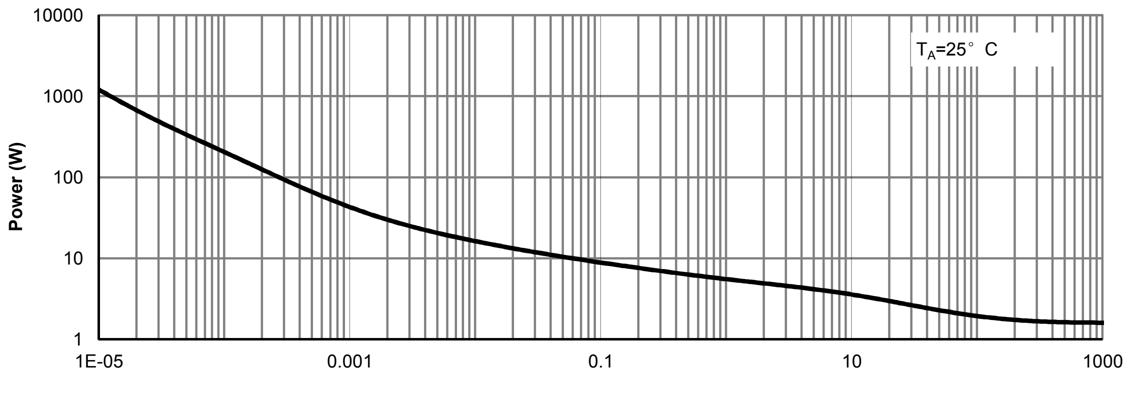


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

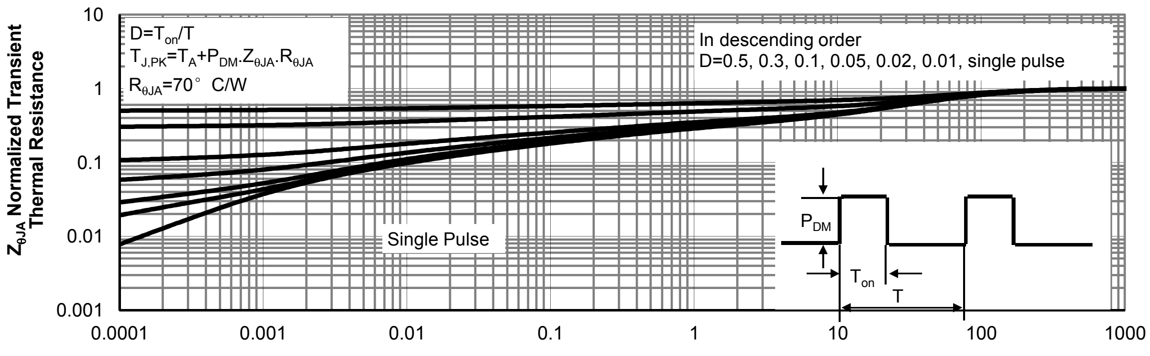


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=-250μA, V_{GS}=0V		-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-48V, V_{GS}=0V				-1	μA
			T_J=55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±25V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=$V_{GS,}$ I_D=-250μA		-1.0	-1.3	-2.0V	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=-10V, I_D=-5A			64	67	mΩ
			T_J=125°C		75	82	
		V_{GS}=-4.5V, I_D=-5A			75	78	mΩ
g_{FS}	Forward Transconductance	V_{DS}=-5V, I_D=-5A			43		S
V_{SD}	Diode Forward Voltage	I_S=-1A, V_{GS}=0V			-0.7	-1.3	V
I_S	Maximum Body-Diode Continuous Current [G]					-16	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-15V, f=1MHz			1995		pF
C_{oss}	Output Capacitance				300		pF
C_{rss}	Reverse Transfer Capacitance				260		pF
R_g	Gate resistance	f=1MHz			4.5	9	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-15V, I_D=-8A			35	50	nC
Q_g(4.5V)	Total Gate Charge				17	25	nC
Q_{gs}	Gate Source Charge				5.7		nC
Q_{gd}	Gate Drain Charge				8.8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-15V, R_L=0.9Ω, R_{GEN}=3Ω			11		ns
t_r	Turn-On Rise Time				7.5		ns
$t_{D(off)}$	Turn-Off DelayTime				43.5		ns
t_f	Turn-Off Fall Time				17.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-16A, di/dt=500A/μs			13.3		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-16A, di/dt=500A/μs			20		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

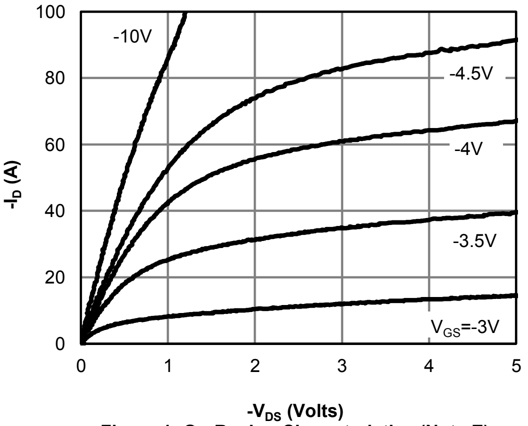


Figure 1: On-Region Characteristics (Note E)

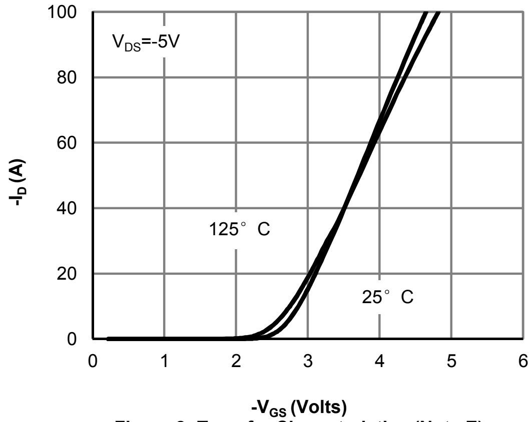


Figure 2: Transfer Characteristics (Note E)

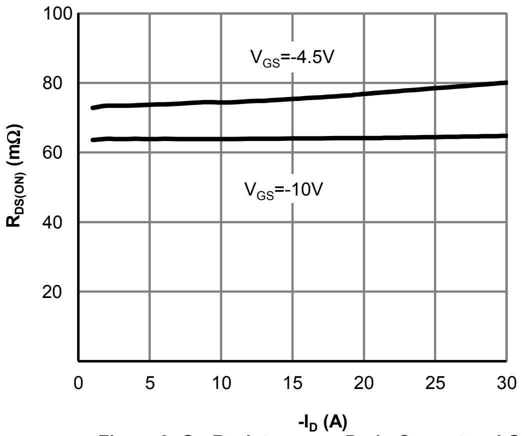


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

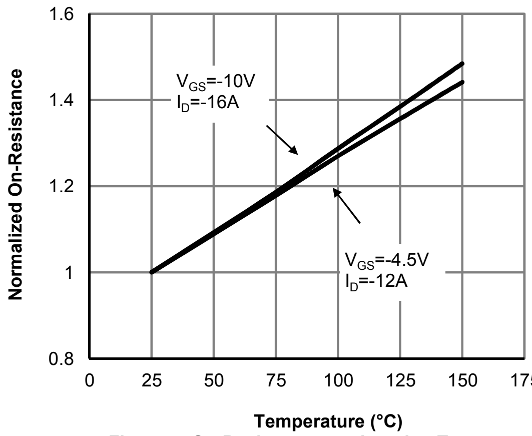


Figure 4: On-Resistance vs. Junction Temperature (Note E)

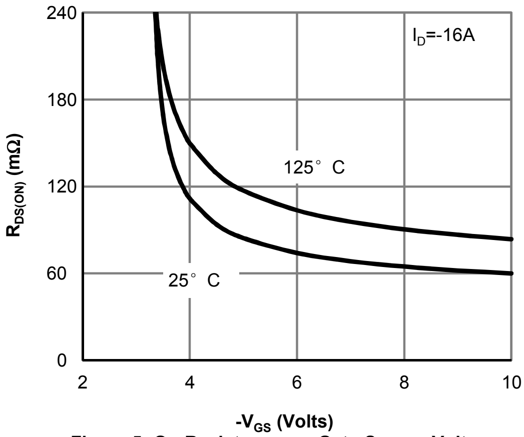


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

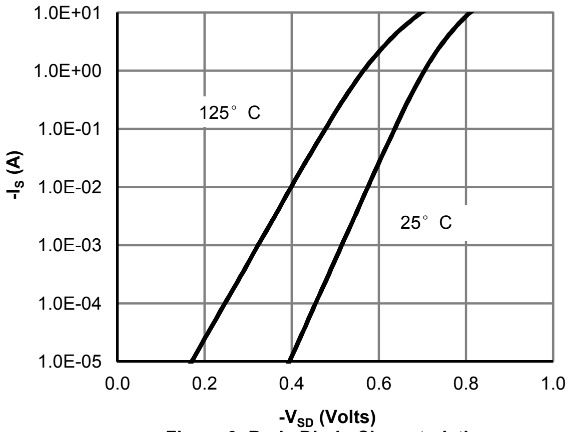


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

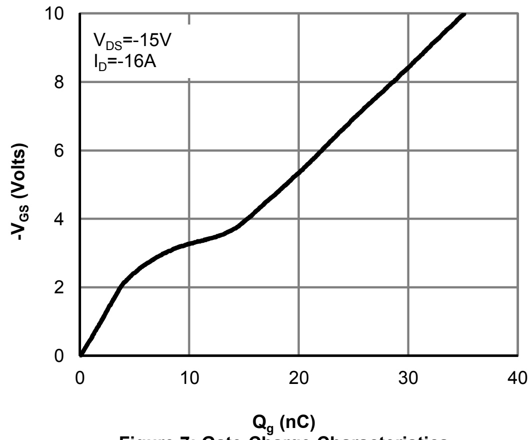


Figure 7: Gate-Charge Characteristics

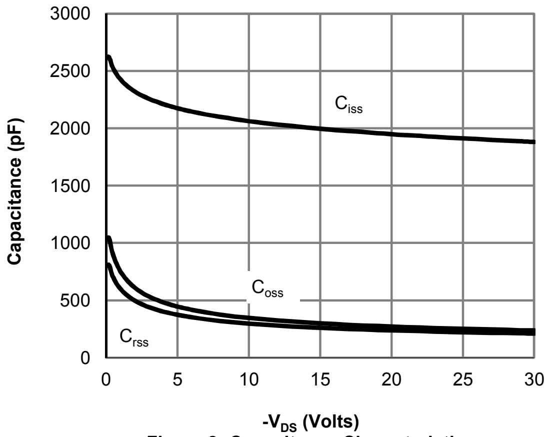
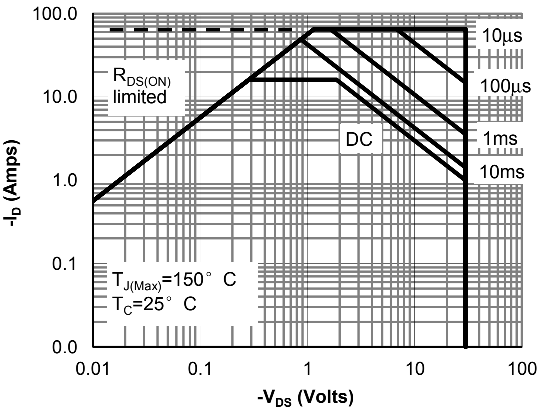


Figure 8: Capacitance Characteristics



$-V_{GS}$> or equal to -4.5V
Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

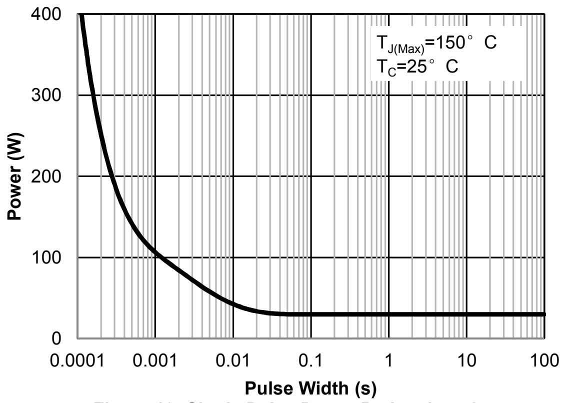


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

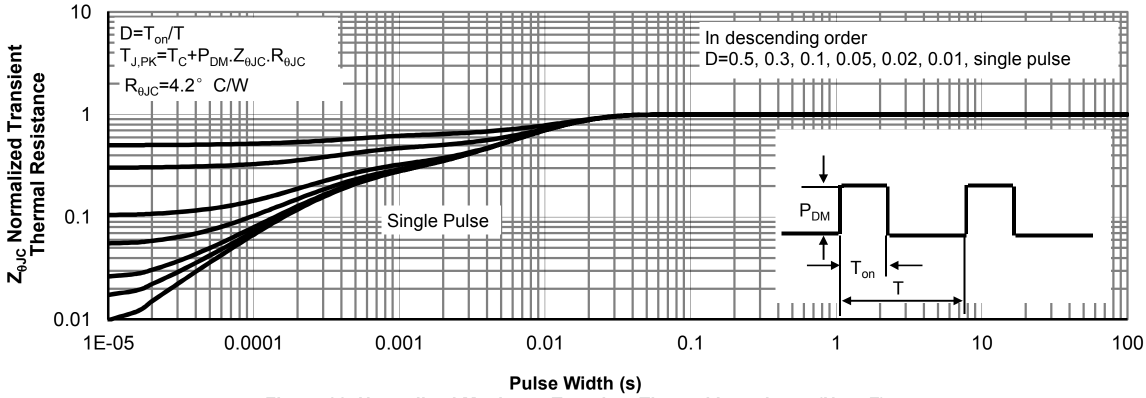


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

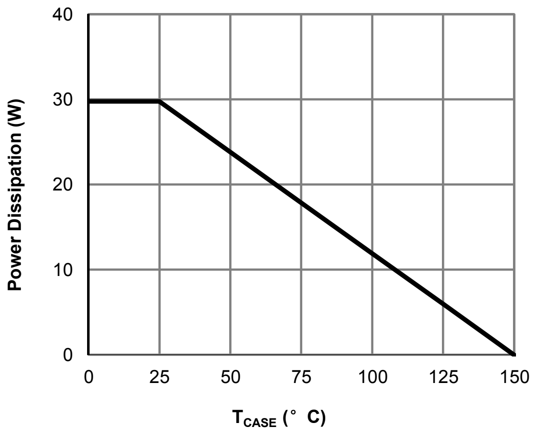


Figure 12: Power De-rating (Note F)

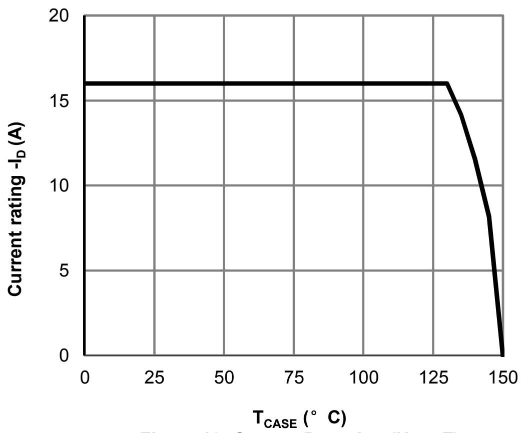


Figure 13: Current De-rating (Note F)

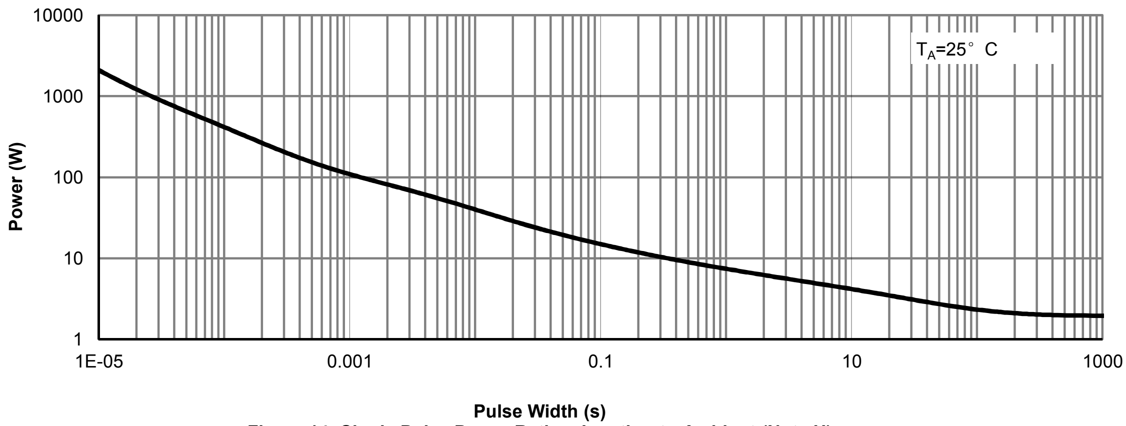


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)

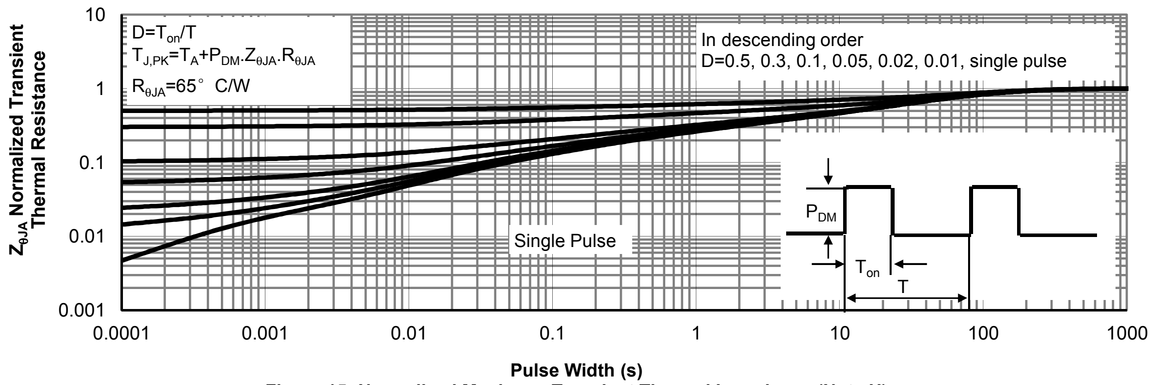


Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)

Figure A: Gate Charge Test Circuit & Waveforms

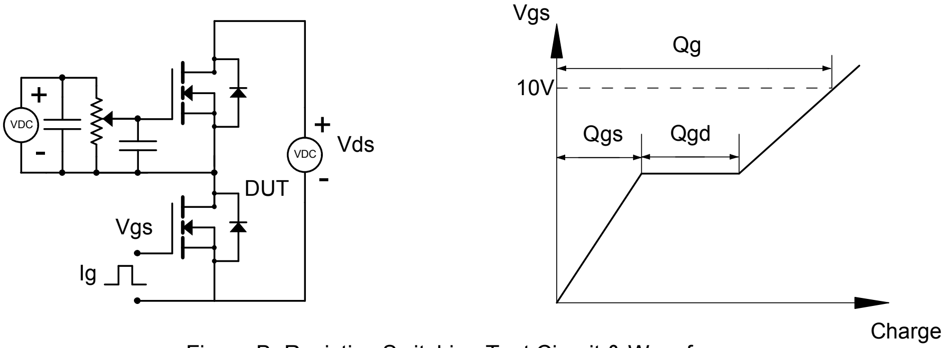


Figure B: Resistive Switching Test Circuit & Waveforms

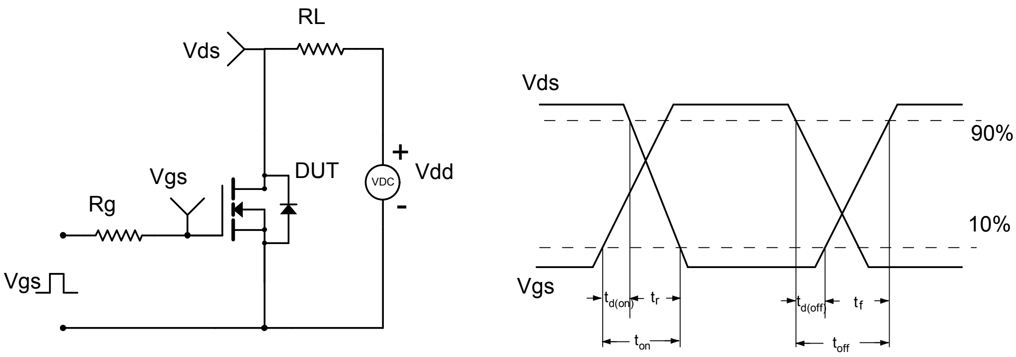


Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

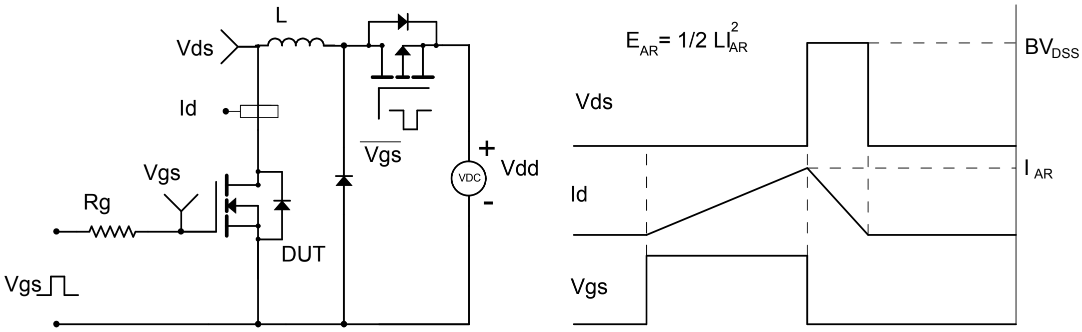
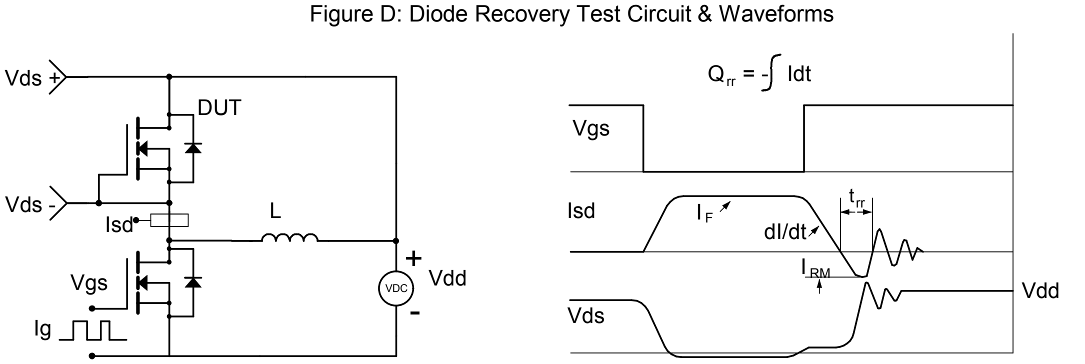
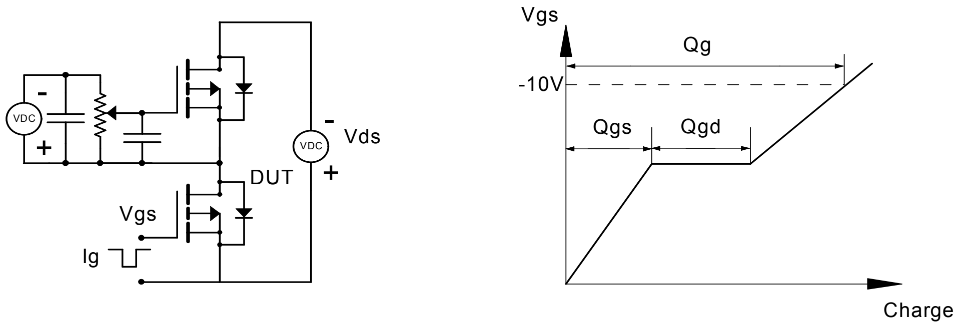


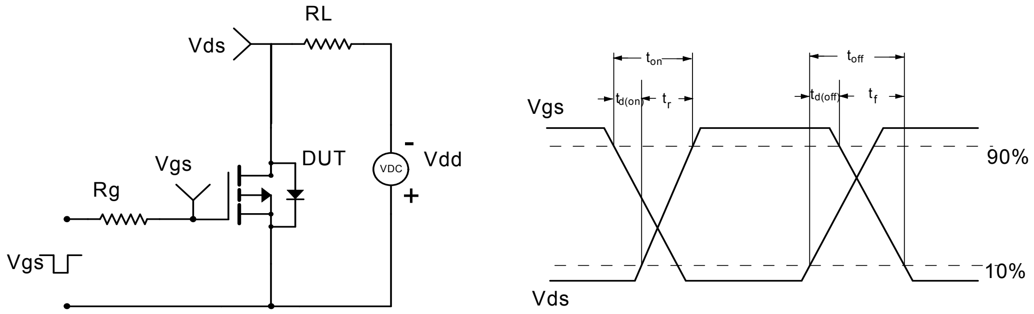
Figure D: Diode Recovery Test Circuit & Waveforms



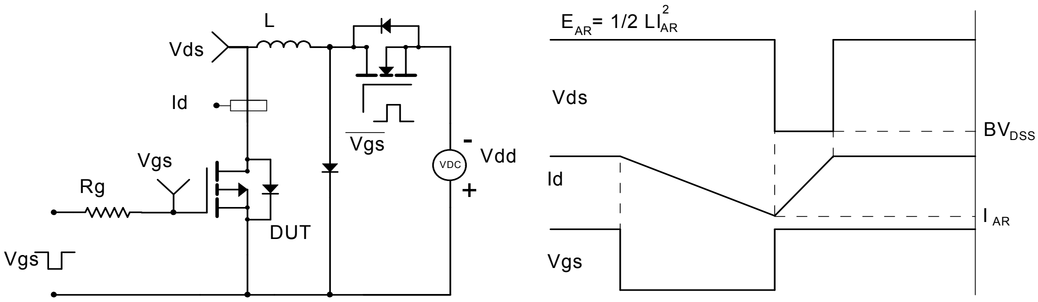
Gate Charge Test Circuit & Waveform



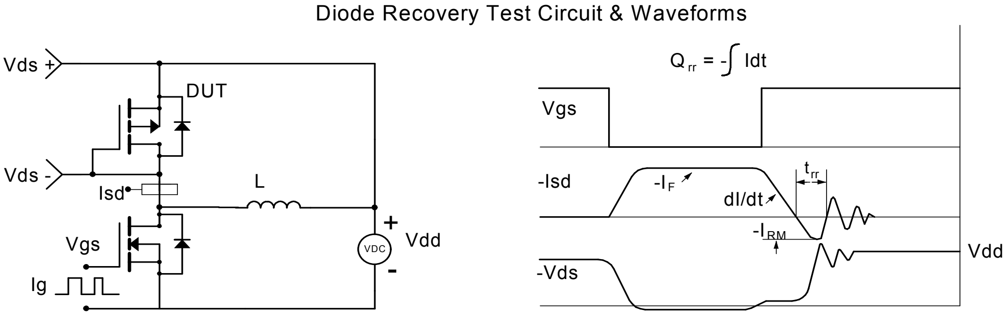
Resistive Switching Test Circuit & Waveforms

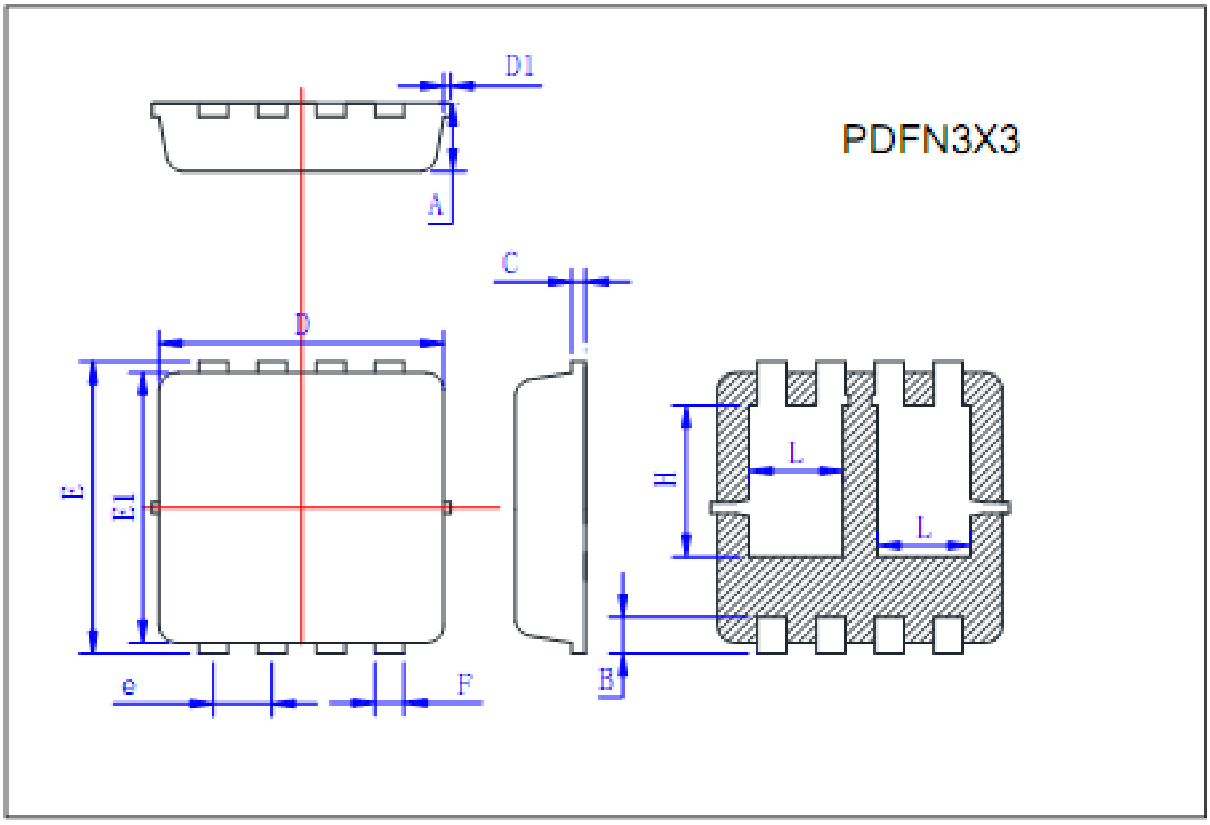


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms





Symbol	Min	Typ	Max
A	0.725	0.775	0.825
B	0.28	0.38	0.48
C	0.13	0.15	0.20
D	3.05	3.15	3.25
D1			0.10
E	3.25	3.35	3.45
E1	3.0	3.1	3.2
e	0.60	0.65	0.70
F	0.27	0.32	0.37
H	1.63	1.73	1.83
L	0.93	1.03	1.13

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