MICRON SEMICONDUCTOR, INC.

MT5LC64K16D4
REVOLUTIONARY PINOUT 64K x 16 SRAM

SRAM

64K x 16 SRAM

3.3V OPERATION WITH OUTPUT ENABLE, REVOLUTIONARY PINOUT

FEATURES

- All I/O pins are 5V tolerant
- Fast access times: 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3Vpower supply
- Individual byte controls for both READ and WRITE cycles
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 10 and 12ns
- Complies to JEDEC low-voltage TTL standards

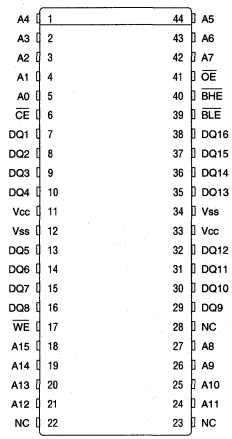
OPTIONS MARKING

- Timing
  - 15ns access -15
  - 20ns access -20
  - 25ns access -25
- Packages
  - 44-pin SOJ (400 mil) DJ
  - 44-pin TSOP (400 mil) TG
- 2V data retention L
- Temperature
  - Commercial (0°C to +70°C) None
  - Industrial (-40°C to +85°C) IT
  - Automotive (-40°C to +125°C) AT
  - Extended (-55°C to +125°C) XT
- Part Number Example: MT5LC64K16D4DJ-20

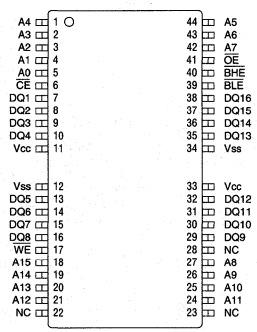
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

44-Pin SOJ (SD-7)



44-Pin TSOP (SE-3)



GENERAL DESCRIPTION

The MT5LC64K16D4 is organized as a 65,536 x 16 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

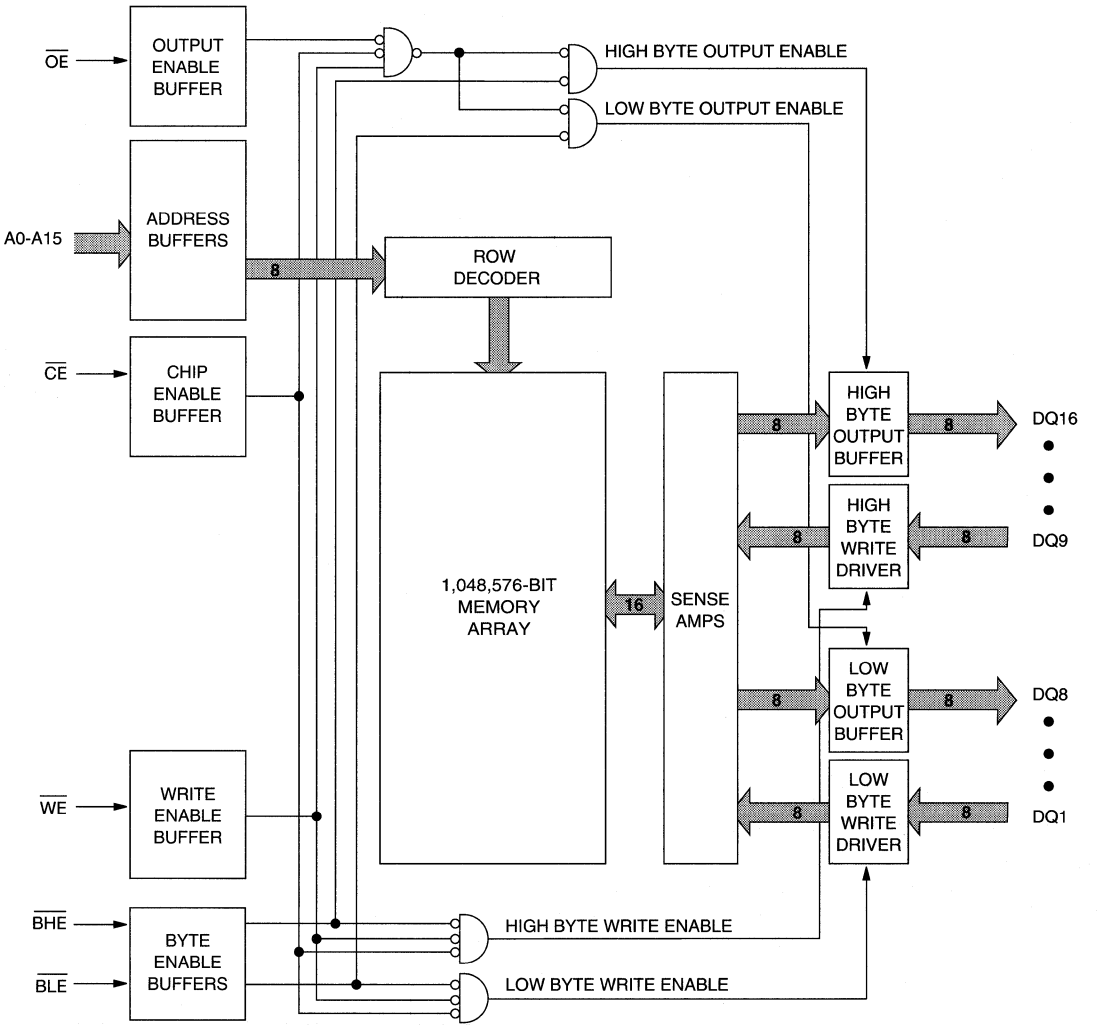
The MT5LC64K16D4 SRAM integrates a 64K x 16 SRAM core with peripheral circuitry consisting of active LOW chip enable, separate upper and lower byte enables and a fast output enable.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls DQ1-DQ8, the lower bits. $\overline{BHE}$ controls DQ9-DQ16, the upper bits.

The MT5LC64K16D4 operates from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

3.3 VOLT SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
5, 4, 3, 2, 1, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19, 18	A0-A15	Input	Address Inputs: These inputs determine which cell is accessed.
17	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
39, 40	$\overline{BLE}$, $\overline{BHE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written or read to the lower byte, DQ1-DQ8. When $\overline{BHE}$ is LOW, data is written or read to the upper byte, DQ9-DQ16.
6	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip automatically goes into standby power mode.
41	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
22, 23, 28	NC	-	No Connect: These signals are not internally connected.
7, 8, 9, 10, 13, 14, 15, 16, 29, 30, 31, 32, 35, 36, 37, 38	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16.
11, 33	Vcc	Supply	Power Supply: +3.3V ±0.3V
12, 34	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH-Z	HIGH-Z	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to 4.6V
V_{IN} ..... -0.5V to +6.0V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; $V_{CC} = 3.3V \pm 0.3V$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	v	

				MAX				
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	60	100	88	80	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	10	20	16	14	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	0.5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1MHz	C_I	6	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 3.3V	$C_{I/O}$	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ± 0.3V)

DESCRIPTION		-15		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle time	^tRC	15		20		25		ns	
Address access time	^tAA		15		20		25	ns	
Chip Enable access time	^tA		15		20		25	ns	
Output hold from address change	^tOH	4		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		ns	6, 7
Chip disable to output in High-Z	^tHZCE		6		8		8	ns	6, 7
Output Enable access time	^tAOE		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	6, 7
Output disable to output in High-Z	^tHZOE		6		8		8	ns	6, 7
Byte Enable access time	^tABE		8		10		12	ns	
Byte Enable to output in Low-Z	^tLZBE	0		0		0		ns	6, 7
Byte disable to output in High-Z	^tHZBE		6		8		8	ns	6, 7
WRITE Cycle									
WRITE cycle time	^tWC	15		20		25		ns	
Chip Enable to end of write	^tCW	12		13		15		ns	
Address valid to end of write	^tAW	9		12		14		ns	
Address setup time	^tAS	0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		ns	
Write pulse width	^tWP	9		10		12		ns	
Data setup time	^tDS	8		10		10		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	1		1		1		ns	6, 7
Write Enable to output in High-Z	^tHZWE		6		8		8	ns	6, 7
Byte Enable to end of write	^tBW	9		12		14		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

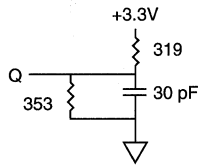


Fig. 1 OUTPUT LOAD EQUIVALENT

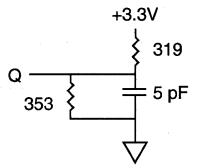


Fig. 2 OUTPUT LOAD EQUIVALENT

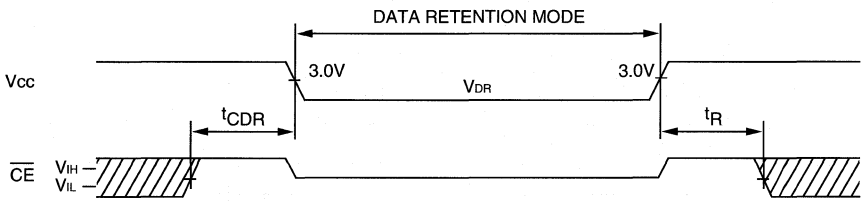
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$, ${}^tHZOE$ is less than ${}^tLZOE$, and ${}^tHZBE$ is less than ${}^tLZBE$.
8. Any combination of write enable, chip enable and byte enable can initiate and terminate a WRITE cycle.
9. $\overline{WE}$ is HIGH for READ cycle.
10. Device is continuously selected. Chip enable is held in its active state.
11. Address valid prior to, or coincident with, the latest occurring chip enable.
12. $\overline{BHE}$ and $\overline{BLE}$ are held in their active state (LOW).
13. The output will be in the High-Z state if output enable is HIGH.
14. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
15. Typical currents are measured at 25°C.

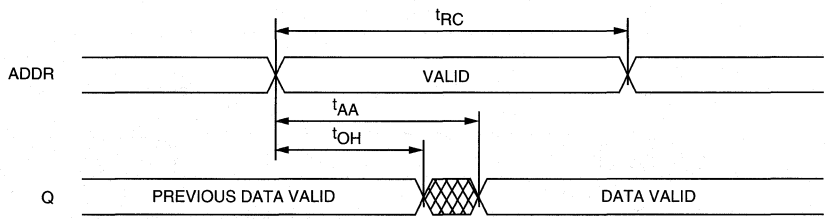
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2			V	
Data Retention Current L version LP version	$\overline{CE} \geq (V_{CC} -0.2V)$ $V_{IN} \geq (V_{CC} -0.2V)$ or $\leq 0.2V$	V_{CC} = 2V	I_{CCDR}		TBD	TBD	µA	15
Chip Deselect to Data Retention Time			${}^tCDR$	0			ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

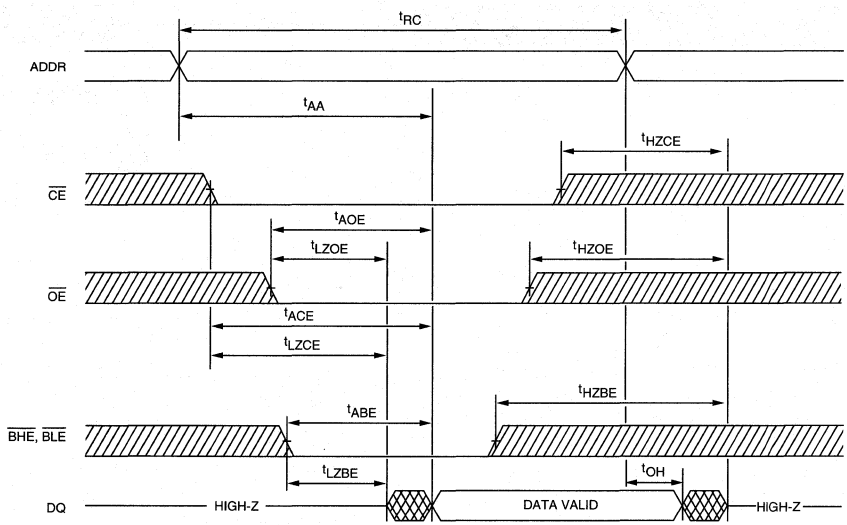
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [9, 10, 12]



READ CYCLE NO. 2 [7, 9]

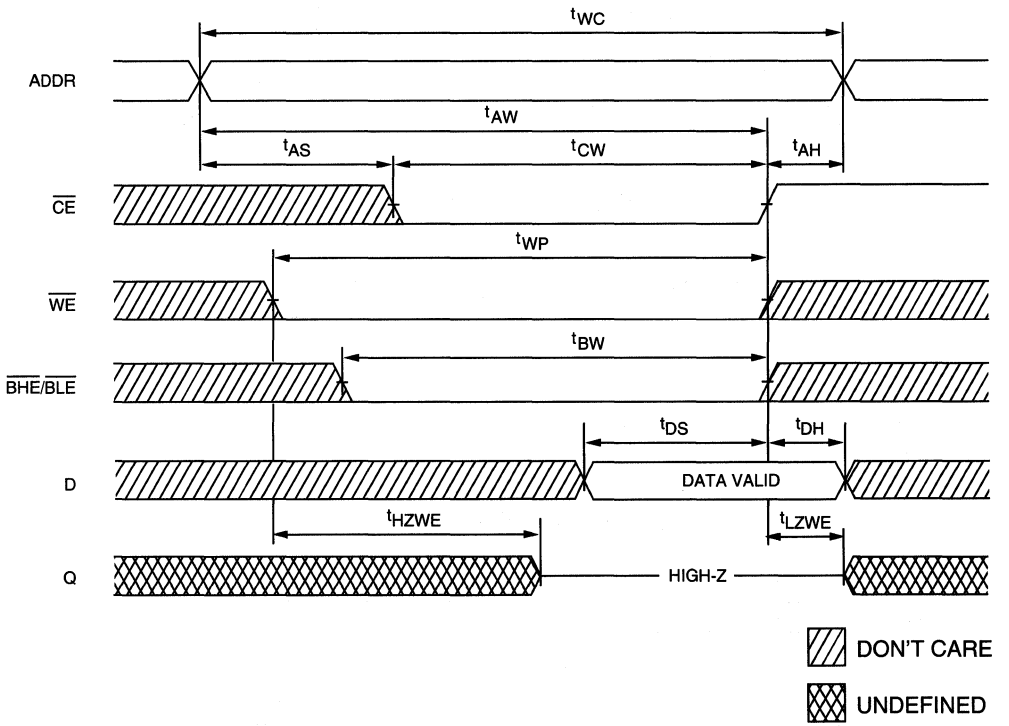


DON'T CARE

UNDEFINED

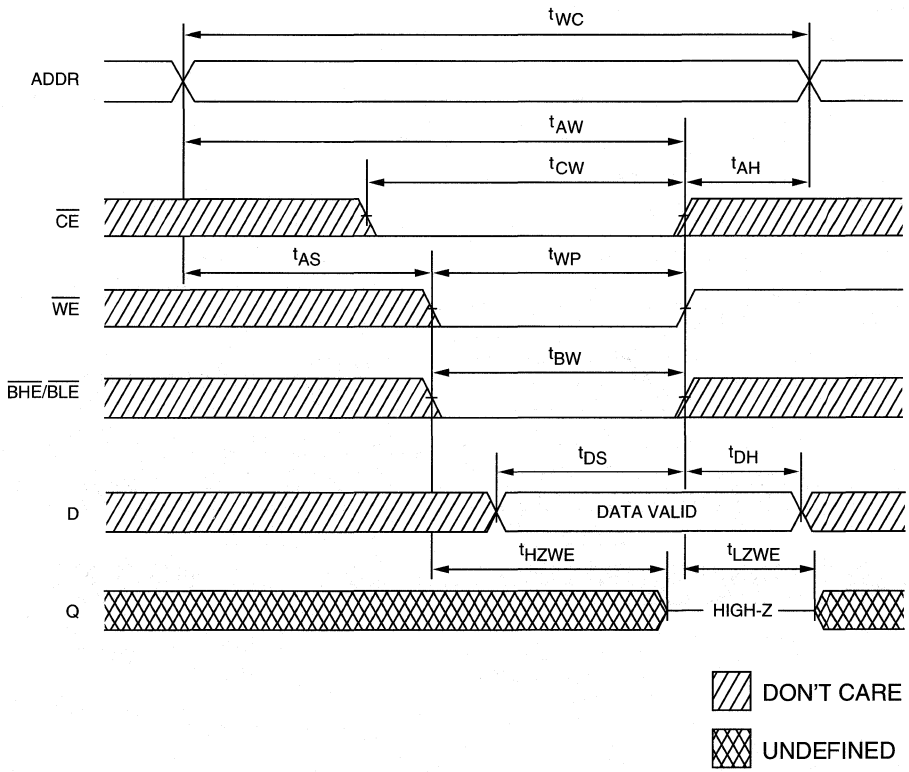
WRITE CYCLE NO. 1 [8, 13]

Chip Enable Controlled



WRITE CYCLE NO. 2 [8, 13]

Write Enable Controlled



WRITE CYCLE NO. 3 [8, 13]

Byte Enable Controlled