



**MT5LC512K8D4  
REVOLUTIONARY PINOUT 512K x 8 SRAM**

# SRAM

# 512K x 8 SRAM

3.3V OPERATION WITH OUTPUT  
ENABLE, REVOLUTIONARY PINOUT

## FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  options
- All inputs and outputs are TTL-compatible
- Fast  $\overline{OE}$  access time: 6, 8, 10, 12 and 15ns
- Complies to JEDEC low-voltage TTL standards

## OPTIONS

- Timing
  - 12ns access
  - 15ns access
  - 20ns access
  - 25ns access
  - 35ns access
- Packages
  - Plastic SOJ (400 mil)
  - Plastic TSOP (400 mil)
- 2V data retention
- Low power
- Temperature
  - Commercial (0°C to +70°C)
  - Industrial (-40°C to +85°C)
  - Automotive (-40°C to +125°C)
  - Extended (-55°C to +125°C)

## MARKING

- |                              |      |
|------------------------------|------|
| 12ns access                  | -12  |
| 15ns access                  | -15  |
| 20ns access                  | -20  |
| 25ns access                  | -25  |
| 35ns access                  | -35  |
| Plastic SOJ (400 mil)        | DJ   |
| Plastic TSOP (400 mil)       | TG   |
| 2V data retention            | L    |
| Low power                    | P    |
| Commercial (0°C to +70°C)    | None |
| Industrial (-40°C to +85°C)  | IT   |
| Automotive (-40°C to +125°C) | AT   |
| Extended (-55°C to +125°C)   | XT   |
- Part number example: MT5LC512K8D4DJ-20 P

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

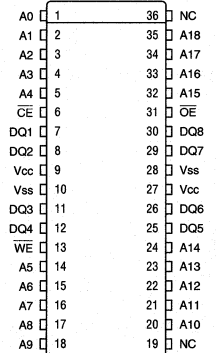
## GENERAL DESCRIPTION

The MT5LC512K8D4 is organized as a 524,288 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

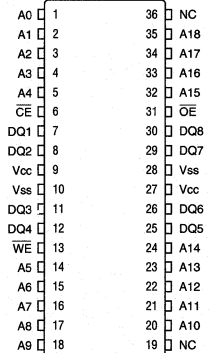
For flexibility in high-speed memory applications, Micron offers chip enable ( $\overline{CE}$ ) and output enable ( $\overline{OE}$ ) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design.

## PIN ASSIGNMENT (Top View)

### 36-Pin SOJ (SD-6)



### 36-Pin TSOP (SE-2)



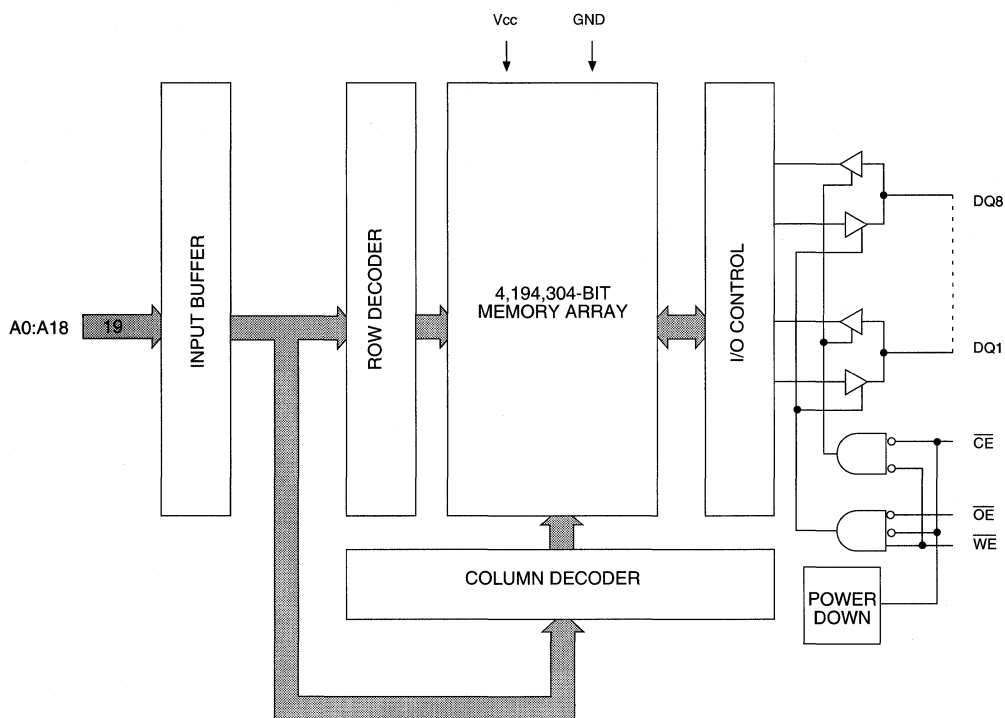
**3.3 VOLT SRAM**

Writing to these devices is accomplished when write enable ( $\overline{WE}$ ) and  $\overline{CE}$  inputs are both LOW. Reading is accomplished when  $\overline{WE}$  remains HIGH and  $\overline{CE}$  goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version also provides a 90 percent reduction in TTL standby current ( $I_{SB1}$ ) through the use of gated inputs, which also facilitate the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

**FUNCTIONAL BLOCK DIAGRAM**



**3.3 VOLT SRAM**

**TRUTH TABLE**

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

**THERMAL IMPEDENCE (EST)<sup>16</sup>**

PACKAGE	NUMBER OF PINS	POWER DISSIPATION (watts)	$\theta_{JC}^*$ ( $^{\circ}\text{C}/\text{W}$ )	$\theta_{JA}^*$ ( $^{\circ}\text{C}/\text{W}$ )
SOJ	36	1.0	15	55
TSOP	36	1.0	5	65

\*The thermal impedance numbers assume the device is socketted on a PC board and air flow is zero.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Vcc Supply Relative to Vss .....	-0.5V to +4.6V
V <sub>IN</sub> .....	-0.5 to +6.0V
Storage Temperature (plastic) .....	-55°C to +150°C
Short Circuit Output Current .....	50mA
Junction Temperature** .....	+150°C

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\*Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS**

(0°C ≤ T<sub>A</sub> ≤ 70°C; V<sub>cc</sub> = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V <sub>IH</sub>	2.2	5.5	V	1, 2
Input Low (Logic 0) Voltage		V <sub>IL</sub>	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>cc</sub>	I <sub>LI</sub>	-1	1	μA	
Output Leakage Current	Output(s) disabled 0V ≤ V <sub>OUT</sub> ≤ V <sub>cc</sub>	I <sub>LO</sub>	-1	1	μA	
Output High Voltage	I <sub>OH</sub> = -4.0mA	V <sub>OH</sub>	2.4		V	1
Output Low Voltage	I <sub>OL</sub> = 8.0mA	V <sub>OL</sub>		0.4	V	1
Supply Voltage		V <sub>cc</sub>	3.0	3.6	V	1

DESCRIPTION	CONDITIONS	SYMBOL	VER	MAX					UNITS	NOTES
				-12	-15	-20	-25	-35		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}$ ; V <sub>cc</sub> = MAX outputs open f = MAX = 1/RC	I <sub>cc</sub>		185	165	160	155	145	mA	3
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}$ ; V <sub>cc</sub> = MAX outputs open f = MAX = 1/RC	I <sub>SB1</sub>	STD	35	30	25	25	20	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	
	I <sub>SB2</sub>	STD	1.0	1.0	1.0	1.0	1.0	mA		
		P	1.0	1.0	1.0	1.0	1.0	mA		
	$\overline{CE} \geq V_{cc} - 0.2V$ ; V <sub>cc</sub> = MAX V <sub>IN</sub> ≥ V <sub>cc</sub> - 0.2V or V <sub>IN</sub> ≤ V <sub>ss</sub> + 0.2V; f = 0									

**CAPACITANCE**

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T <sub>A</sub> = 25°C; f = 1 MHz V <sub>cc</sub> = 3.3V	C <sub>i</sub>	5	pF	4
Output Capacitance		C <sub>o</sub>	7	pF	4



# MT5LC512K8D4 REVOLUTIONARY PINOUT 512K x 8 SRAM

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 13) ( $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ ;  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ )

DESCRIPTION	SYM	-12		-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ Cycle</b>													
READ cycle time	$t_{RC}$	12		15		20		25		35		ns	
Address access time	$t_{AA}$		12		15		20		25		35	ns	
Chip Enable access time	$t_{ACE}$		12		15		20		25		35	ns	
Output hold from address change	$t_{OH}$	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	$t_{LZCE}$	3		3		5		5		5		ns	7
Chip disable to output in High-Z	$t_{HZCE}$		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	$t_{PU}$	0		0		0		0		0		ns	
Chip disable to power-down time	$t_{PD}$		12		15		20		25		35	ns	
Output Enable access time	$t_{AOE}$		6		8		10		12		15	ns	
Output Enable to output in Low-Z	$t_{LZOE}$	0		0		0		0		0		ns	
Output disable to output in High-Z	$t_{HZOE}$		5		6		7		10		12	ns	6
<b>WRITE Cycle</b>													
WRITE cycle time	$t_{WC}$	12		15		20		25		35		ns	
Chip Enable to end of write	$t_{CW}$	8		10		12		15		20		ns	
Address valid to end of write	$t_{AW}$	8		10		12		15		20		ns	
Address setup time	$t_{AS}$	0		0		0		0		0		ns	
Address hold from end of write	$t_{AH}$	0		0		0		0		0		ns	
WRITE pulse width	$t_{WP1}$	8		9		12		15		20		ns	
WRITE pulse width	$t_{WP2}$	9		11		14		17		22		ns	
Data setup time	$t_{DS}$	6		7		8		10		15		ns	
Data hold time	$t_{DH}$	0		0		0		0		0		ns	
Write disable to output in Low-Z	$t_{LZWE}$	3		3		5		5		5		ns	7
Write Enable to output in High-Z	$t_{HZWE}$		5		6		8		10		15	ns	6, 7

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**AC TEST CONDITIONS**

Input pulse levels .....	V <sub>ss</sub> to 3.0V
Input rise and fall times .....	3ns
Input timing reference levels .....	1.5V
Output reference levels .....	1.5V
Output load .....	See Figures 1 and 2

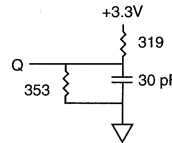


Fig. 1 OUTPUT LOAD EQUIVALENT

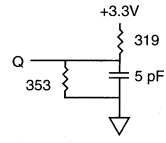


Fig. 2 OUTPUT LOAD EQUIVALENT

**NOTES**

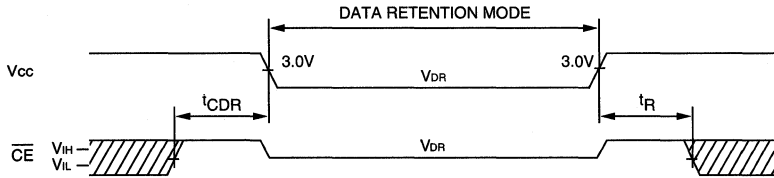
- All voltages referenced to V<sub>ss</sub> (GND).
- Overshoot: V<sub>IH</sub> ≤ +6.0V for t ≤ <sup>t</sup>RC/2  
Undershoot: V<sub>IL</sub> ≥ -2.0V for t ≤ <sup>t</sup>RC/2  
Power-up: V<sub>IH</sub> ≤ +6.0V and V<sub>CC</sub> ≤ 3.1V for t ≤ 200msec.
- I<sub>CC</sub> is dependent on output loading and cycle rates.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- <sup>t</sup>HZCE, <sup>t</sup>HZOE and <sup>t</sup>HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
- At any given temperature and voltage condition, <sup>t</sup>HZCE is less than <sup>t</sup>LZCE and <sup>t</sup>HZWE is less than <sup>t</sup>LZWE.
- $\overline{WE}$  is HIGH for READ cycle.
- Device is continuously selected. All chip enables and output enables are held in their active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- <sup>t</sup>RC = Read Cycle Time.
- Chip enable and write enable can initiate and terminate a WRITE cycle.
- Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
- Output enable ( $\overline{OE}$ ) is inactive (HIGH).
- Output enable ( $\overline{OE}$ ) is active (LOW).
- Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

**3.3 VOLT SRAM**

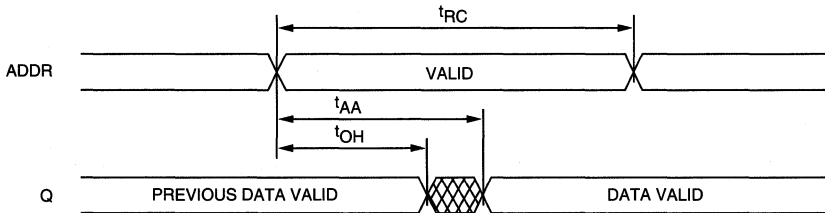
**DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)**

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V <sub>CC</sub> for Retention Data		V <sub>DR</sub>	2		V	
Data Retention Current L version	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or ≤ 0.2V V <sub>CC</sub> = 2V	I <sub>CCDR</sub>		700	μA	
Data Retention Current LP version	$\overline{CE} \geq (V_{CC} - 0.2V)$ V <sub>CC</sub> = 2V	I <sub>CCDR</sub>		700	μA	
Chip Deselect to Data Retention Time		<sup>t</sup> CDR	0		ns	4
Operation Recovery Time		<sup>t</sup> R	<sup>t</sup> RC		ns	4, 11

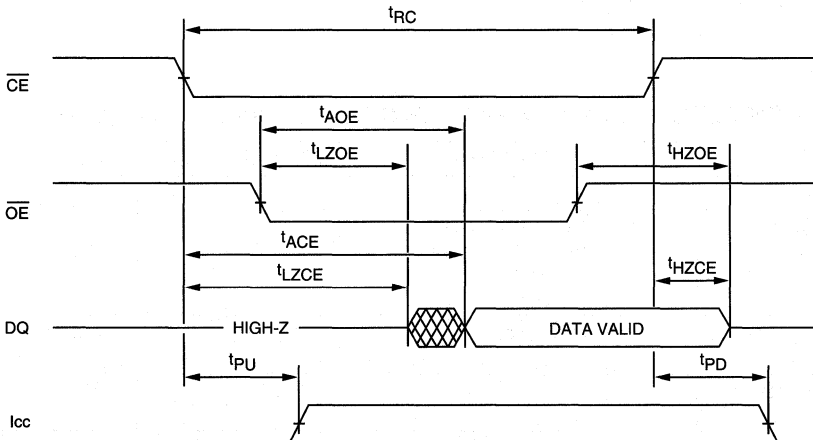
**LOW V<sub>CC</sub> DATA RETENTION WAVEFORM**





**READ CYCLE NO. 1 8, 9**



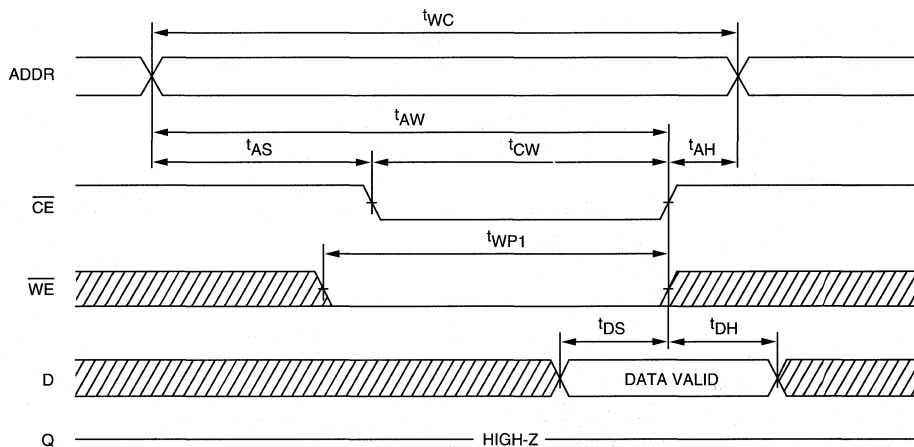
**READ CYCLE NO. 2 7, 8, 10**



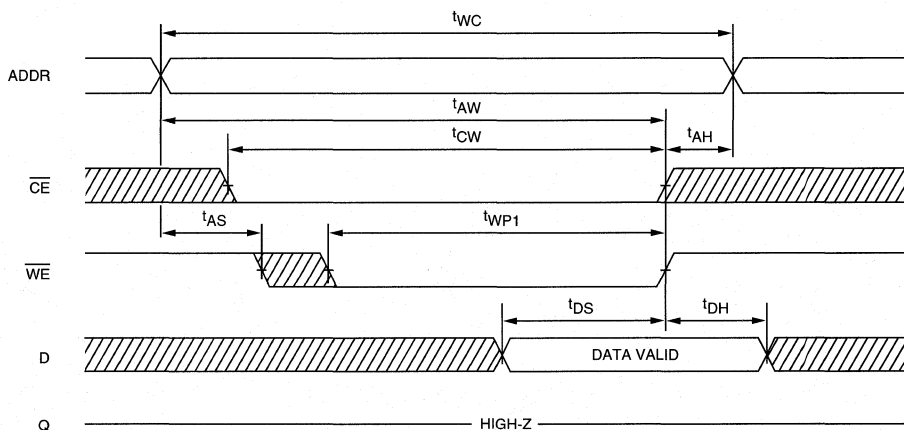
 DON'T CARE  
 UNDEFINED



**3.3 VOLT SRAM**

**WRITE CYCLE NO. 1**<sup>12</sup>  
(Chip Enable Controlled)



**WRITE CYCLE NO. 2**<sup>12, 14</sup>  
(Write Enable Controlled)



 DON'T CARE  
 UNDEFINED

**WRITE CYCLE NO. 3** <sup>7, 12, 15</sup>  
(Write Enable Controlled)

