SRAM

256K x 16 SRAM

3.3V OPERATION WITH OUTPUT ENABLE

FEATURES

- All I/O pins are 5V tolerant
- High speed: 12, 15, 20, 25 and 35ns
- Multiple center power and ground pins for improved noise immunity
- Single +3.3V ±0.3V power supply
- Easy memory expansion with chip enable($\overline{CE}$) and output enable ($\overline{OE}$) options
- All inputs and outputs are TTL-compatible
- Fast $\overline{OE}$ access time: 6, 8, 10, 12, and 15ns
- High-performance, low-power, CMOS double-metal process
- Complies to JEDEC low-voltage TTL standards

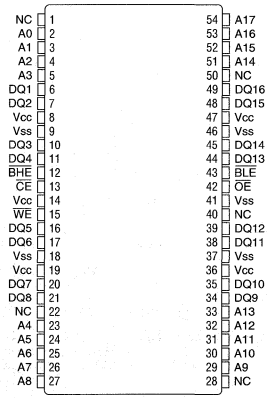
OPTIONS — MARKING

- Timing
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
  - 35ns access — -35
- Packages
  - Plastic SOJ (400 mil) — DJ
  - Plastic TSOP (400 mil) — TG
- 2V data retention — L
- Low power — P
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part number example: MT5LC256K16D4DJ-20 P

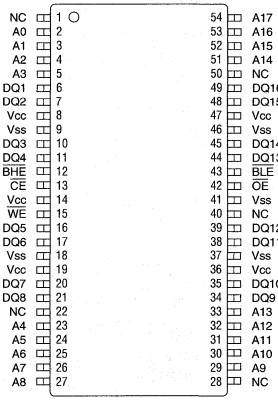
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

54-Pin SOJ* (SD-8)



54-Pin TSOP* (SE-4)



* JEDEC-proposed pinout (0.8mm pitch)

GENERAL DESCRIPTION

The MT5LC256K16D4 is organized as a 262,144 x 16 using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using a double-layer metal, triple-layer polysilicon technology.

This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers $\overline{CE}$ and $\overline{OE}$ capabilities. These enhancements can place the outputs in High-Z for additional flexibility in system design.

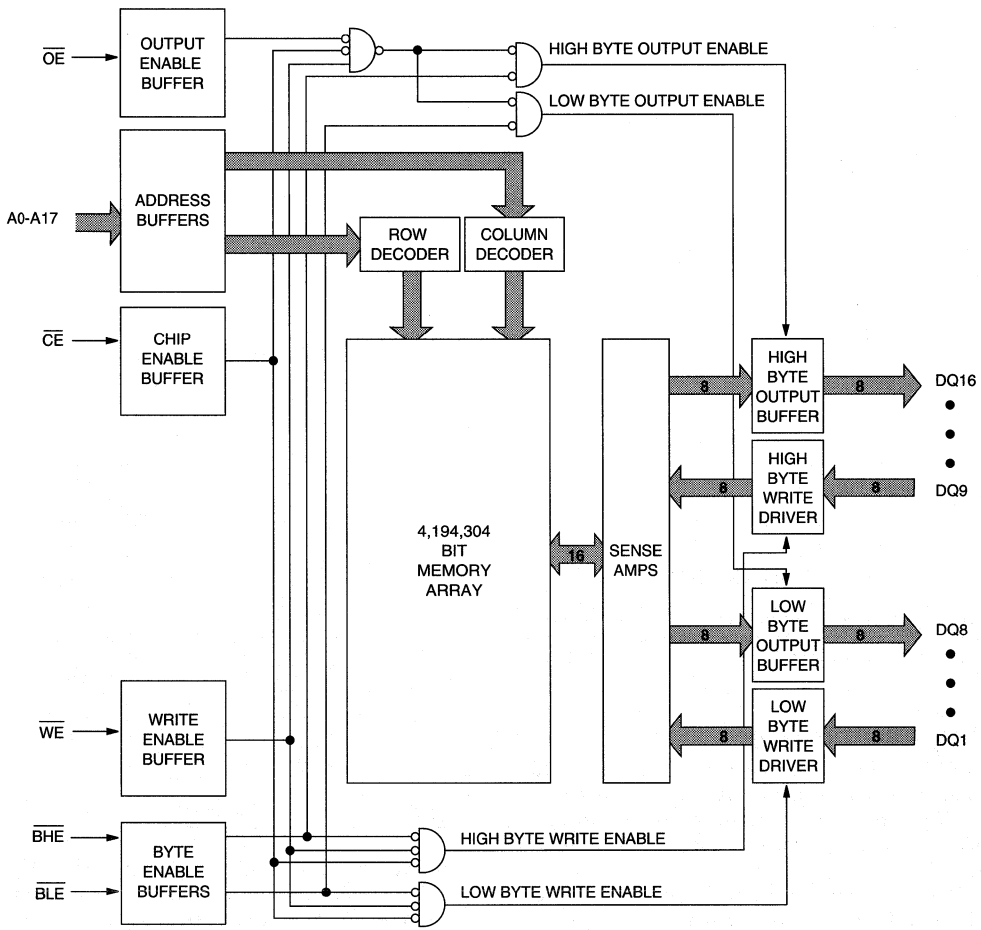
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW and the appropriate byte enables ($\overline{BHE}$ and $\overline{BLE}$) are in their proper states. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW and the appropriate byte enables ($\overline{BHE}$ and $\overline{BLE}$) are in their proper states. The device offers a reduced-power standby mode when disabled. This allows system designers to meet low standby power requirements.

Separate byte enable controls ($\overline{BLE}$ and $\overline{BHE}$) allow individual bytes to be written and read. $\overline{BLE}$ controls the lower bits (DQ1-DQ8). $\overline{BHE}$ controls the upper bits (DQ9-DQ16).

The LP version also provides a 90 percent reduction in TTL standby current (I_{SB1}). This is achieved by including gated inputs on the design. The gated inputs also facilitate the design of battery-backed systems where the designer needs to protect against inadvertent battery current drain during power-down when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL-compatible and 5V tolerant. These low-voltage parts are ideal for mixed 3.3V and 5V systems.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

SOJ and TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
2-5, 23-27, 29-33 51-54	A0-A17	Input	Address Inputs: These inputs determine which cell is accessed.
15	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
12, 43	$\overline{BHE}$, $\overline{BLE}$	Input	Byte Enables: These active LOW inputs allow individual bytes to be written or read. When $\overline{BLE}$ is LOW, data is written to or read from the lower byte, D1-D8. When $\overline{BHE}$ is LOW, data is written to or read from the upper byte, D9-D16.
13	$\overline{CE}$	Input	Chip Enable: This signal is used to enable the device. When $\overline{CE}$ is HIGH, the chip goes into standby power mode.
42	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
1, 22, 28, 40, 50	NC	-	No Connect: These signals are not internally connected.
6, 7, 10, 11, 16, 17, 20, 21, 34, 35, 38, 39, 44, 45, 48, 49	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; upper byte is DQ9-DQ16.
8, 14, 19, 36, 47	Vcc	Supply	Power Supply: +3.3V ±0.3V
9, 18, 37, 41, 46	Vss	Supply	Ground: GND

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	DQ1-DQ8	DQ9-DQ16	POWER
STANDBY	H	X	X	X	X	HIGH-Z	HIGH-Z	STANDBY
LOW BYTE READ (DQ1-DQ8)	L	L	H	L	H	D	HIGH-Z	ACTIVE
HIGH BYTE READ (DQ9-DQ16)	L	L	H	H	L	HIGH-Z	D	ACTIVE
WORD READ (DQ1-DQ16)	L	L	H	L	L	D	D	ACTIVE
WORD WRITE (DQ1-DQ16)	L	X	L	L	L	Q	Q	ACTIVE
LOW BYTE WRITE (DQ1-DQ8)	L	X	L	L	H	Q	HIGH-Z	ACTIVE
HIGH BYTE WRITE (DQ9-DQ16)	L	X	L	H	L	HIGH-Z	Q	ACTIVE
OUTPUT DISABLE	L	H	H	X	X	HIGH-Z	HIGH-Z	ACTIVE
	L	X	X	H	H	HIGH -Z	HIGH-Z	ACTIVE

THERMAL IMPEDENCE (EST)[18]

PACKAGE	NUMBER OF PINS	POWER DISSIPATION (watts)	θ_{JC}* (°C/W)	θ_{JA}* (°C/W)
SOJ	54	1.0	15	55
TSOP	54	1.0	5	65

*The thermal impedence numbers assume the device is socketted on a PC board and air flow is zero.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} .....-0.5V to +4.6V
V_{IN}.....-0.5 to +6.0V
Storage Temperature (plastic) .....-55°C to +150°C
Short Circuit Output Current 50mA
Junction Temperature** .....+150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this data sheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX						
DESCRIPTION	CONDITIONS	SYMBOL	VER	-12	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{CC}	ALL	185	165	160	155	145	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC outputs open	I_{SB1}	STD	35	30	25	25	20	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IN} \le V_{SS}$ +0.2V or $V_{IN} \ge V_{CC}$ -0.2V; f = 0	I_{SB2}	STD	1.0	1.0	1.0	1.0	1.0	mA	
			P	1.0	1.0	1.0	1.0	1.0	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes 5, 15) ($0°C \le T_A \le 70°C$; V_{CC} = 3.3V ±0.3V)

DESCRIPTION		-12		-15		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle													
READ cycle time	tRC	12		15		20		25		35		ns	
Address access time	tAA		12		15		20		25		35	ns	
Chip Enable access time	tACE		12		15		20		25		35	ns	
Output hold from address change	tOH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	tLZCE	3		3		5		5		5		ns	7
Chip disable to output in High-Z	tHZCE		6		7		8		10		15	ns	6, 7
Chip Enable to power-up time	tPU	0		0		0		0		0		ns	
Chip disable to power-down time	tPD		12		15		20		25		35	ns	
Output Enable access time	tAOE		6		8		10		12		15	ns	
Output Enable to output in Low-Z	tLZOE	0		0		0		0		0		ns	
Output disable to output in High-Z	tHZOE		5		6		7		10		12	ns	6
Byte Enable access time	tABE		7		8		10		12		15	ns	
Byte Enable to output in Low-Z	tLZBE	0		0		0		0		0		ns	
Byte Enable to output in High-Z	tHZBE		7		8		8		8		10	ns	
WRITE Cycle													
WRITE cycle time	tWC	12		15		20		25		35		ns	
Chip Enable to end of WRITE	tCW	8		10		12		15		20		ns	
Address valid to end of WRITE	tAW	8		10		12		15		20		ns	
Address setup time	tAS	0		0		0		0		0		ns	
Address hold from end of WRITE	tAH	0		0		0		0		0		ns	
WRITE pulse width	tWP1	8		9		12		15		20		ns	
WRITE pulse width	tWP2	9		11		14		17		22		ns	
Data setup time	tDS	6		7		8		10		15		ns	
Data hold time	tDH	0		0		0		0		0		ns	
Write disable to output in Low-Z	tLZWE	3		3		5		5		5		ns	7
Write Enable to output in High-Z	tHZWE		5		6		8		10		15	ns	6, 7
Byte Enable to end of WRITE	tBW	8		9		12		14		18		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

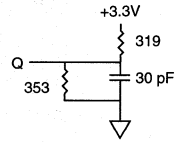


Fig. 1 OUTPUT LOAD EQUIVALENT

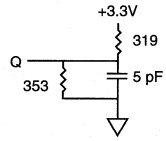


Fig. 2 OUTPUT LOAD EQUIVALENT

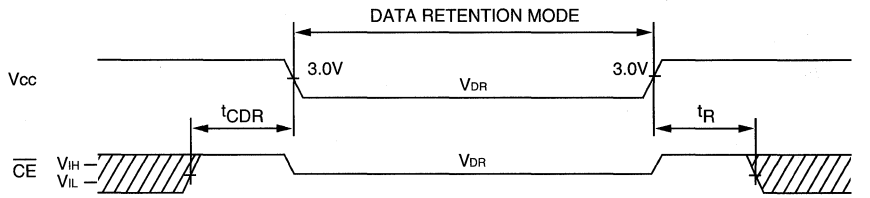
NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tRC/2$
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tRC/2$
   Power-up: $V_{IH} \leq +6.0V$ and $V_{CC} \leq 3.1V$ for $t \leq 200msec$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$, ${}^tHZBE$ and ${}^tHZWE$ are specified with CL = 5pF as in Fig. 2. Transition is measured ±200mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ${}^tRC$ = READ cycle time.
12. Chip enable, write enable and byte enables can initiate and terminate a WRITE cycle.
13. $\overline{BLE}$ and $\overline{BLH}$ determine what outputs are active during the READ cycle.
14. The output will be in a High-Z state if $\overline{OE}$ is HIGH.
15. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
16. Output enable ($\overline{OE}$) is inactive (HIGH).
17. Output enable ($\overline{OE}$) is active (LOW).
18. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

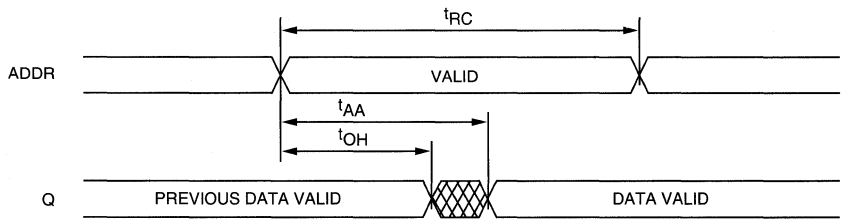
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2		V	
Data Retention Current L version	$\overline{CE} \geq (Vcc - 0.2V)$ $V_{IN} \geq (Vcc - 0.2V)$ or ≤ 0.2V Vcc = 2V	I_{CCDR}		700	µA	
Data Retention Current LP version	$\overline{CE} \geq (Vcc - 0.2V)$ Vcc = 2V	I_{CCDR}		700	µA	
Chip Deselect to Data Retention Time		${}^tCDR$	0		ns	4
Operation Recovery Time		${}^tR$	${}^tRC$		ns	4, 11

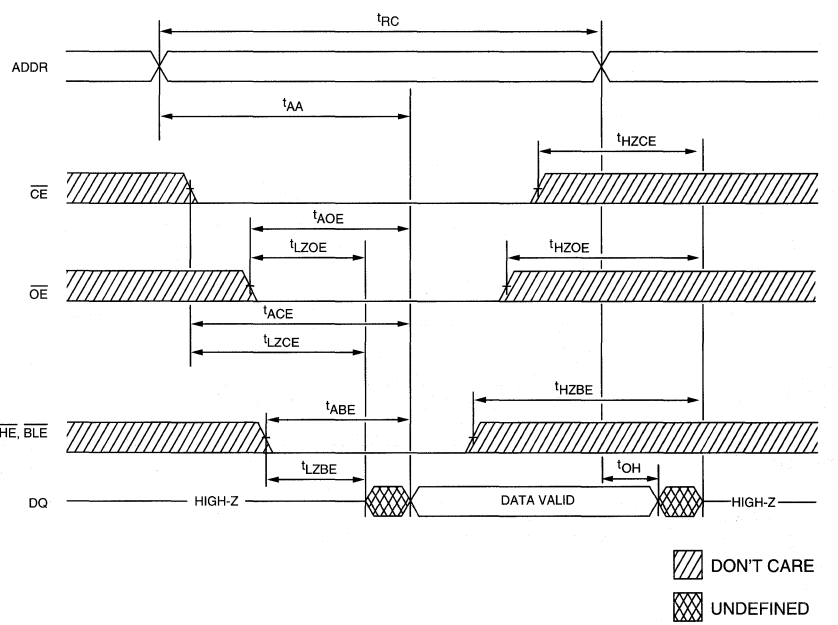
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9, 13]

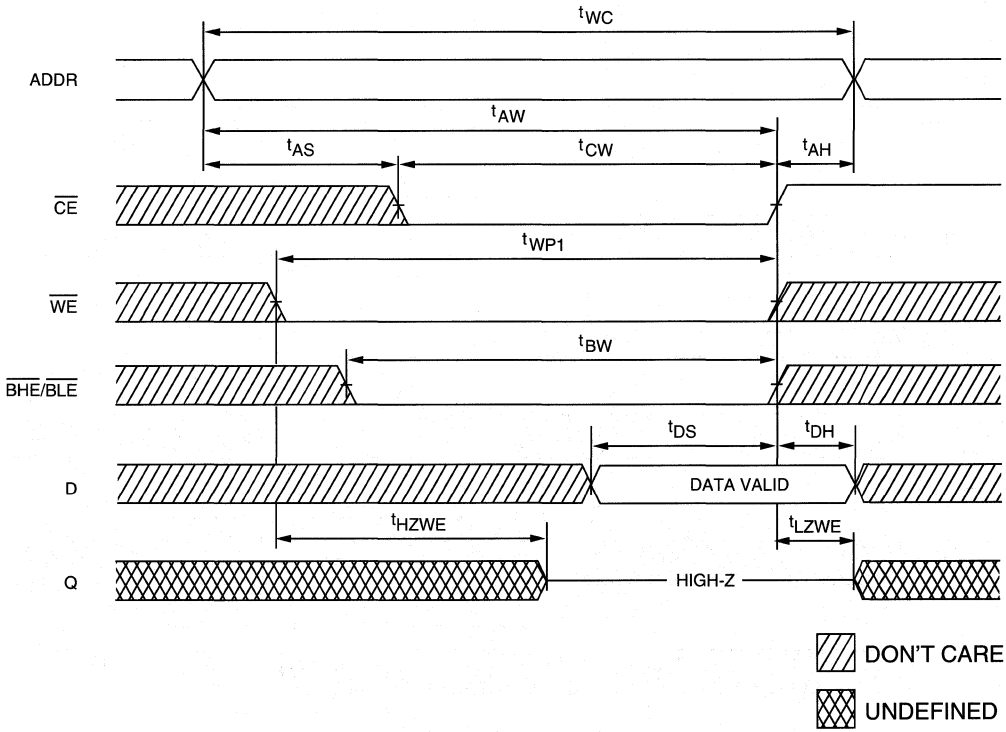


READ CYCLE NO. 2 [7, 8, 10]

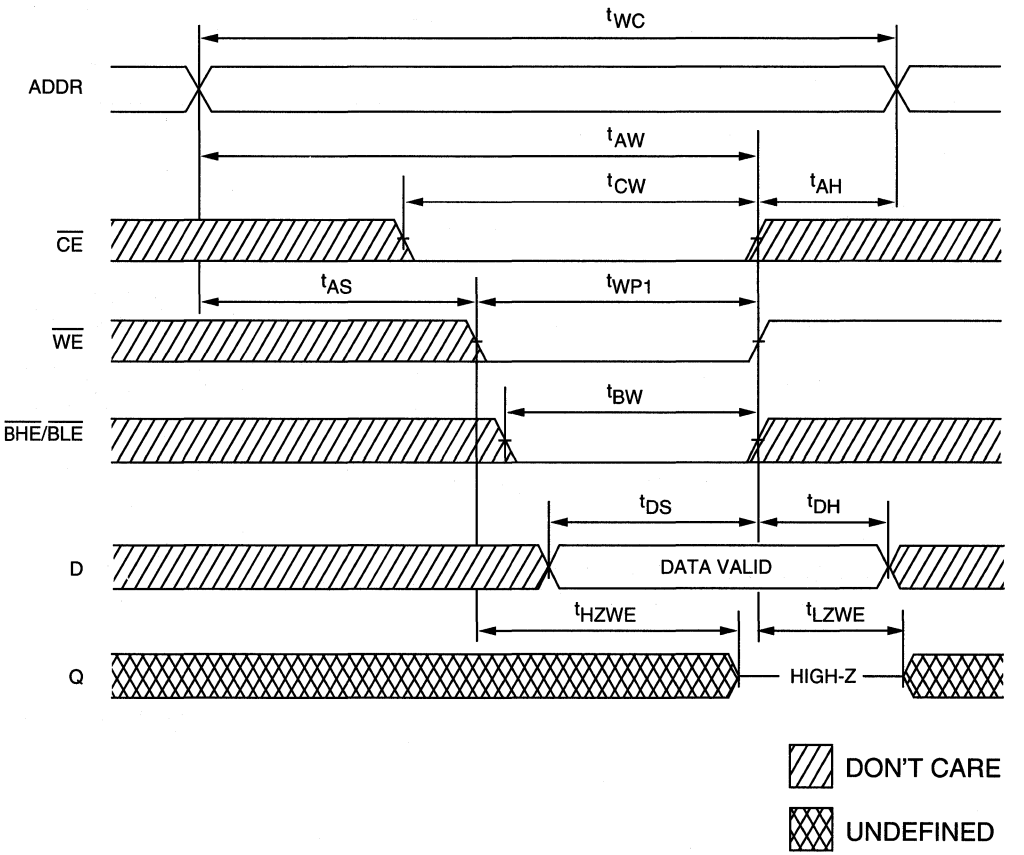


WRITE CYCLE NO. 1 [12,14]

(Chip Enable Controlled)

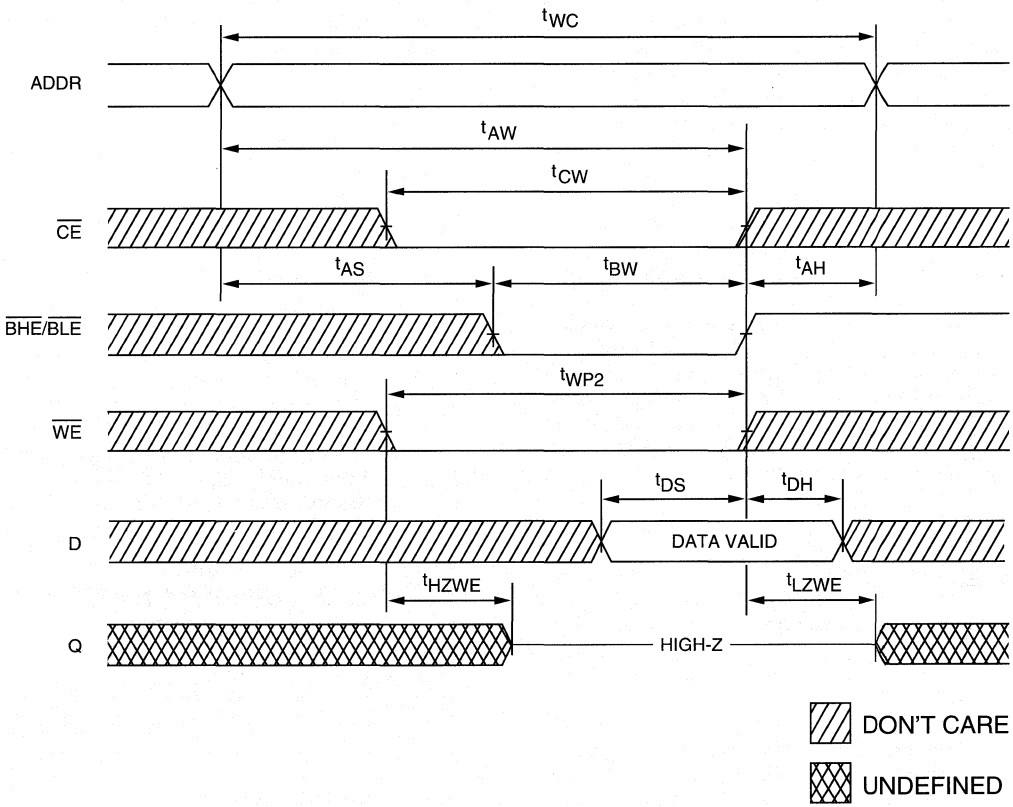


WRITE CYCLE NO. 2 [7, 12, 14, 16]
(Write Enable Controlled)



WRITE CYCLE NO. 3 [7, 12, 14, 17]

(Write Enable Controlled)



APPLICATION INFORMATION

THERMAL CONSIDERATIONS

This section describes how to determine the junction temperature during operating conditions. It is essential that the maximum junction temperature of the 4 Meg SRAM is not exceeded. If this temperature is exceeded it is necessary to add external cooling such as forced airflow or change the operating conditions. The maximum junction temperature for Micron SRAMs is 150°C. The limiting temperature factor is not the SRAM but the mold compound which prevents reliable operating temperatures significantly about 150°C. However, it is advisable to run the part as cool as possible since reliability (FIT rates) are exponentially dependent upon junction temperature.

The calculation of the actual junction temperature begins with the power calculation and then the junction temperation calculation. Equations 1 and 2 below show how T_j is determined using the ambient temperature, thermal resistance and operating power. If an airflow is introduced into a system then Equation 2 should be used with an airflow thermal multiplier. Specific thermal resistances are given in Micron technical note "SRAM Thermal Design Considerations" and in individual data sheets.

$$T_j = T_A + P * \theta_{JA} \quad (1)$$

$$T_j = T_A + P * \theta_{JA} * \theta_M \quad (2)$$

T_j = Junction temperature of the active portion of the silicon die (°C)
T_A = Ambient air temperature (°C) at which the device is operated
P = Average power dissipation of the device (W)
θ_{JA} = Junction to ambient thermal resistance (°C/W)
θ_M = Airflow multiplier. This value changes for different values of airflow over the part (fpm).

To solve the above equations the average operating power must be calculated. Total power has three separate components (P_1, P_2 and P_3). P_1 is the operating power dissipated by the chip, P_2 is the AC output power due to the capacitive load and P_3 is the DC output power due to TTL DC load current (P_3 is usually negligible). For this example we have chosen P_2 such that outputs are switching from a logic LOW state to a logic HIGH state which gives the worst case output AC current. A complete description of these equations and their derivation is given in Micron technical note "Design Tips: 32K x 36 SRAM."

$$P_1 = V_{CC} I_{CC}$$

$$P_2 = \frac{C_L}{T} (V_{CC} [V_{OH} - V_{OL}] - 0.5 [V_{OH}^2 - V_{OL}^2]) N_S$$

$$P_3 = (V_{CC} - V_{OH}) I_O N_H + V_{OL} I_I N_L.$$

V_{CC} = Supply voltage
I_{CC} = Supply current
C_L = Capacitive output loading
T = Clock period
V_{OH} = Output high voltage
V_{OL} = Output low voltage
I_O = Output current on DQ lines which are high
I_I = Input current on DQ lines which are low
N_H = Number of DQ lines which are high
N_L = Number of DQ lines which are low.

Table 1
EFFECTS OF AIRFLOW ON 4 MEG SRAM SOJ PACKAGES

Package	Air Flow	θ_M Multiplier
PSOJ	200 fpm	0.7 - 0.75
PSOJ	500 fpm	0.55 - 0.65

ADDITIONAL INFORMATION

For more information on thermal considerations see Micron's technical notes, "SRAM Thermal Design Considerations" and "Design Tips: 32K x 36 SRAM." These notes explain how to calculate thermal resistance and how to improve thermal performance in much greater detail. Also available is Micron's *Quality and Reliability Handbook*, which gives an explanation of how thermal impedances are calculated.