# SRAM

# 8K x 8 SRAM



## FEATURES

- High speed: 9, 10, 12, 15, 20 and 25ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL-compatible

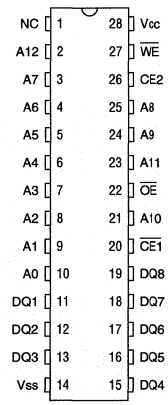
## OPTIONS — MARKING

- Timing
  - 9ns access — -9
  - 10ns access — -10
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
  - 25ns access — -25
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
- 2V data retention — L
- Temperature
  - Commercial (0°C to +70°C) — None
  - Industrial (-40°C to +85°C) — IT
  - Automotive (-40°C to +125°C) — AT
  - Extended (-55°C to +125°C) — XT
- Part Number Example: MT5C6408DJ-15 AT

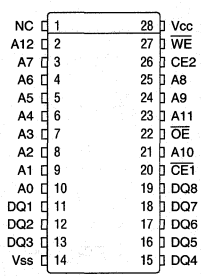
NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

## PIN ASSIGNMENT (Top View)

### 28-Pin DIP (SA-4)




### 28-Pin SOJ (SD-2)




## GENERAL DESCRIPTION

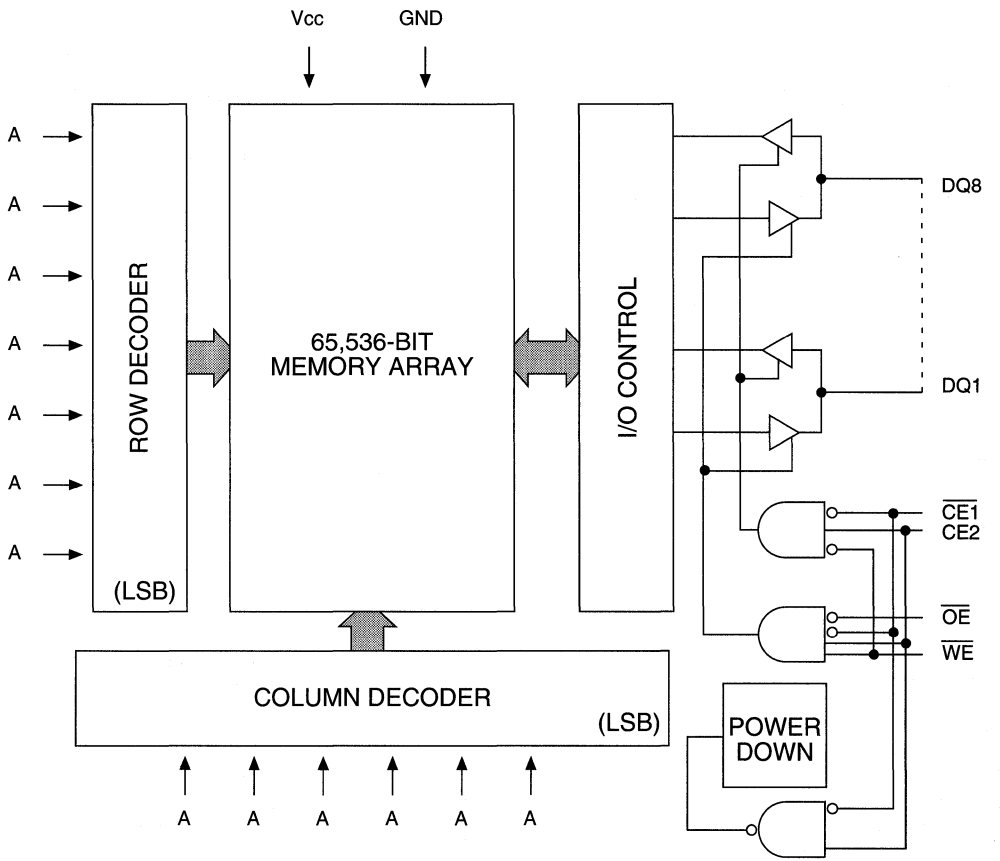
The MT5C6408 is organized as a 8,192 x 8 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers two chip enables and an output enable on the x8 organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to achieve their low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

## FUNCTIONAL BLOCK DIAGRAM




## TRUTH TABLE

| MODE | $\overline{CE1}$ | CE2 | $\overline{WE}$ | $\overline{OE}$ | DQ | POWER |
|---|---|---|---|---|---|---|
| STANDBY | H | X | X | X | HIGH-Z | STANDBY |
| STANDBY | X | L | X | X | HIGH-Z | STANDBY |
| READ | L | H | H | L | Q | ACTIVE |
| NOT SELECTED | L | H | H | H | HIGH-Z | ACTIVE |
| WRITE | L | H | L | X | D | ACTIVE |

## ABSOLUTE MAXIMUM RATINGS*

Voltage on $V_{CC}$ supply relative to $V_{SS}$ ..... -1V to +7V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation ..... 1W
Short Circuit Output Current ..... 50mA
Voltage on Any Pin Relative to $V_{SS}$ ..... -1V to $V_{CC}$ +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ $T_A$ ≤ 70°C; Vcc = 5V ±10%)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input High (Logic 1) Voltage | | $V_{IH}$ | 2.2 | $V_{CC}$ +1 | V | 1 |
| Input Low (Logic 0) Voltage | | $V_{IL}$ | -0.5 | 0.8 | V | 1, 2 |
| Input Leakage Current | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ | $I_{LI}$ | -5 | 5 | µA | |
| Output Leakage Current | Output(s) disabled 0V ≤ $V_{OUT}$ ≤ $V_{CC}$ | $I_{LO}$ | -5 | 5 | µA | |
| Output High Voltage | $I_{OH}$ = -4.0mA | $V_{OH}$ | 2.4 | | V | 1 |
| Output Low Voltage | $I_{OL}$ = 8.0mA | $V_{OL}$ | | 0.4 | V | 1 |
| Supply Voltage | | $V_{CC}$ | 4.5 | 5.5 | V | 1 |

| | | | | MAX | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DESCRIPTION | CONDITIONS | SYMBOL | TYP | -9 | -10 | -12 | -15 | -20 | -25 | UNITS | NOTES |
| Power Supply Current: Operating | $\overline{CE}$ ≤ $V_{IL}$; $V_{CC}$ = MAX f = MAX = 1/ $^tRC$ outputs open | $I_{CC}$ | 125 | 190 | 185 | 175 | 165 | 140 | 130 | mA | 3, 14 |
| Power Supply Current: Standby | $\overline{CE}$ ≥ $V_{IH}$; $V_{CC}$ = MAX f = MAX = 1/ $^tRC$ outputs open | $I_{SB1}$ | 22 | 60 | 50 | 45 | 40 | 35 | 35 | mA | 14 |
| | $\overline{CE}$ ≥ $V_{CC}$ -0.2V; $V_{CC}$ = MAX $V_{IN}$ ≤ $V_{SS}$ +0.2V or $V_{IN}$ ≥ $V_{CC}$ -0.2V; f = 0 | $I_{SB2}$ | 0.5 | 3 | 3 | 3 | 3 | 3 | 5 | mA | 14 |

## CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| Input Capacitance | $T_A$ = 25°C; f = 1 MHz | $C_I$ | 5 | pF | 4 |
| Output Capacitance | $V_{CC}$ = 5V | $C_O$ | 7 | pF | 4 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ $T_A$ ≤ 70°C; Vcc = 5V ±10%)

| DESCRIPTION | | -9 | | -10 | | -12 | | -15 | | -20 | | -25 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SYM | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| **READ Cycle** | | | | | | | | | | | | | | | |
| READ cycle time | $^tRC$ | 9 | | 10 | | 12 | | 15 | | 20 | | 25 | | ns | |
| Address access time | $^tAA$ | | 9 | | 10 | | 12 | | 15 | | 20 | | 25 | ns | |
| Chip Enable access time | $^tACE$ | | 9 | | 9 | | 10 | | 12 | | 15 | | 20 | ns | |
| Output hold from address change | $^tOH$ | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | | ns | |
| Chip Enable to output in Low-Z | $^tLZCE$ | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns | 7, 15 |
| Chip disable to output in High-Z | $^tHZCE$ | | 5 | | 5 | | 6 | | 7 | | 8 | | 8 | ns | 6, 7 |
| Chip Enable to power-up time | $^tPU$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Chip disable to power-down time | $^tPD$ | | 9 | | 10 | | 12 | | 15 | | 20 | | 25 | ns | |
| Output Enable access time | $^tAOE$ | | 4.5 | | 5 | | 6 | | 7 | | 8 | | 8 | ns | |
| Output Enable to output in Low-Z | $^tLZOE$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Output disable to output in High-Z | $^tHZOE$ | | 4.5 | | 5 | | 5 | | 6 | | 7 | | 8 | ns | 6 |
| **WRITE Cycle** | | | | | | | | | | | | | | | |
| WRITE cycle time | $^tWC$ | 9 | | 10 | | 12 | | 15 | | 20 | | 25 | | ns | |
| Chip Enable to end of write | $^tCW$ | 7 | | 8 | | 10 | | 12 | | 15 | | 20 | | ns | |
| Address valid to end of write | $^tAW$ | 7 | | 8 | | 10 | | 12 | | 15 | | 20 | | ns | |
| Address setup time | $^tAS$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Address hold from end of write | $^tAH$ | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| WRITE pulse width | $^tWP1$ | 6 | | 7 | | 8 | | 10 | | 12 | | 15 | | ns | |
| WRITE pulse width | $^tWP2$ | 8 | | 9 | | 10 | | 14 | | 18 | | 20 | | ns | |
| Data setup time | $^tDS$ | 5 | | 6 | | 7 | | 8 | | 9 | | 10 | | ns | |
| Data hold time | $^tDH$ | 1 | | 1 | | 1 | | 1 | | 1 | | 1 | | ns | |
| Write disable to output in Low-Z | $^tLZWE$ | 2 | | 2 | | 2 | | 2 | | 2 | | 2 | | ns | 7 |
| Write Enable to output in High-Z | $^tHZWE$ | | 4 | | 5 | | 5 | | 6 | | 8 | | 8 | ns | 6, 7 |

## INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C6408 SRAMs.
(-40°C ≤ $T_A$ ≤ 85°C)

| | | | MAX | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **DESCRIPTION** | **CONDITIONS** | **SYMBOL** | **-10** | **-12** | **-15** | **-20** | **-25** | **UNITS** | **NOTES** |
| Power Supply Current: Operating | $\overline{CE}$ ≤ $V_{IL}$; $V_{CC}$ = MAX f = MAX = 1/ $^tRC$ outputs open | $I_{CC}$ | 195 | 185 | 175 | 150 | 140 | mA | 3, 13 |
| Power Supply Current: Standby | $\overline{CE}$ ≥ $V_{IH}$; $V_{CC}$ = MAX f = MAX = 1/ $^tRC$ outputs open | $I_{SB1}$ | 60 | 50 | 45 | 40 | 40 | mA | 13 |
| | $\overline{CE}$ ≥ $V_{CC}$ -0.2V; $V_{CC}$ = MAX $V_{IN}$ ≤ $V_{SS}$ +0.2V or $V_{IN}$ ≥ $V_{CC}$ -0.2V; f = 0 | $I_{SB2}$ | 5 | 5 | 5 | 5 | 5 | mA | 13 |

## DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

| **DESCRIPTION** | **CONDITIONS** | | **SYMBOL** | **TYP** | **MAX** | **UNITS** | **NOTES** |
|---|---|---|---|---|---|---|---|
| Data Retention Current | $\overline{CE}$ ≥ ($V_{CC}$ -0.2V) $V_{IN}$ ≥ ($V_{CC}$ -0.2V) or ≤ 0.2V | $V_{CC}$ = 2V | $I_{CCDR}$ | 130 | 300 | µA | 14 |
| | | $V_{CC}$ = 3V | $I_{CCDR}$ | 210 | 550 | µA | 14 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ $T_A$ ≤ 85°C)

| **DESCRIPTION** | | -12 | | -15 | | -20 | | -25 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| **READ Cycle** | | | | | | | | | | | |
| Output hold from address change | $^tOH$ | 2 | | 2 | | 2 | | 2 | | ns | |
| Chip Enable to output in Low-Z | $^tLZCE$ | 1 | | 1 | | 1 | | 1 | | ns | 7 |
| **WRITE Cycle** | | | | | | | | | | | |
| Write disable to output in Low-Z | $^tLZWE$ | 1 | | 1 | | 1 | | 1 | | ns | 7 |

## AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C6408 SRAMs. (-40°C ≤ $T_A$ ≤ 125°C - AT) (-55°C ≤ $T_A$ ≤ 125°C - XT)

| | | | MAX | | | | | |
|---|---|---|---|---|---|---|---|---|
| **DESCRIPTION** | **CONDITIONS** | **SYMBOL** | **-12** | **-15** | **-20** | **-25** | **UNITS** | **NOTES** |
| Power Supply Current: Operating | $\overline{CE}$ ≤ $V_{IL}$; $V_{CC}$ = MAX<br>f = MAX = 1/ $^tRC$<br>outputs open | $I_{CC}$ | 185 | 175 | 150 | 140 | mA | 3, 13 |
| Power Supply Current: Standby | $\overline{CE}$ ≥ $V_{IH}$; $V_{CC}$ = MAX<br>f = MAX = 1/ $^tRC$<br>outputs open | $I_{SB1}$ | 50 | 45 | 40 | 40 | mA | 13 |
| | $\overline{CE}$ ≥ $V_{CC}$ -0.2V; $V_{CC}$ = MAX<br>$V_{IN}$ ≤ $V_{SS}$ +0.2V or<br>$V_{IN}$ ≥ $V_{CC}$ -0.2V; f = 0 | $I_{SB2}$ | 5 | 5 | 5 | 5 | mA | 13 |

## DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

| **DESCRIPTION** | **CONDITIONS** | | **SYMBOL** | **TYP** | **MAX** | **UNITS** | **NOTES** |
|---|---|---|---|---|---|---|---|
| Data Retention Current | $\overline{CE}$ ≥ ($V_{CC}$ -0.2V)<br>$V_{IN}$ ≥ ($V_{CC}$ -0.2V)<br>or ≤ 0.2V | $V_{CC}$ = 2V | $I_{CCDR}$ | 130 | 300 | µA | 14 |
| | | $V_{CC}$ = 3V | $I_{CCDR}$ | 210 | 550 | µA | 14 |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 14) (-40°C ≤ $T_A$ ≤ 125°C; -55°C ≤ $T_A$ ≤ 125°C; $V_{CC}$ = 5V ±10%)

| **DESCRIPTION** | | -12 | | -15 | | -20 | | -25 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **SYM** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| **READ Cycle** | | | | | | | | | | | |
| Output hold from address change | $^tOH$ | 2 | | 2 | | 2 | | 2 | | ns | |
| Chip Enable to output in Low-Z | $^tLZCE$ | 1 | | 1 | | 1 | | 1 | | ns | 7 |
| **WRITE Cycle** | | | | | | | | | | | |
| Write disable to output in Low-Z | $^tLZWE$ | 1 | | 1 | | 1 | | 1 | | ns | 7 |

## AC TEST CONDITIONS

| | |
|---|---|
| Input pulse levels | Vss to 3.0V |
| Input rise and fall times | 3ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figures 1 and 2 |

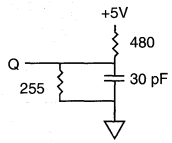



Fig. 1 OUTPUT LOAD EQUIVALENT

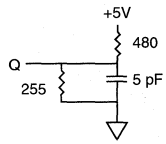



Fig. 2 OUTPUT LOAD EQUIVALENT

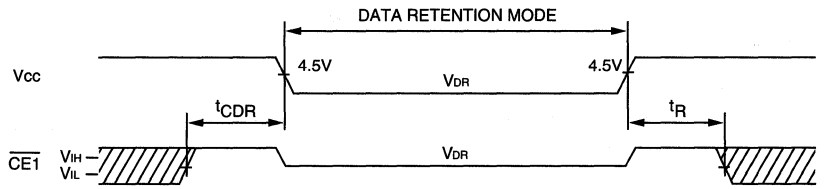
## NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}$RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. $^{t}$HZCE, $^{t}$HZWE and $^{t}$HZOE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}$HZCE is less than $^{t}$LZCE and $^{t}$HZWE is less than $^{t}$LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. $^{t}$RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The wave is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Typical values are measured at 5V, 25°C and 15ns cycle time.
15. Typical currents are measured at 25°C.
16. Output enable ($\overline{OE}$) is inactive (HIGH).
17. Output enable ($\overline{OE}$) is active (LOW).

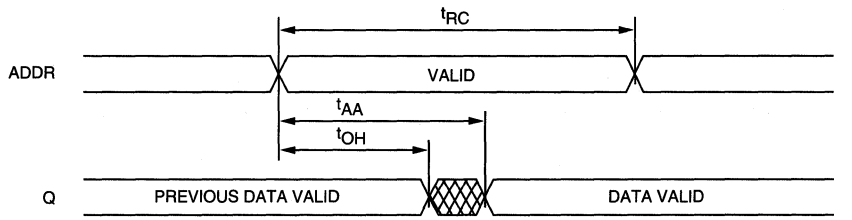
## DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

| DESCRIPTION | CONDITIONS | | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| Vcc for Retention Data | | | VDR | 2 | | | V | |
| Data Retention Current | $\overline{CE}$ ≥ (Vcc -0.2V) VIN ≥ (Vcc -0.2V) or ≤ 0.2V | Vcc = 2V | ICCDR | | 130 | 300 | µA | 15 |
| | | Vcc = 3V | ICCDR | | 210 | 400 | µA | 15 |
| Chip Deselect to Data Retention Time | | | $^{t}$CDR | 0 | | | ns | 4 |
| Operation Recovery Time | | | $^{t}$R | $^{t}$RC | | | ns | 4, 11 |

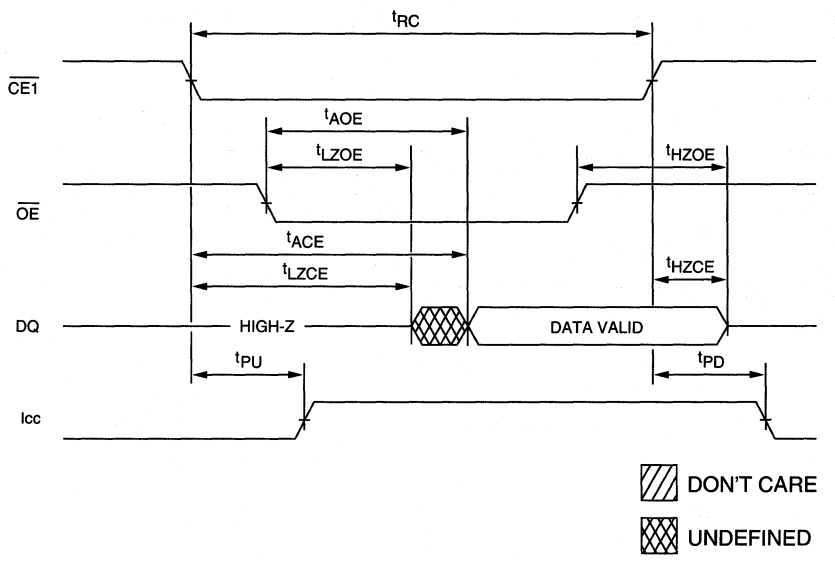
## LOW Vcc DATA RETENTION WAVEFORM [12]



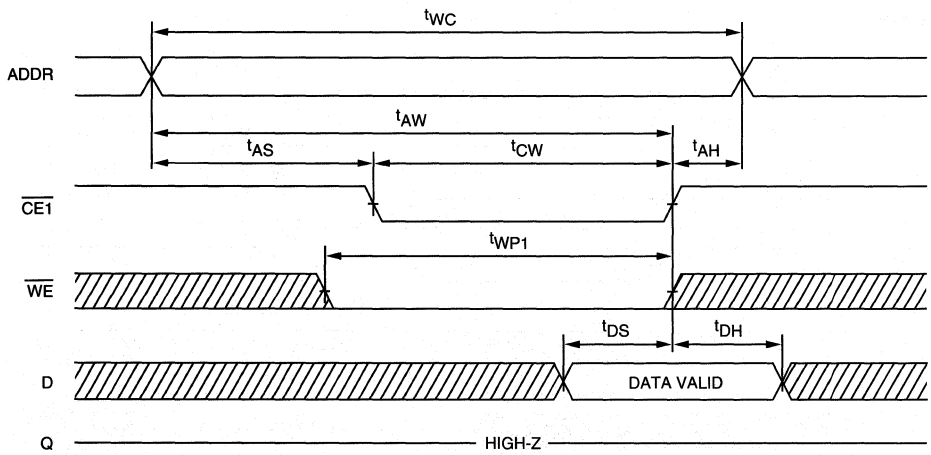

## READ CYCLE NO. 1 [8, 9]



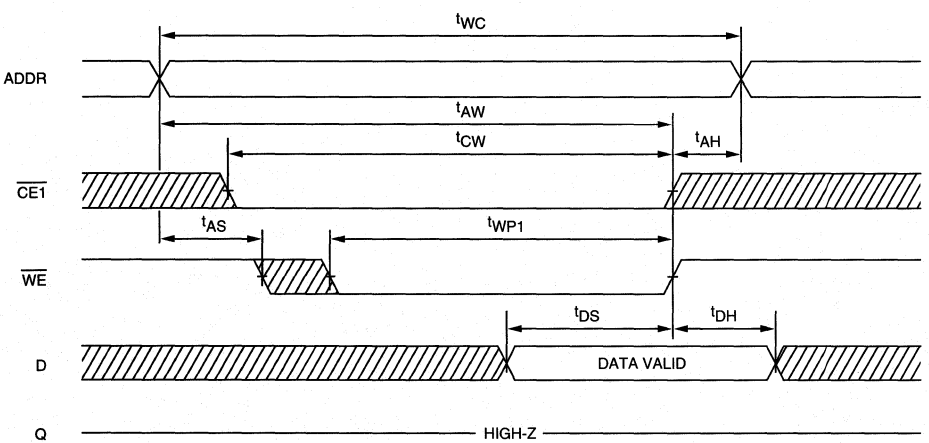

## READ CYCLE NO. 2 [7, 8, 10, 12]

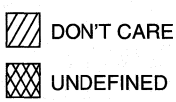


## WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)




## WRITE CYCLE NO. 2 [12, 13, 16]
(Write Enable Controlled)



## WRITE CYCLE NO. 3 [7, 12, 13, 17]
(Write Enable Controlled)