

SRAM

1 MEG x 4 SRAM

WITH OUTPUT ENABLE

5 VOLT SRAM

FEATURES

- High speed: 12, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Multiple center power and ground pins for improved noise immunity
- Single +5V $\pm 10\%$ power supply
- Easy memory expansion with \overline{CE} and \overline{OE} options
- All inputs and outputs are TTL-compatible
- Fast \overline{OE} access time: 6, 8, 10, 12 and 15ns

OPTIONS

- Timing

| | |
|-------------|-----|
| 12ns access | -12 |
| 15ns access | -15 |
| 20ns access | -20 |
| 25ns access | -25 |
| 35ns access | -35 |
- Packages

| | |
|------------------------|----|
| Plastic SOJ (400 mil) | DJ |
| Plastic TSOP (400 mil) | TG |
- 2V data retention

| | |
|--|---|
| | L |
|--|---|
- Low power

| | |
|--|---|
| | P |
|--|---|
- Temperature

| | |
|------------------------------|------|
| Commercial (0°C to +70°C) | None |
| Industrial (-40°C to +85°C) | IT |
| Automotive (-40°C to +125°C) | AT |
| Extended (-55°C to +125°C) | XT |

MARKING

- Part Number Example: MT5C1M4B2DJ-35 L

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

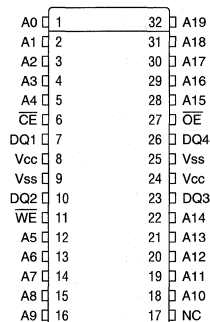
GENERAL DESCRIPTION

The MT5C1M4B2 is organized as a 1,048,576 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron 4 Meg SRAMs are fabricated using double-layer metal, triple-layer polysilicon technology.

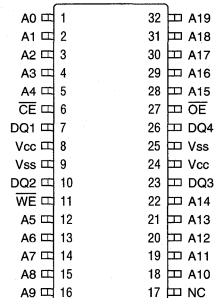
This device offers multiple center power and ground pins for improved performance. For flexibility in high-speed memory applications, Micron offers chip enable (\overline{CE}) and output enable (\overline{OE}) with this configuration. These enhancements can place the outputs in High-Z for additional flexibility in system design.

PIN ASSIGNMENT (Top View)

32-Pin SOJ (SD-5)



32-Pin TSOP (SE-1)

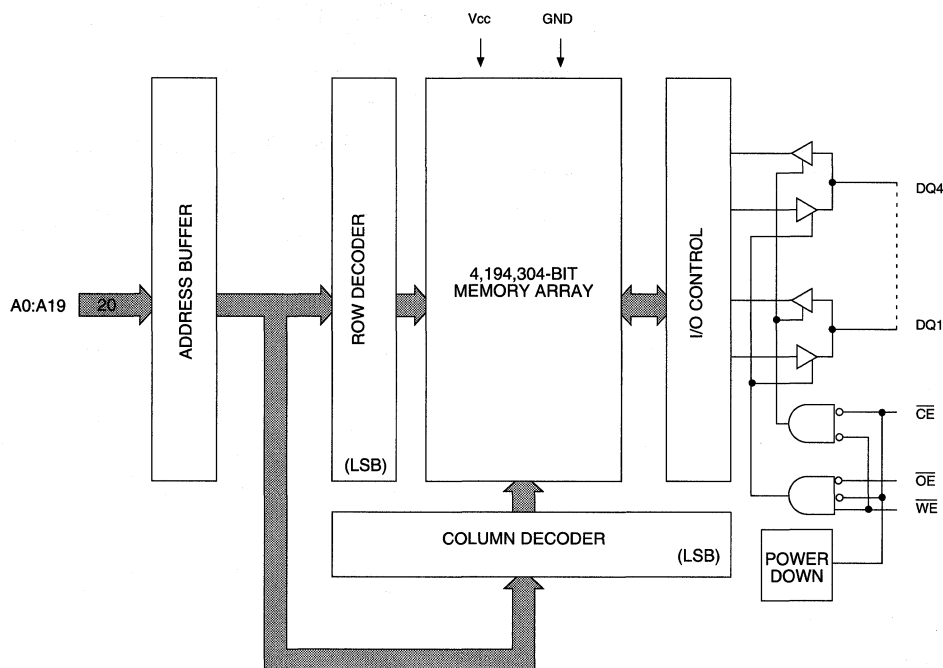


Writing to this device is accomplished when write enable (\overline{WE}) and \overline{CE} inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH while output enable (\overline{OE}) and \overline{CE} go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a 90 percent reduction in TTL standby current (I_{SB1}) through the use of gated inputs on the \overline{WE} , \overline{OE} and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

| MODE | \overline{OE} | \overline{CE} | \overline{WE} | DQ | POWER |
|--------------|-----------------|-----------------|-----------------|--------|---------|
| STANDBY | X | H | X | HIGH-Z | STANDBY |
| READ | L | L | H | Q | ACTIVE |
| NOT SELECTED | H | L | H | HIGH-Z | ACTIVE |
| WRITE | X | L | L | D | ACTIVE |

THERMAL IMPEDENCE (EST)¹⁶

| PACKAGE | NUMBER OF PINS | θ_{JC}^* (°C/W) | θ_{JA}^* (°C/W) |
|---------|----------------|---------------------------|---------------------------|
| SOJ | 32 | 15 | 60 |
| TSOP | 32 | 5 | 70 |

*The thermal impedance numbers assume the device is socketted on a PC board and air flow is zero.

ABSOLUTE MAXIMUM RATINGS*

| | |
|---|---------------------------|
| Voltage on V _{CC} Supply Relative to V _{SS} | -1V to +7V |
| Storage Temperature (plastic) | -55°C to +150°C |
| Short Circuit Output Current | 50mA |
| Voltage on any pin relative to V _{SS} | -1V to V _{CC} +1 |
| Junction Temperature** | +150°C |

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this data sheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|------------------------------|---|-----------------|------|--------------------|-------|-------|
| Input High (Logic 1) Voltage | | V _{IH} | 2.2 | V _{CC} +1 | V | 1 |
| Input Low (Logic 0) Voltage | | V _{IL} | -0.5 | 0.8 | V | 1, 2 |
| Input Leakage Current | 0V ≤ V _{IN} ≤ V _{CC} | I _{LI} | -2 | 2 | μA | |
| Output Leakage Current | Output(s) disabled 0V ≤ V _{OUT} ≤ V _{CC} | I _{LO} | -2 | 2 | μA | |
| Output High Voltage | I _{OH} = -4.0mA | V _{OH} | 2.4 | | V | 1 |
| Output Low Voltage | I _{OL} = 8.0mA | V _{OL} | | 0.4 | V | 1 |
| Supply Voltage | | V _{CC} | 4.5 | 5.5 | V | 1 |

| DESCRIPTION | CONDITIONS | SYMBOL | MAX | | | | | UNITS | NOTES |
|---------------------------------|--|------------------|-----|-----|-----|-----|-----|-------|-------|
| | | | -12 | -15 | -20 | -25 | -35 | | |
| Power Supply Current: Operating | $\overline{CE} \leq V_{IL}$; V _{CC} = MAX f = MAX = 1/'RC outputs open | I _{CC} | 200 | 180 | 175 | 170 | 160 | mA | 3 |
| Power Supply Current: Standby | $\overline{CE} \geq V_{IH}$; V _{CC} = MAX f = MAX = 1/'RC outputs open | I _{SB1} | 35 | 30 | 25 | 25 | 20 | mA | |
| | P version only | I _{SB1} | 2 | 2 | 2 | 2 | 2 | mA | |
| | $\overline{CE} \geq V_{CC} - 0.2V$; V _{CC} = MAX V _{IN} ≤ V _{SS} +0.2V or V _{IN} ≥ V _{CC} -0.2V; f = 0 | I _{SB2} | 2 | 2 | 2 | 2 | 2 | mA | |
| | P version only | I _{SB2} | 2 | 2 | 2 | 2 | 2 | mA | |

CAPACITANCE

| DESCRIPTION | CONDITIONS | SYMBOL | MAX | UNITS | NOTES |
|--------------------|--|----------------|-----|-------|-------|
| Input Capacitance | T _A = 25°C; f = 1 MHz V _{CC} = 5V | C _I | 5 | pF | 4 |
| Output Capacitance | | C _O | 7 | pF | 4 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Notes 5, 13) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 5\text{V} \pm 10\%$)

| DESCRIPTION | | -12 | | -15 | | -20 | | -25 | | -35 | | | |
|------------------------------------|-------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-------|-------|
| | SYM | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| READ Cycle | | | | | | | | | | | | | |
| READ cycle time | t _{RC} | 12 | | 15 | | 20 | | 25 | | 35 | | ns | |
| Address access time | t _{AA} | | 12 | | 15 | | 20 | | 25 | | 35 | ns | |
| Chip Enable access time | t _{ACE} | | 12 | | 15 | | 20 | | 25 | | 35 | ns | |
| Output hold from address change | t _{OH} | 3 | | 3 | | 3 | | 3 | | 3 | | ns | |
| Chip Enable to output in Low-Z | t _{LZCE} | 3 | | 3 | | 5 | | 5 | | 5 | | ns | 7 |
| Chip disable to output in High-Z | t _{HZCE} | | 6 | | 7 | | 8 | | 10 | | 15 | ns | 6, 7 |
| Chip Enable to power-up time | t _{PU} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Chip disable to power-down time | t _{PD} | | 12 | | 15 | | 20 | | 25 | | 35 | ns | |
| Output Enable access time | t _{AOE} | | 6 | | 8 | | 10 | | 12 | | 15 | ns | |
| Output Enable to output in Low-Z | t _{LZOE} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Output disable to output in High-Z | t _{HZOE} | | 5 | | 6 | | 7 | | 10 | | 12 | ns | 6 |
| WRITE Cycle | | | | | | | | | | | | | |
| WRITE cycle time | t _{WC} | 12 | | 15 | | 20 | | 25 | | 35 | | ns | |
| Chip Enable to end of write | t _{CW} | 8 | | 10 | | 12 | | 15 | | 20 | | ns | |
| Address valid to end of write | t _{AW} | 8 | | 10 | | 12 | | 15 | | 20 | | ns | |
| Address setup time | t _{AS} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Address hold from end of write | t _{AH} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| WRITE pulse width | t _{WP1} | 8 | | 9 | | 10 | | 15 | | 20 | | ns | |
| WRITE pulse width | t _{WP2} | 9 | | 11 | | 12 | | 17 | | 22 | | ns | |
| Data setup time | t _{DS} | 6 | | 7 | | 8 | | 10 | | 15 | | ns | |
| Data hold time | t _{DH} | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Write disable to output in Low-Z | t _{LZWE} | 3 | | 3 | | 4 | | 5 | | 5 | | ns | 7 |
| Write Enable to output in High-Z | t _{HZWE} | | 5 | | 6 | | 8 | | 10 | | 15 | ns | 6, 7 |

AC TEST CONDITIONS

| | |
|-------------------------------------|-------------------------|
| Input pulse levels | V _{SS} to 3.0V |
| Input rise and fall times | 3ns |
| Input timing reference levels | 1.5V |
| Output reference levels | 1.5V |
| Output load | See Figures 1 and 2 |

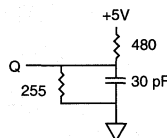


Fig. 1 OUTPUT LOAD EQUIVALENT

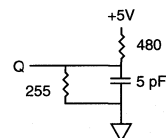


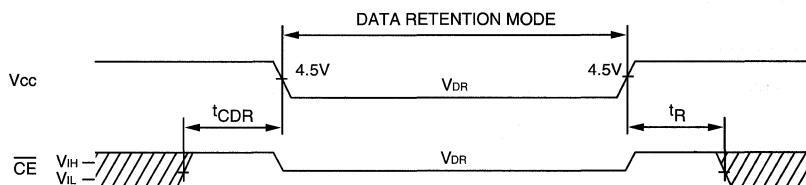
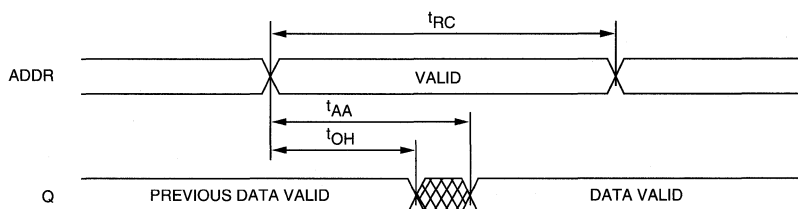
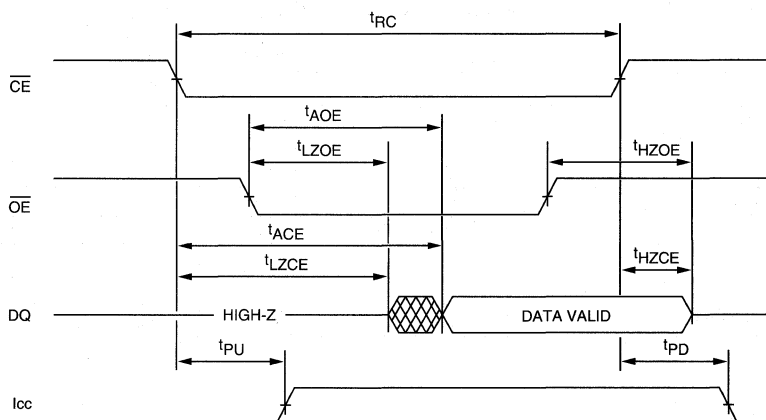
Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to V_{SS} (GND).
2. -3V for pulse width < t_{RC}/2.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE}.
8. \overline{WE} is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. t_{RC} = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Contact Micron for IT/AT/XT timing and current specifications; they may differ from the commercial temperature range specifications shown in this data sheet.
14. Output enable (\overline{OE}) is inactive (HIGH).
15. Output enable (\overline{OE}) is active (LOW).
16. Micron does not warrant functionality nor reliability of any product in which the junction temperature exceeds 150°C. Care should be taken to limit power to acceptable levels.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

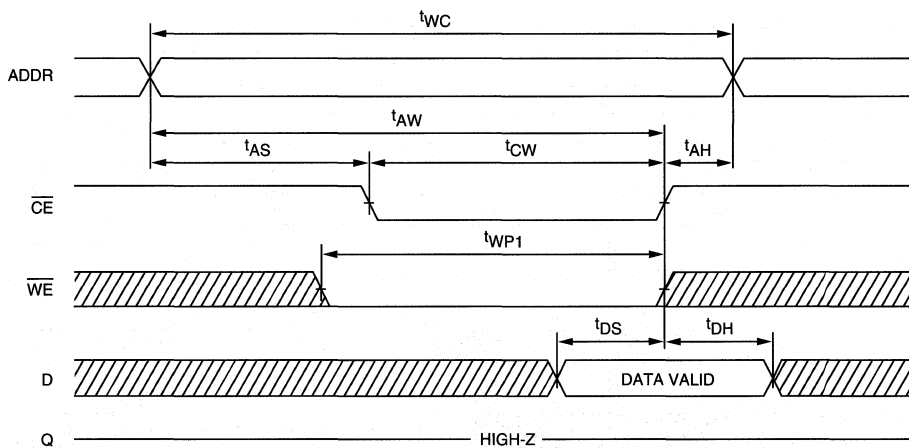
| DESCRIPTION | CONDITIONS | | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|----------------------|-------------------|-----------------|-----|-------|-------|
| V _{CC} for Retention Data | | | V _{DR} | 2 | | V | |
| Data Retention Current L version | $\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$ | V _{CC} = 2V | I _{CCDR} | | 1 | mA | |
| | | V _{CC} = 3V | I _{CCDR} | | 1.5 | mA | |
| Data Retention Current LP version | $\overline{CE} \geq (V_{CC} - 0.2V)$ | V _{CC} = 2V | I _{CCDR} | | 1 | mA | |
| | | V _{CC} = 3V | I _{CCDR} | | 1.5 | mA | |
| Chip Deselect to Data Retention Time | | | t _{CDR} | 0 | | ns | 4 |
| Operation Recovery Time | | | t _R | t _{RC} | | ns | 4, 11 |

LOW V_{CC} DATA RETENTION WAVEFORM

READ CYCLE NO. 1 8, 9

READ CYCLE NO. 2 7, 8, 10


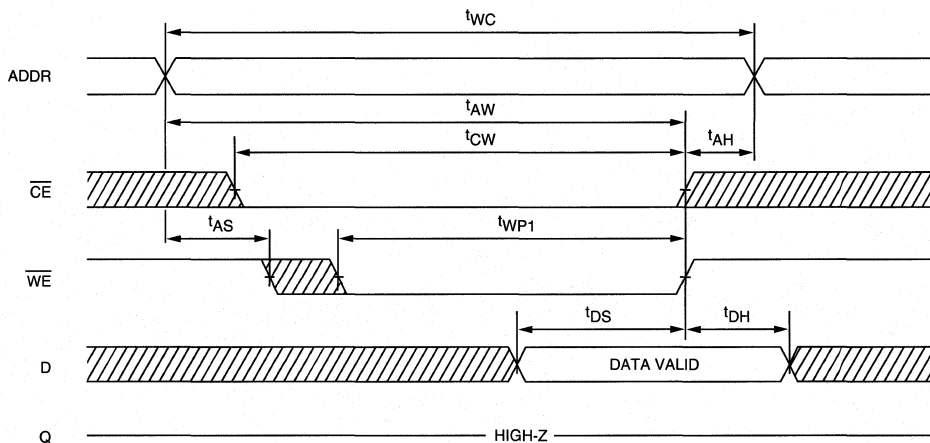
DON'T CARE

UNDEFINED

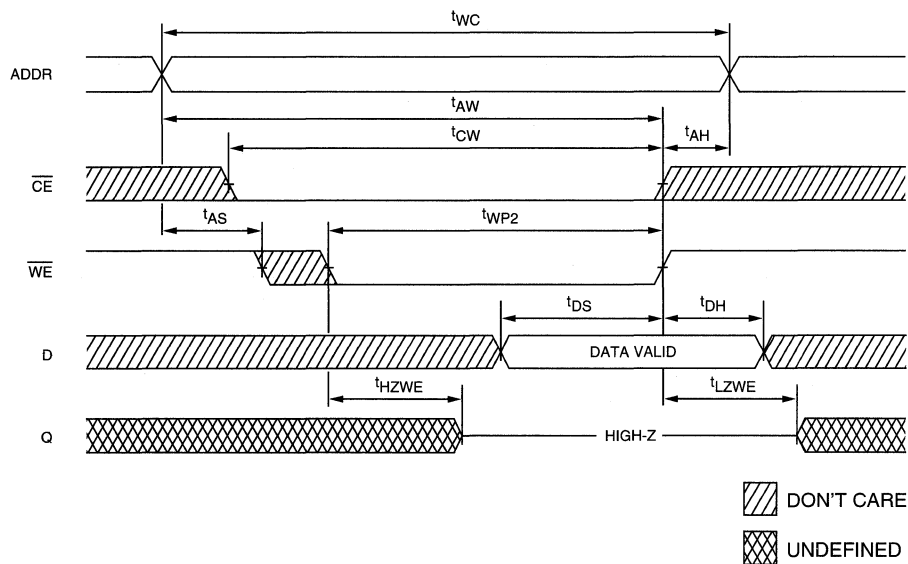
WRITE CYCLE NO. 1 ¹²
(Chip Enable Controlled)



WRITE CYCLE NO. 2 ^{12, 14}
(Write Enable Controlled)



DON'T CARE
 UNDEFINED

WRITE CYCLE NO. 3 7, 12, 15
 (Write Enable Controlled)


APPLICATION INFORMATION

THERMAL CONSIDERATIONS

This section describes how to determine the junction temperature during operating conditions. It is essential that the maximum junction temperature of the 4 Meg SRAM is not exceeded. If this temperature is exceeded it is necessary to add external cooling such as forced airflow or change the operating conditions. The maximum junction temperature for Micron SRAMs is 150°C. The limiting temperature factor is not the SRAM but the mold compound which prevents reliable operating temperatures significantly about 150°C. However, it is advisable to run the part as cool as possible since reliability (FIT rates) are exponentially dependent upon junction temperature.

The calculation of the actual junction temperature begins with the power calculation and then the junction temperature calculation. Equations 1 and 2 below show how T_j is determined using the ambient temperature, thermal resistance and operating power. If an airflow is introduced into a system then Equation 2 should be used with an airflow thermal multiplier. Specific thermal resistances are given in Micron technical note "SRAM Thermal Design Considerations" and in individual data sheets.

$$T_j = T_A + P * \theta_{JA} \quad (1)$$

$$T_j = T_A + P * \theta_{JA} * \theta_M \quad (2)$$

- T_j = Junction temperature of the active portion of the silicon die (°C)
 T_A = Ambient air temperature (°C) at which the device is operated
 P = Average power dissipation of the device (W)
 θ_{JA} = Junction to ambient thermal resistance (°C/W)
 θ_M = Airflow multiplier. This value changes for different values of airflow over the part (fpm).

To solve the above equations the average operating power must be calculated. Total power has three separate components (P_1 , P_2 and P_3). P_1 is the operating power dissipated by the chip, P_2 is the AC output power due to the capacitive load and P_3 is the DC output power due to TTL DC load current (P_3 is usually negligible). For this example we have chosen P_2 such that outputs are switching from a logic LOW

state to a logic HIGH state which gives the worst case output AC current. A complete description of these equations and their derivation is given in Micron technical note "Design Tips: 32K x 36 SRAM."

$$P_1 = V_{CC} I_{CC}$$

$$P_2 = \frac{C_L}{T} (V_{CC} [V_{OH} - V_{OL}] - 0.5 [V_{OH}^2 - V_{OL}^2]) N_S$$

$$P_3 = (V_{CC} - V_{OH}) I_O N_H + V_{OL} I_I N_L$$

V_{CC} = Supply voltage

I_{CC} = Supply current

C_L = Capacitive output loading

T = Clock period

V_{OH} = Output high voltage

V_{OL} = Output low voltage

I_O = Output current on DQ lines which are high

I_I = Input current on DQ lines which are low

N_H = Number of DQ lines which are high


N_L = Number of DQ lines which are low.

Table 1
EFFECTS OF AIRFLOW ON 4 MEG SRAM
SOJ PACKAGES

| Package | Air Flow | θ_M Multiplier |
|---------|----------|-----------------------|
| PSOJ | 200 fpm | 0.7 - 0.75 |
| PSOJ | 500 fpm | 0.55 - 0.65 |

ADDITIONAL INFORMATION

For more information on thermal considerations see Micron's technical notes, "SRAM Thermal Design Considerations" and "Design Tips: 32K x 36 SRAM." These notes explain how to calculate thermal resistance and how to improve thermal performance in much greater detail. Also available is Micron's *Quality and Reliability Handbook*, which gives an explanation of how thermal impedances are calculated.


5 VOLT SRAM