MICRON SEMICONDUCTOR, INC.

MT58LC32K36M1
32K x 36 SYNCHRONOUS SRAM

SYNCHRONOUS SRAM

32K x 36 SRAM

+3.3V SUPPLY WITH CLOCKED, REGISTERED INPUTS AND LINEAR BURST COUNTER

NEW ■ 3.3 VOLT SYNCHRONOUS SRAM

FEATURES

- Fast access times: 9, 10, 12 and 17ns
- Fast $\overline{OE}$: 5, 6 and 7ns
- Single +3.3V ±5% power supply
- 5V-tolerant I/O
- Common data inputs and data outputs
- Individual BYTE WRITE control
- Three Chip Enables for simple depth expansion
- Clock controlled, registered, address, data and control
- Internally self-timed WRITE cycle
- Burst control pins (linear burst sequence)
- 100-lead TQFP package for high density, high speed
- Low capacitive bus loading
- High 30pF output drive capability at rated access time
- Parity Disable function for 32-bit operation

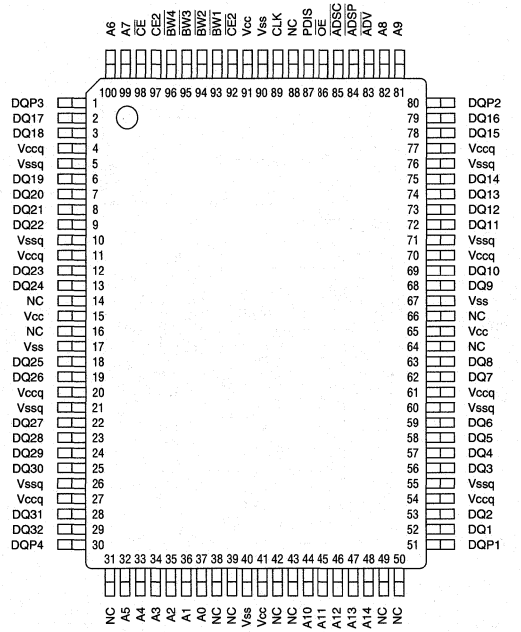
OPTIONS MARKING

- Timing
  - 9ns access/15ns cycle - 9
  - 10ns access/15ns cycle -10
  - 12ns access/20ns cycle -12
  - 17ns access/25ns cycle -17
- Packages
  - 100-pin TQFP LG
- Part Number Example: MT58LC32K36M1LG-12

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

100-Pin TQFP
(SC-1)



GENERAL DESCRIPTION

The Micron Synchronous SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT58LC32K36M1 SRAM integrates a 32K x 36 SRAM core with advanced synchronous peripheral circuitry and a 2-bit burst counter. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input (CLK). The synchronous inputs include all addresses, all data inputs, active LOW chip enable ($\overline{CE}$), two additional chip enables for easy depth expansion ($\overline{CE2}$, CE2), burst control inputs ($\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$) and the byte write enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$).

Asynchronous inputs include the output enable ($\overline{OE}$) and the clock (CLK). The data-out (Q), enabled by $\overline{OE}$, is also asynchronous. WRITE cycles can be from one to four bytes wide as controlled by the byte write enables.

Burst operation can be initiated with either address status processor ($\overline{ADSP}$) or address status controller ($\overline{ADSC}$) input pins. Subsequent burst addresses can be internally generated as controlled by the burst advance pin ($\overline{ADV}$).

Address and write control are registered on-chip to simplify WRITE cycles. This allows self-timed WRITE cycles. Individual byte enables allow individual bytes to be written. $\overline{BW1}$ controls DQ1-DQ8 and DQP1, $\overline{BW2}$ controls DQ9-DQ16 and DQP2, $\overline{BW3}$ controls DQ17-DQ24 and

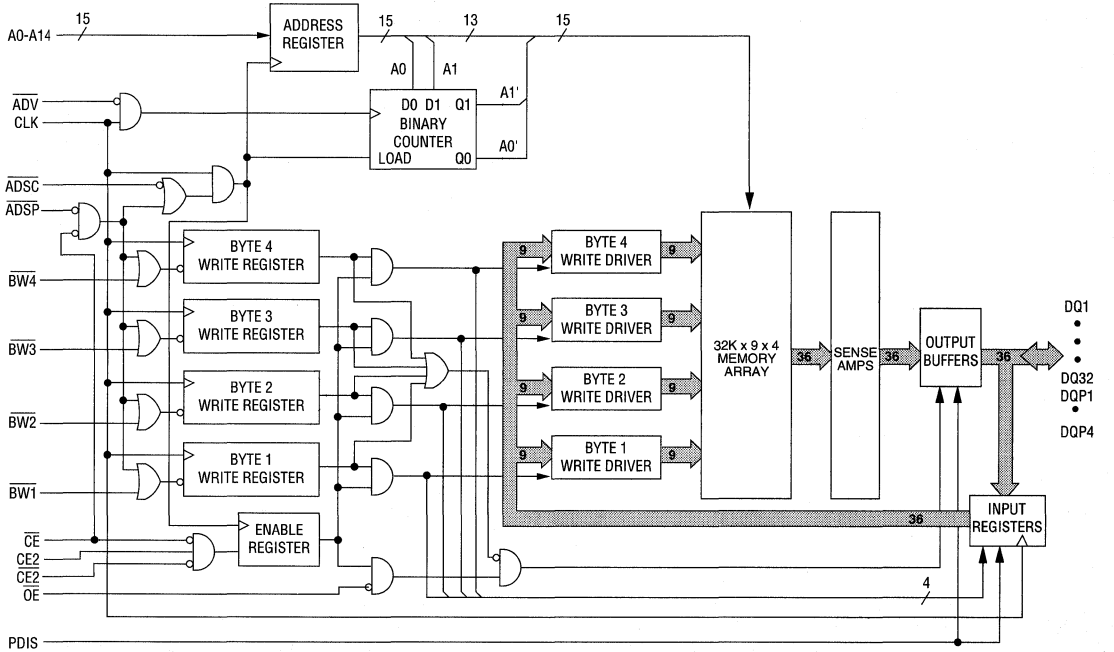
NEW ■ 3.3 VOLT SYNCHRONOUS SRAM

GENERAL DESCRIPTION (continued)

DQP3, and $\overline{BW4}$ controls DQ25-DQ32 and DQP4.

The MT58LC32K36M1 operates from a +3.3V power supply and all inputs and outputs are TTL-compatible and 5V tolerant. The device is ideally suited for PowerPC™, 680X0 and any other system which benefits from a very wide data bus and linear-burst synchronous operation. The device can also be used in 32-, 64- and 72-bit wide applications.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN DESCRIPTIONS

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 44, 45, 46, 47, 48	A0-A14	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
93, 94, 95, 96	$\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$	Input	Synchronous Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CLK. A byte write enable is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{BW1}$ controls DQ1-DQ8 and DQP1. $\overline{BW2}$ controls DQ9-DQ16 and DQP2. $\overline{BW3}$ controls DQ17-DQ24 and DQP3. $\overline{BW4}$ controls DQ25-DQ32 and DQP4. Data I/O are tristated if any of these four inputs are LOW.
89	CLK	Input	Clock: This signal registers the address, data, chip enables, byte write enables and burst control inputs on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
98	$\overline{CE}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device and conditions internal use of $\overline{ADSP}$. This input is sampled only when a new external address is loaded.
92	$\overline{CE2}$	Input	Synchronous Chip Enable: This active LOW input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
97	CE2	Input	Synchronous Chip Enable: This active HIGH input is used to enable the device. This input is sampled only when a new external address is loaded. This input can be used for memory depth expansion.
86	$\overline{OE}$	Input	Output Enable: This active LOW asynchronous input enables the data I/O output drivers.
83	$\overline{ADV}$	Input	Synchronous Address Advance: This active LOW input is used to advance the internal burst counter, controlling burst access after the external address is loaded. A HIGH on this pin effectively causes wait states to be generated (no address advance). This pin must be HIGH at the rising edge of the first clock after an $\overline{ADSP}$ cycle is initiated if a WRITE cycle is desired (to ensure use of correct address).
84	$\overline{ADSP}$	Input	Synchronous Address Status Processor: This active LOW input interrupts any ongoing burst, causing a new external address to be registered. A READ is performed using the new address, independent of the byte write enables and $\overline{ADSC}$ but dependent upon CE2 and $\overline{CE2}$. $\overline{ADSP}$ is ignored if $\overline{CE}$ is HIGH. Power-down state is entered if CE2 is LOW or $\overline{CE2}$ is HIGH.
85	$\overline{ADSC}$	Input	Synchronous Address Status Controller: This active LOW input interrupts any ongoing burst and causes a new external address to be registered. A READ or WRITE is performed using the new address if all chip enables are active. Power-down state is entered if one or more chip enables are inactive.

PIN DESCRIPTIONS (continued)

TQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
14, 16, 31, 38, 39, 42, 43, 49, 50, 64, 66, 88	NC	-	No Connect: These signals are not internally connected.
52, 53, 56, 57, 58, 59, 62, 63, 68, 69, 72, 73, 74, 75, 78, 79, 2, 3, 6, 7, 8, 9, 12, 13, 18, 19, 22, 23, 24, 25, 28, 29	DQ1-DQ32	Input/ Output	SRAM Data I/O: Byte 1 is DQ1-DQ8; Byte 2 is DQ9-DQ16; Byte 3 is DQ17-DQ24; Byte 4 is DQ25-DQ32. Input data must meet setup and hold times around the rising edge of CLK.
51, 80, 1, 30	DQP1-DQP4	Input/ Output	Parity Data I/O: Byte 1 Parity is DQP1; Byte 2 Parity is DQP2; Byte 3 Parity is DQP3; Byte 4 Parity is DQP4.
87	PDIS	Input	Parity Disable: When HIGH, this input disables DQP1 through DQP4 for 32-bit data bus width. A LOW on PDIS enables control of DQP1 through DQP4 in the same manner as DQ1-DQ32 are controlled.
15, 41, 65, 91	Vcc	Supply	Power Supply: +3.3V ±5%
17, 40, 67, 90	Vss	Supply	Ground: GND
4, 11, 20, 27, 54, 61, 70, 77	VccQ	Supply	Isolated Output Buffer Supply: +3.3V ±5%
5, 10, 21, 26, 55, 60, 71, 76	VssQ	Supply	Isolated Output Buffer Ground: GND

BURST ADDRESS TABLE

First Address	Second Address	Third Address	Fourth Address
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

TRUTH TABLE

OPERATION	ADDRESS USED	$\overline{CE}$	$\overline{CE2}$	CE2	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	$\overline{OE}$	CLK	DQ
Deselected Cycle, Power-down	None	H	X	X	X	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	L	X	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	X	L	H	L	X	X	X	L-H	High-Z
Deselected Cycle, Power-down	None	L	H	X	H	L	X	X	X	L-H	High-Z
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	L	X	X	X	H	L-H	High-Z
WRITE Cycle, Begin Burst	External	L	L	H	H	L	X	L	X	L-H	D
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	L	L-H	Q
READ Cycle, Begin Burst	External	L	L	H	H	L	X	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	X	X	X	H	H	L	H	H	L-H	High-Z
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	L	L-H	Q
READ Cycle, Continue Burst	Next	H	X	X	X	H	L	H	H	L-H	High-Z
WRITE Cycle, Continue Burst	Next	X	X	X	H	H	L	L	X	L-H	D
WRITE Cycle, Continue Burst	Next	H	X	X	X	H	L	L	X	L-H	D
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	X	X	X	H	H	H	H	H	L-H	High-Z
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	L	L-H	Q
READ Cycle, Suspend Burst	Current	H	X	X	X	H	H	H	H	L-H	High-Z
WRITE Cycle, Suspend Burst	Current	X	X	X	H	H	H	L	X	L-H	D
WRITE Cycle, Suspend Burst	Current	H	X	X	X	H	H	L	X	L-H	D

NOTE:
1. X means "don't care." H means logic HIGH. L means logic LOW. $\overline{WRITE}$=L means any one or more byte write enable signals ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$ or $\overline{BW4}$) are LOW. $\overline{WRITE}$=H means all byte write enable signals are HIGH.
2. $\overline{BW1}$ enables writes to Byte 1 (DQ1-DQ8, DQP1). $\overline{BW2}$ enables writes to Byte 2 (DQ9-DQ16, DQP2). $\overline{BW3}$ enables writes to Byte 3 (DQ17-DQ24, DQP3). $\overline{BW4}$ enables writes to Byte 4 (DQ25-DQ32, DQP4).
3. All inputs except $\overline{OE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. Wait states are inserted by suspending burst.
5. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required setup time and held HIGH throughout the input data hold time.
6. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
7. PDIS disables the DQP lines when HIGH and enables the DQP lines when LOW.
8. $\overline{ADSP}$ LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals LOW for the subsequent L-H edge of CLK. Refer to WRITE timing diagram for clarification.

NEW 3.3 VOLT SYNCHRONOUS SRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to Vss .....-0.5V to +4.6V
V_{IN} .....-0.5V to +6V
Storage Temperature (plastic) .....-55°C to +150°C
Junction Temperature .....+150°C
Power Dissipation 1.6W
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; T_C ≤ 110°C; V_{CC} = 3.3V ±5% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	5.5	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	3.1	3.5	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYPICAL	-9	-10	-12	-17	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} OR ≥ V_{IH}; cycle time ≥ ^tKC min; V_{CC} = MAX; outputs open	I_{CC}	200	275	275	250	225	mA	3, 12, 13
Power Supply Current: Idle	Device selected; $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$ ≥ V_{IH}; all inputs ≤ V_{IL} OR ≥ V_{IH}; V_{CC} = MAX; cycle time ≥ ^tKC min	I_{SB1}	55	85	85	70	60	mA	12, 13
CMOS Standby	Device deselected; V_{CC} = MAX; all inputs ≤ V_{SS} +0.2 or ≥ V_{CC} -0.2; all inputs static; CLK frequency = 0	I_{SB2}	0.2	2	2	2	2	mA	12, 13
TTL Standby	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; all inputs static; V_{CC} = MAX; CLK frequency = 0	I_{SB3}	10	18	18	18	18	mA	12, 13
Clock Running	Device deselected; all inputs ≤ V_{IL} OR ≥ V_{IH}; V_{CC} = MAX; CLK cycle time ≥ ^tKC min	I_{SB4}	20	35	35	30	25	mA	12, 13

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	3	4	pF	4
Input/Output Capacitance (DQ)	V_{CC} = 3.3V	C_O	5	6	pF	4

THERMAL CONSIDERATIONS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Thermal resistance - Junction to Ambient	Still Air	θ_{JA}	65	°C/W	
Thermal resistance - Junction to Case		θ_{JC}	6	°C/W	
Maximum Case Temperature		TC	110	°C	11

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±5%)

		-9		-10		-12		-17			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock											
Clock cycle time	^tKC	15		20		25		30		ns	
Clock HIGH time	^tKH	4		5		6		8		ns	
Clock LOW time	^tKL	4		5		6		8		ns	
Output Times											
Clock to output valid	^tKQ		9		10		12		17	ns	
Clock to output invalid	^tKQX	3		3		3		3		ns	
Clock to output in Low-Z	^tKQLZ	5		5		5		5		ns	6, 7
Clock to output in High-Z	^tKQHZ		5		5		6		6	ns	6, 7
$\overline{OE}$ to output valid	^tOEQ		5		5		6		7	ns	9
$\overline{OE}$ to output in Low-Z	^tOELZ	0		0		0		0		ns	6, 7
$\overline{OE}$ to output in High-Z	^tOEHZ		5		5		6		6	ns	6, 7
Setup Times											
Address	^tAS	2.5		3		3		3		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSS	2.5		3		3		3		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAS	2.5		3		3		3		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	^tWS	2.5		3		3		3		ns	8, 10
Data-in	^tDS	2.5		3		3		3		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCES	2.5		3		3		3		ns	8, 10
Hold Times											
Address	^tAH	0.5		0.5		0.5		0.5		ns	8, 10
Address Status ($\overline{ADSC}$, $\overline{ADSP}$)	^tADSH	0.5		0.5		0.5		0.5		ns	8, 10
Address Advance ($\overline{ADV}$)	^tAAH	0.5		0.5		0.5		0.5		ns	8, 10
Byte Write Enables ($\overline{BW1}$, $\overline{BW2}$, $\overline{BW3}$, $\overline{BW4}$)	^tWH	0.5		0.5		0.5		0.5		ns	8, 10
Data-in	^tDH	0.5		0.5		0.5		0.5		ns	8, 10
Chip Enables ($\overline{CE}$, $\overline{CE2}$, CE2)	^tCEH	0.5		0.5		0.5		0.5		ns	8, 10

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

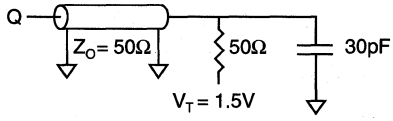


Fig. 1 OUTPUT LOAD EQUIVALENT

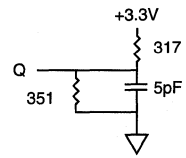
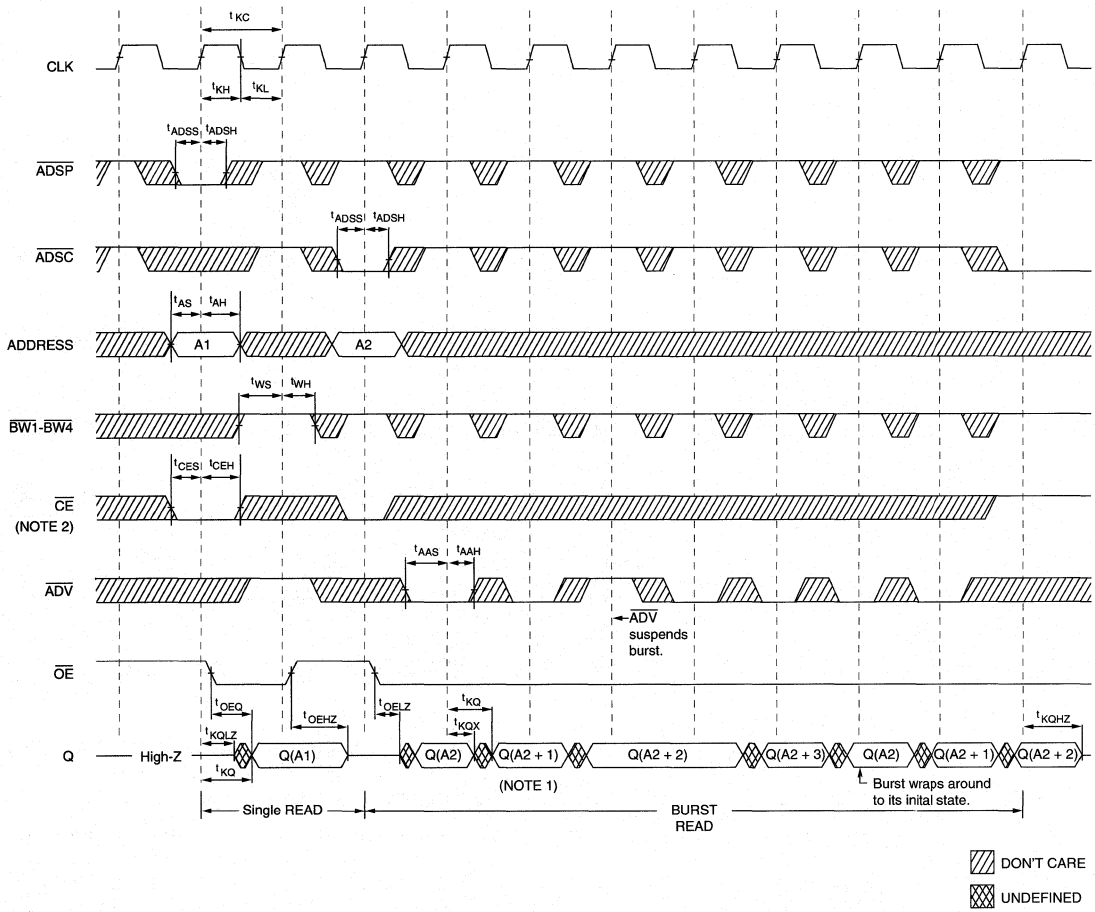


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \geq -2.0V$ for $t \leq {}^tKC/2$.
   Power-up: $V_{IH} \leq +6.0V$ and $Vcc \leq 3.1V$ for $t \leq 200msec$.
3. Icc is given with no output current. Icc increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$ and ${}^tOEHZ$ is less than ${}^tOELZ$.
8. A READ cycle is defined by byte write enables all HIGH or $\overline{ADSP}$ LOW for the required setup and hold times. A WRITE cycle is defined by at least one byte write enable LOW and $\overline{ADSP}$ HIGH for the required setup and hold times.
9. $\overline{OE}$ is a "don't care" when a byte write enable is sampled LOW.
10. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW and chip enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CLK) when chip is enabled. Chip enable must be valid at each rising edge of CLK (when either $\overline{ADSP}$ or $\overline{ADSC}$ is LOW) to remain enabled.
11. Micron does not warrant the functionality or reliability of any product in which the case temperature exceeds 110°C. Care should be taken to limit case temperature to acceptable levels.
12. "Device Deselected" means device is in POWER-DOWN mode as defined in the truth table. "Device Selected" means device is active (not in POWER-DOWN mode).
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.

READ TIMING

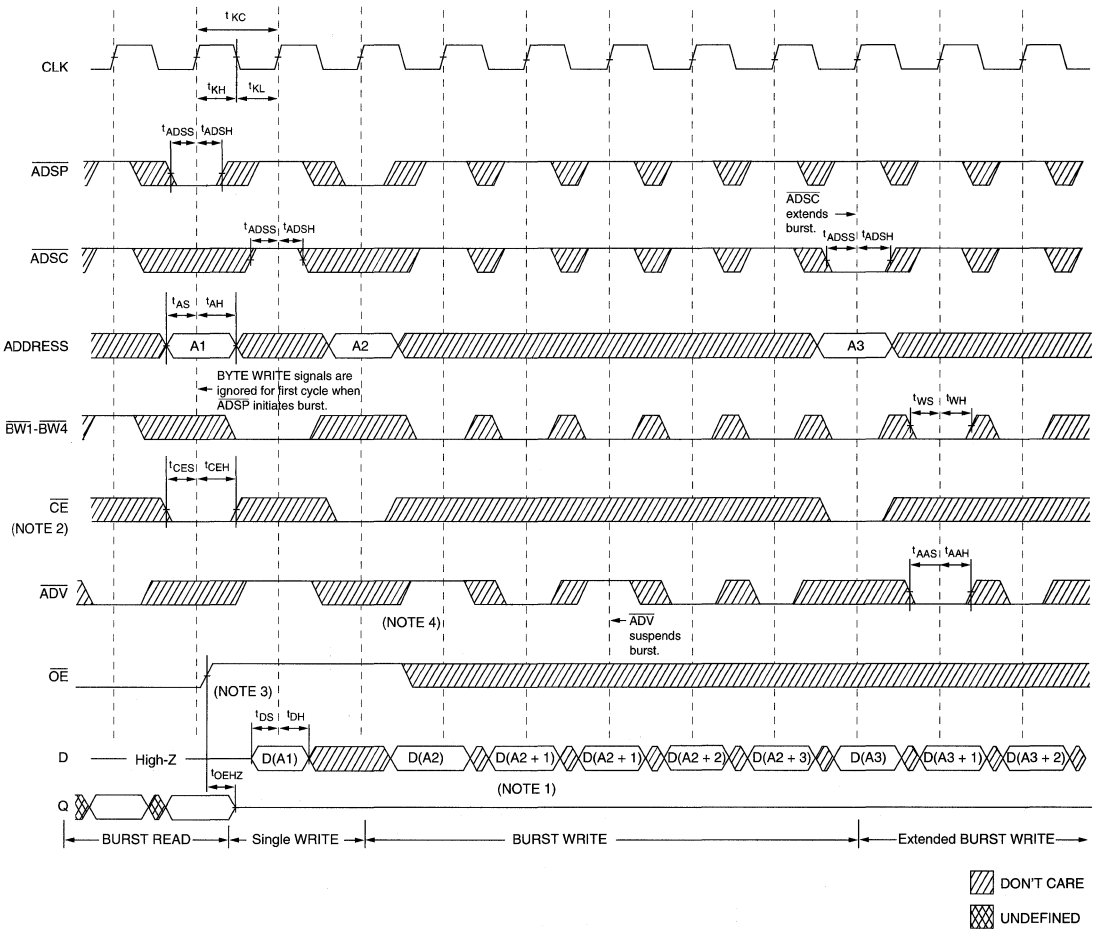


NOTE: 1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

NEW 3.3 VOLT SYNCHRONOUS SRAM

WRITE TIMING

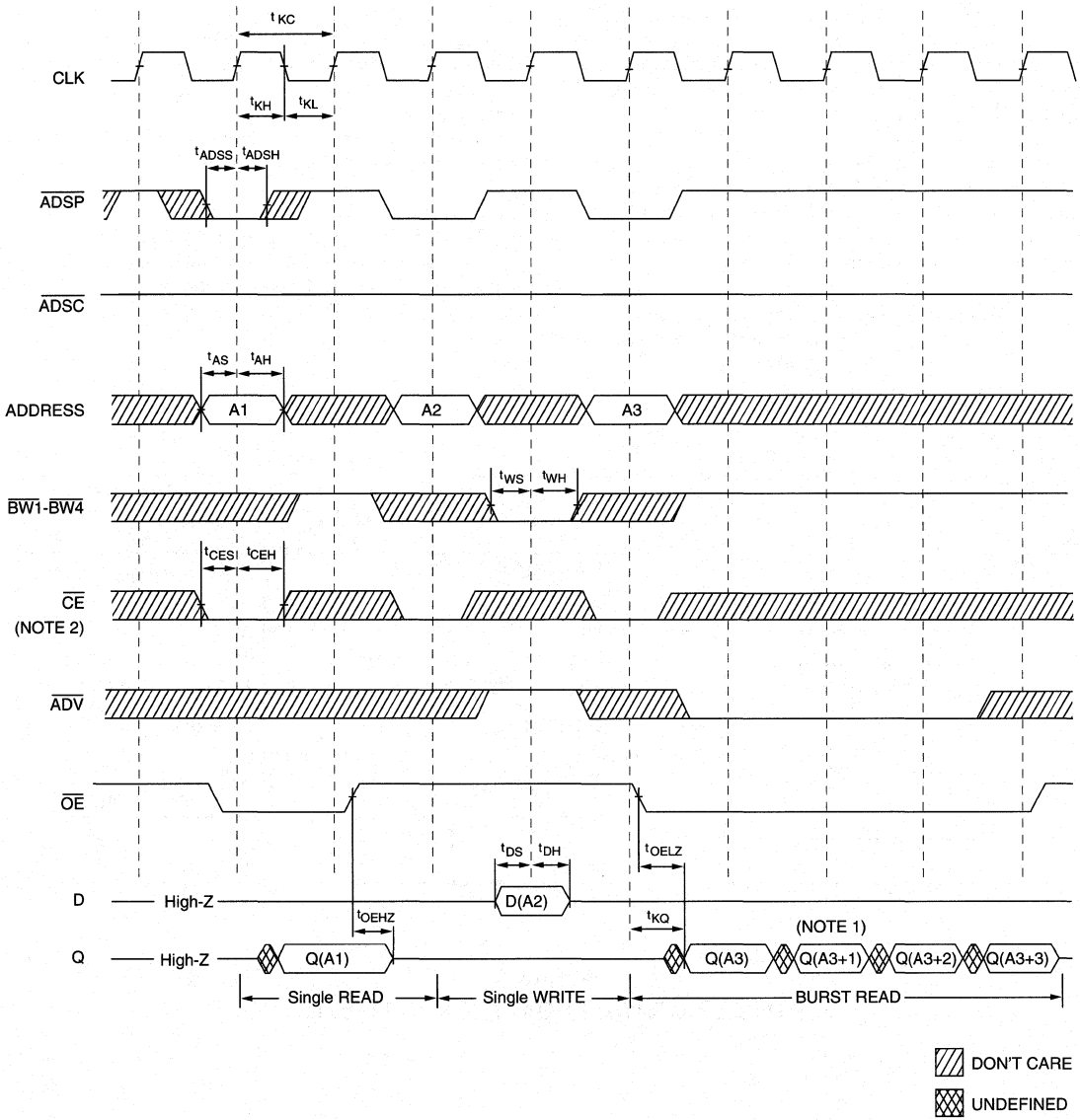


NOTE:

1. Q(A2) refers to output from address A2. Q(A2+1) refers to output from the next internal burst address following A2.
2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.
3. $\overline{OE}$ must be HIGH before the input data setup and held HIGH throughout the the data hold time. This prevents input/output data contention for the time period prior to the byte write enable inputs being sampled.
4. $\overline{ADV}$ must be HIGH to permit a WRITE to the loaded address.

NEW 3.3 VOLT SYNCHRONOUS SRAM

READ/WRITE TIMING



NOTE: 1. Q(A3) refers to output from address A3. Q(A3+1) refers to output from the next internal burst address following A3.

2. $\overline{CE2}$ and CE2 have timing identical to $\overline{CE}$. On this diagram, when $\overline{CE}$ is LOW, $\overline{CE2}$ is LOW and CE2 is HIGH. When $\overline{CE}$ is HIGH, $\overline{CE2}$ is HIGH and CE2 is LOW.

NEW 3.3 VOLT SYNCHRONOUS SRAM

APPLICATION INFORMATION

32-BIT-WIDE SYSTEMS

The Micron 32K x 36 Synchronous SRAM may be used in a 32-bit-wide system without the use of any external components by connecting PDIS to Vcc. This disables the output buffer on the data parity input/output lines (DQP1, DQP2, DQP3 and DQP4).

LOAD DERATING CURVES

The Micron 32K x 36 Synchronous SRAM timing is dependent upon the capacitive loading on the outputs. The data sheet is written assuming a load of 30pF. Access time changes with load capacitance as follows:

$\Delta^tKQ = 0.016$ ns/pF x ΔC_L pF. (Note: this is preliminary information subject to change.)

For example, if the SRAM loading is 22pF, ΔC_L is -8pF (8pF less than rated load). The clock to valid output time of the SRAM is reduced by 0.016 x 8 = 0.128ns. If the device is a 12ns part, the worse case ^tKQ becomes 11.87ns (approximately).

Consult the factory for copies of I/O current versus voltage curves and Quad Design models.

DEPTH EXPANSION

The Micron 32K x 36 Synchronous SRAM incorporates two additional chip enables to facilitate simple depth expansion. This permits easy cache upgrades from 32K depth to 64K depth with no extra logic as shown in Figure 3.

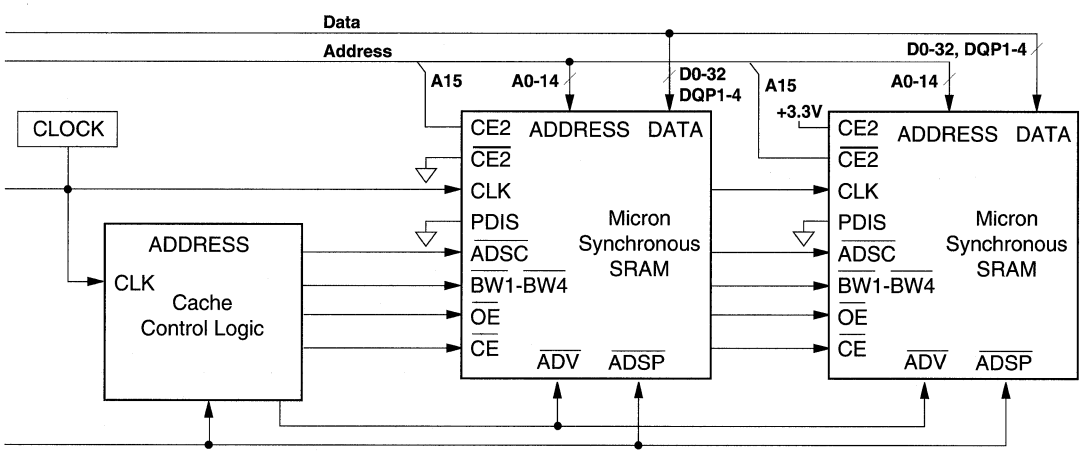


Figure 3
DEPTH EXPANSION FROM 32K x 36 TO 64K x 36

APPLICATION EXAMPLES

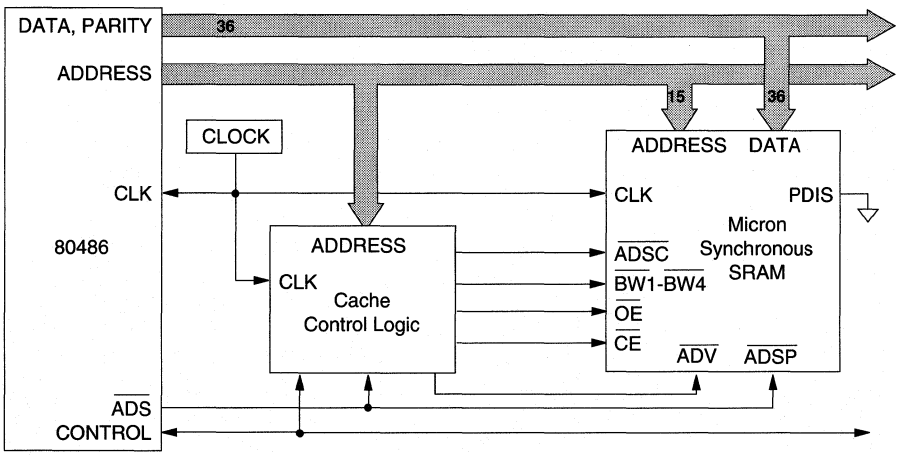


Figure 4
128K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 50 MHz 80486 OR 680X0 USING ONE MT58LC32K36M1LG-12 SYNCHRONOUS SRAM

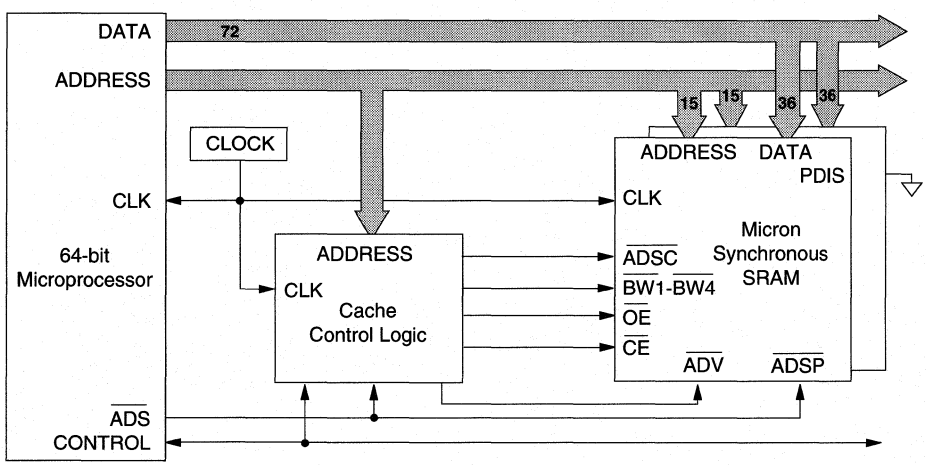


Figure 5
256K BYTE SECONDARY CACHE WITH PARITY AND BURST FOR 66 MHz PROCESSOR USING TWO MT58LC32K36M1LG-9 SYNCHRONOUS SRAMs

MICRON SEMICONDUCTOR, INC.

MT58LC32K36M1
32K x 36 SYNCHRONOUS SRAM