SYNCHRONOUS SRAM

128K x 9 SRAM

FULLY REGISTERED INPUTS AND OUTPUTS

FEATURES

- Timing specific to SPARC® microprocessor
- Fast cycle times: 12, 16.6 and 20ns
- Fast clock to data valid: 6, 8 and 10ns
- Single +5V ±10% power supply
- READ data and WRITE data registers
- Common, TTL-compatible data inputs and outputs
- All inputs and outputs registered with clock
- Fully synchronous, pipelined architecture

OPTIONS — MARKING

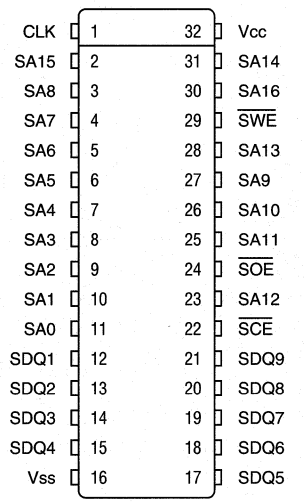
- Timing
  - 6ns access/12ns cycle — -12*
  - 8ns access/16.6ns cycle — -16
  - 10ns access/20ns cycle — -20
- Packages
  - 32-pin SOJ (400mil) — DJ
- Part Number Example: MT58C1289DJ-16

*Preliminary

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

32-Pin SOJ (SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

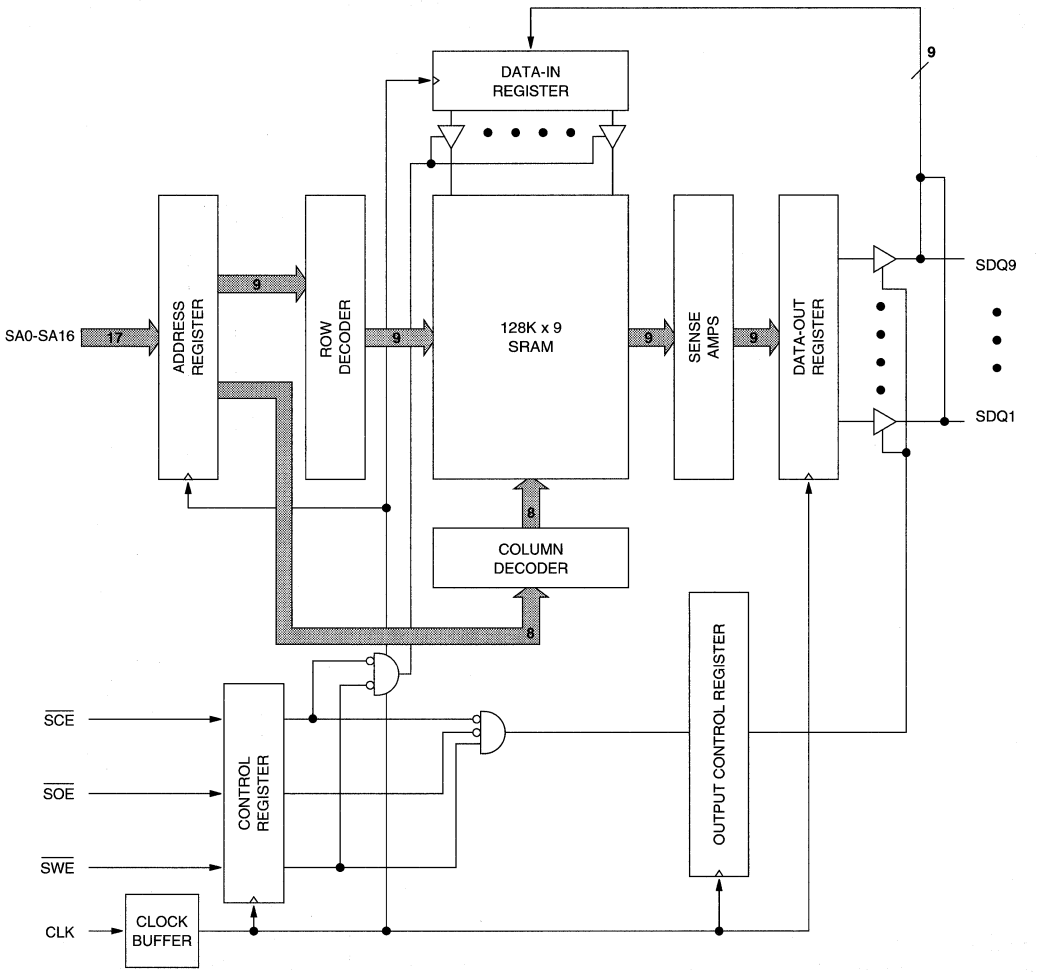
The MT58C1289 is a fully "pipelined" SRAM that integrates registers for address, data-in, data-out and synchronous chip enable ($\overline{SCE}$), output enable ($\overline{SOE}$) and write enable ($\overline{SWE}$). All registers are triggered with the positive edge of the clock signal (CLK).

READ cycles are performed when $\overline{SWE}$ is HIGH and $\overline{SOE}$ and $\overline{SCE}$ are LOW at the positive edge of CLK. Read data is then presented at the next positive edge of CLK.

WRITE cycles occur when $\overline{SWE}$ and $\overline{SCE}$ are LOW at the rising edge CLK. Data present at the data input registers is written to the SRAM address present at the address input registers on that same rising edge of CLK. The WRITE cycle is internally self-timed, eliminating the need for complex write pulse generation external to the SRAM. The WRITE cycle requires three preceding deselect cycles when a WRITE cycle follows a READ cycle. This allows the D/Q lines to be in the High-Z state when write data is applied. The SRAM is deselected if $\overline{SCE}$ is HIGH when a positive edge of CLK occurs.

The MT58C1289 operates from a +5V power supply.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC AND PQFP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
11, 10, 9, 8, 7, 6, 5, 4, 3, 27, 26, 25, 23, 28, 31, 2, 30	SA0-SA16	Input	Address Inputs: These inputs are synchronous and must meet the setup and hold times around the positive edge of CLK. The address inputs are clocked into the address register on each positive edge of CLK.
29	$\overline{SWE}$	Input	Synchronous Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{SWE}$ is LOW for a WRITE cycle and HIGH for a READ cycle. $\overline{SWE}$ is registered on every positive edge of CLK and must meet the setup and hold times referenced to that edge. WRITE cycles are self-timed internally by the SRAM.
1	CLK	Input	Clock: All timing is controlled by the positive edge of CLK. All synchronous input and output signals are registered on the positive edge of CLK and must meet the setup and hold times referenced to that edge.
22	$\overline{SCE}$	Input	Synchronous Chip Enable: This signal is used to enable the device. This is a synchronous input and must meet the setup and hold times around CLK. When $\overline{SCE}$ is HIGH, the SRAM automatically goes into the standby power mode.
24	$\overline{SOE}$	Input	Synchronous Output Enable: This active LOW input enables the output drivers. This is a synchronous input and must meet the setup and hold times around CLK.
12, 13, 14, 15, 17, 18, 19, 20, 21	SDQ1-SDQ9	Input/ Output	SRAM Data I/O: For a READ, control signals and address are presented at the rising edge of CLK and data is valid ^{t}KQ after the next rising edge of CLK. Data presented for a WRITE cycle must meet the setup and hold times around CLK.
32	Vcc	Supply	Power Supply: +5V ±10%
16	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	$\overline{SCE}$	$\overline{SWE}$	CLK	$\overline{SOE}$	D	Q NEXT CLOCK	POWER
Deselected	H	X	↑	X	X	High-Z	Standby
READ	L	H	↑	H	X	High-Z	Active
READ	L	H	↑	L	X	Q1-Q9	Active
WRITE	L	L	↑	X	D1-D9	High-Z	Active

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +7V
Voltage on any pin relative to V_{SS} ..... -1V to V_{CC}+1V
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -1.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 4.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-12	-16	-20	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX outputs open f = MAX = 1/ ^tRC	I_{CC}	200	160	150	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX outputs open f = MAX = 1/ ^tRC	I_{SB1}	90	70	60	mA	
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX; V_{IL} ≤ V_{SS} +0.2V V_{IH} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	5	pF	4
Input/Output Capacitance (D/Q)	V_{CC} = 5V	$C_{I/O}$	7	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

		-12*		-16		-20			
DESCRIPTION	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Clock									
Clock cycle time	^tKC	12		16.6		20		ns	
Clock HIGH time	^tKH	4		5		5		ns	
Clock LOW time	^tKL	4		5		5		ns	
READ Cycle									
READ cycle time	^tRC	12		16.6		20		ns	9
Address setup time	^tSAS	3		3		3		ns	9
Address hold time	^tSAH	0.5		0.5		1		ns	9
Chip Enable setup time	^tSCES	3		3		3		ns	9
Chip Enable hold time	^tSCEH	0.5		0.5		1		ns	9
Output Enable setup time	^tSOES	3		3		3		ns	9
Output Enable hold time	^tSOEH	0.5		0.5		1		ns	9
Write Enable setup time	^tSWES	3		3		3		ns	9
Write Enable hold time	^tSWEH	0.5		0.5		1		ns	9
Output hold time from clock	^tKOH	1		2		3		ns	
Clock to data valid	^tKQ		6		8		10	ns	
Clock to output High-Z	^tKQHZ		6		8		10	ns	4, 6, 7
Clock to output Low-Z	^tKQLZ	0		0		0		ns	4, 6, 7
WRITE Cycle									
WRITE cycle time	^tWC	12		16.6		20		ns	
Address setup time	^tSAS	3		3		3		ns	9
Address hold time	^tSAH	0.5		0.5		1		ns	9
Chip Enable setup time	^tSCES	3		3		3		ns	9
Chip Enable hold time	^tSCEH	0.5		0.5		1		ns	9
Write Enable setup time	^tSWES	3		3		3		ns	9
Write Enable hold time	^tSWEH	0.5		0.5		1		ns	9
Data setup time	^tSDS	3		3		3		ns	
Data hold time	^tSDH	0.5		0.5		1		ns	

*Preliminary. Consult factory for availability.

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

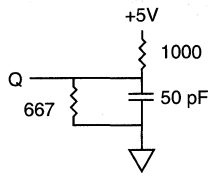


Fig. 1 OUTPUT LOAD EQUIVALENT

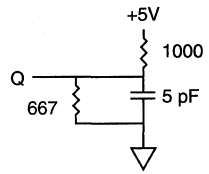
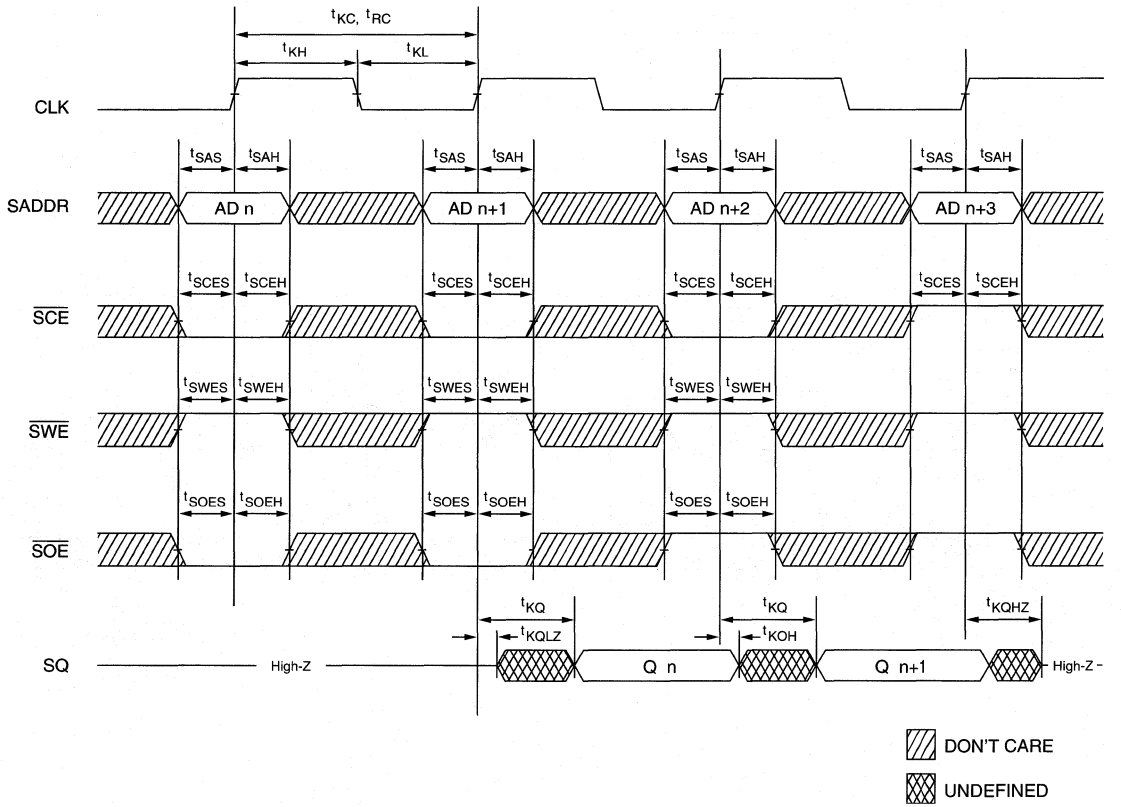


Fig. 2 OUTPUT LOAD EQUIVALENT

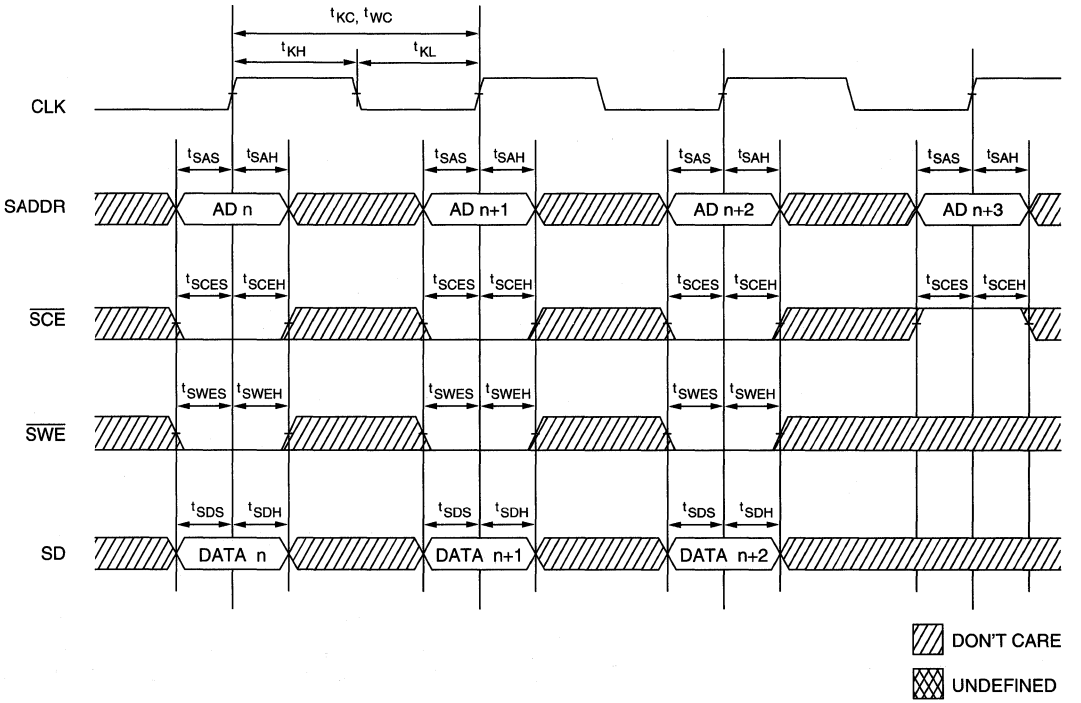
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^{t}RC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, $^{t}KQHZ$ is less than $^{t}KQLZ$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. This is a synchronous device. All synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK.

READ TIMING [7, 8, 9]



WRITE TIMING [7, 9]



READ/WRITE TIMING [7, 8, 9]