www.DataSheet4U.com

DRAM

1 MEG x 1 DRAM

STATIC COLUMN

FEATURES

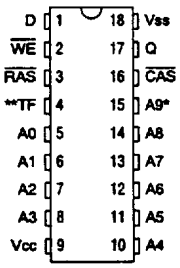
- Industry-standard x1 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single +5V ±10% power supply
- Low power, 3mW standby; 175mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- 512-cycle refresh in 8ms
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), and HIDDEN
- STATIC COLUMN access cycle

OPTIONS — MARKING

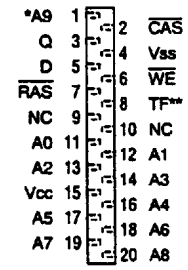
- Timing
  - 70ns access — -7
  - 80ns access — -8
  - 100ns access — -10
- Packages
  - Plastic DIP (300 mil) — None
  - Plastic SOJ (300 mil) — DJ
  - Plastic ZIP (350 mil) — Z
- Part Number Example: MT4C1026DJ-7

PIN ASSIGNMENT (Top View)

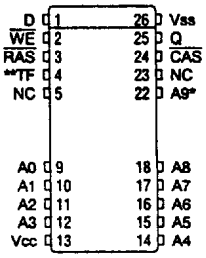
18-Pin DIP (DA-1)



20-Pin ZIP (DB-1)



20/26-Pin SOJ (DC-1)



*Address not used for $\overline{RAS}$ ONLY REFRESH
**TF = Test Function; V_{IN} must not exceed Vcc+1V for normal operation.

GENERAL DESCRIPTION

The MT4C1026 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x1 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at a time. $\overline{RAS}$ is used to latch the first 10 bits and $\overline{CAS}$ the latter 10 bits. A READ or WRITE cycle is selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin, data-out (Q), remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, Q is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A9) page boundary. After the first READ, any column-address transition will result in new data-out. Unlike the PAGE MODE, which requires $\overline{CAS}$ to be toggled for each successive PAGE MODE access, the STATIC COLUMN allows $\overline{CAS}$ to be left LOW for successive STATIC COLUMN accesses. Returning $\overline{RAS}$ HIGH terminates the STATIC COLUMN operation.

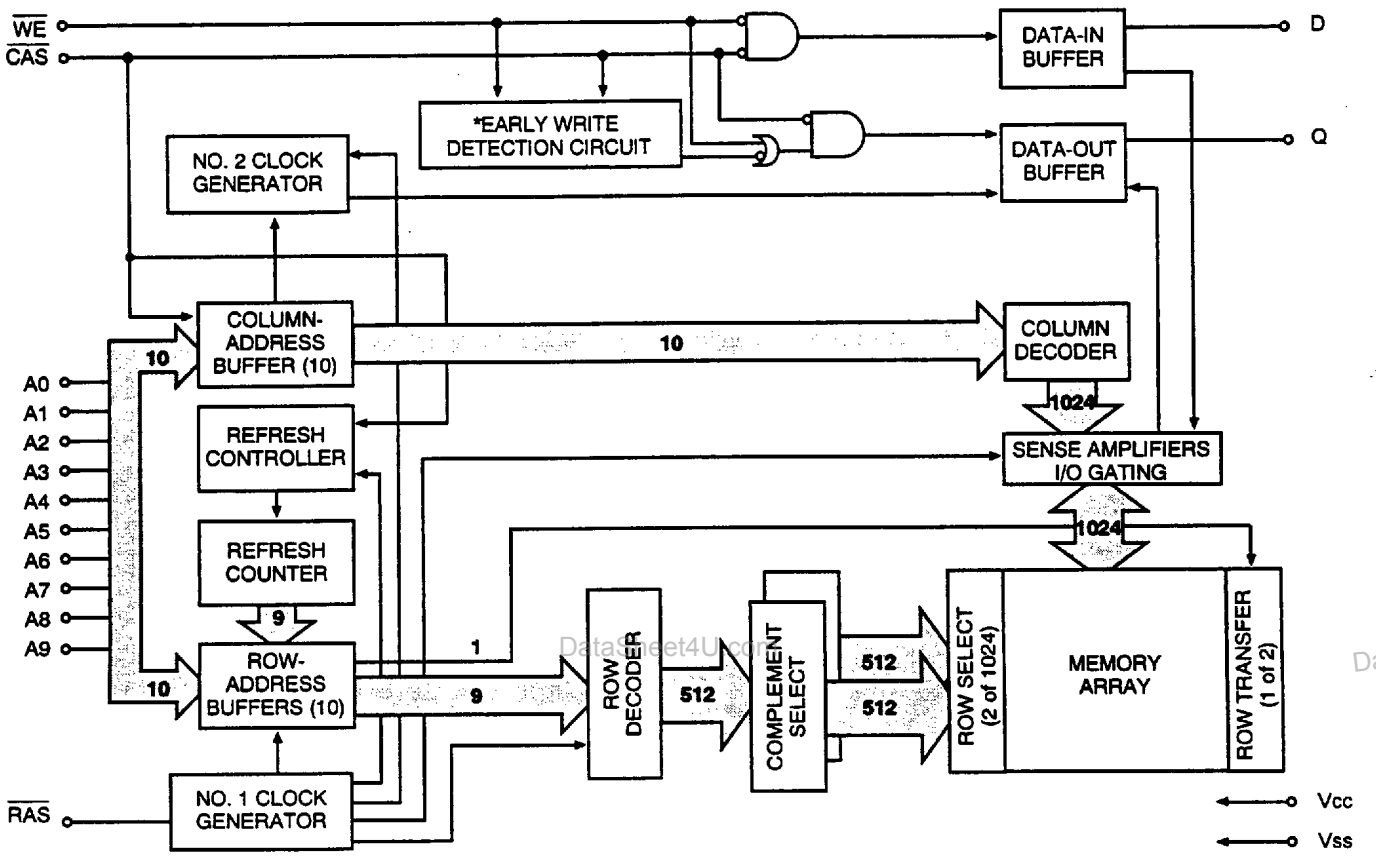
Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 512 combinations of $\overline{RAS}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

TRUTH TABLE

FUNCTION		RAS	CAS	WE	ADDRESSES		DATA	
					^tR	^tC	D (Data-In)	Q (Data-Out)
Standby		H	H→X	X	X	X	"don't care"	High-Z
READ		L	L	H	ROW	COL	"don't care"	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
STATIC-COLUMN READ	1st Cycle	L	L	H	ROW	COL	"don't care"	Data-Out
	2nd Cycle	L	L	H	n/a	COL	"don't care"	Data-Out
STATIC-COLUMN EARLY-WRITE	1st Cycle	L	L	L	ROW	COL	Data-In	High-Z
	2nd Cycle	L	L	H→L	n/a	COL	Data-In	High-Z
STATIC-COLUMN READ-WRITE	1st Cycle	L	L	H→L	ROW	COL	Data-In	Data-Out
	2nd Cycle	L	L	H→L	n/a	COL	Data-In	Data-Out
RAS ONLY REFRESH		L	H	X	ROW	n/a	"don't care"	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	ROW	COL	"don't care"	Data-Out
	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	X	X	X	"don't care"	High-Z

et4U.com
DataSheet4U.com
DataShee

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

et4U.com DataSheet4U.com DataShee

		MAX				
PARAMETER/CONDITION	SYMBOL	-7	-8	-10	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} -0.2V)	I_{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	80	70	60	mA	3, 4
OPERATING CURRENT: STATIC COLUMN Average power supply current ($\overline{RAS}$ = V_{IL}; $\overline{CAS}$, Address Cycling: ^tSC = ^tSC [MIN])	I_{CC4}	60	50	40	mA	3, 4
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling; $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	80	70	60	mA	3
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	80	70	60	mA	3, 5

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

DataSheet4U.com www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: A0-A9, D	C_{I1}		5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}		7	pF	2
Output Capacitance: Q	C_O		7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	130		150		180		ns	
READ WRITE cycle time	t_{RWC}	155		175		205		ns	
STATIC-COLUMN READ or WRITE cycle time	t_{SC}	35		40		50		ns	
STATIC-COLUMN READ-WRITE cycle time	t_{SRWC}	70		80		100		ns	
Access time from $\overline{RAS}$	t_{RAC}		70		80		100	ns	14
Access time from $\overline{CAS}$	t_{CAC}		20		20		25	ns	15
Access time from column-address	t_{AA}		35		40		50	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ pulse width (STATIC COLUMN)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		20		25		ns	
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	70		80		100		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		15		ns	16
$\overline{CAS}$ precharge time (STATIC COLUMN)	t_{CP}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		5		ns	
Row-address setup time	t_{ASR}	0		0		0		ns	
Row-address hold time	t_{RAH}	10		10		15		ns	
$\overline{RAS}$ to column-address delay time	t_{RAD}	15	35	15	40	20	50	ns	18
Column-address setup time	t_{ASC}	0		0		0		ns	
Column-address hold time	t_{CAH}	15		15		20		ns	
Column-address hold time (referenced to $\overline{RAS}$)	t_{AR}	80		90		100		ns	
Column-address to $\overline{RAS}$ lead time	t_{RAL}	35		40		50		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0		0		0		ns	
Output buffer turn-off delay	t_{OFF}	3	20	3	20	3	20	ns	20, 24

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-7		-8		-10			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Column-address hold time EARLY WRITE (referenced to $\overline{RAS}$)	tAWR	55		60		70		ns	
$\overline{WE}$ command setup time	tWCS	0		0		0		ns	21
Write command hold time	tWCH	15		15		20		ns	
Write command hold time (referenced to $\overline{RAS}$)	tWCR	55		60		75		ns	
Write command pulse width	tWP	15		15		20		ns	
Write command to $\overline{RAS}$ lead time	tRWL	20		20		25		ns	
Write command to $\overline{CAS}$ lead time	tCWL	20		20		25		ns	
Data-in setup time	tDS	0		0		0		ns	22
Data-in hold time	tDH	15		15		20		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	tDHR	55		60		75		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	tRWD	70		80		100		ns	21
Column-address to $\overline{WE}$ delay time	tAWD	35		40		50		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	tCWD	20		20		25		ns	21
Transition time (rise or fall)	tT	3	50	3	50	3	50	ns	9, 10
Refresh period (512 cycles)	tREF		8		8		8	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	tRPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	tCSR	10		10		10		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	tCHR	15		15		15		ns	5
Write inactive time	tWI	10		10		10		ns	
Previous WRITE to column-address delay time	tLWAD	20	30	20	35	25	45	ns	
Previous WRITE to column-address hold time	tAHLW	65		75		95		ns	
Output data hold time from column-address	tAOH	5		5		5		ns	
Output data enable from WRITE	tOW	tAA + 5		tAA + 5		tAA + 5		ns	
Access time from last WRITE	tALW	65		75		95		ns	
Column-address hold time referenced to $\overline{RAS}$ HIGH	tAH	5		5		10		ns	
$\overline{CAS}$ pulse width in STATIC COLUMN mode	tCSC	tCAS		tCAS		tCAS		ns	
Output data hold from WRITE	tWOH	0		0		0		ns	

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

NOTES

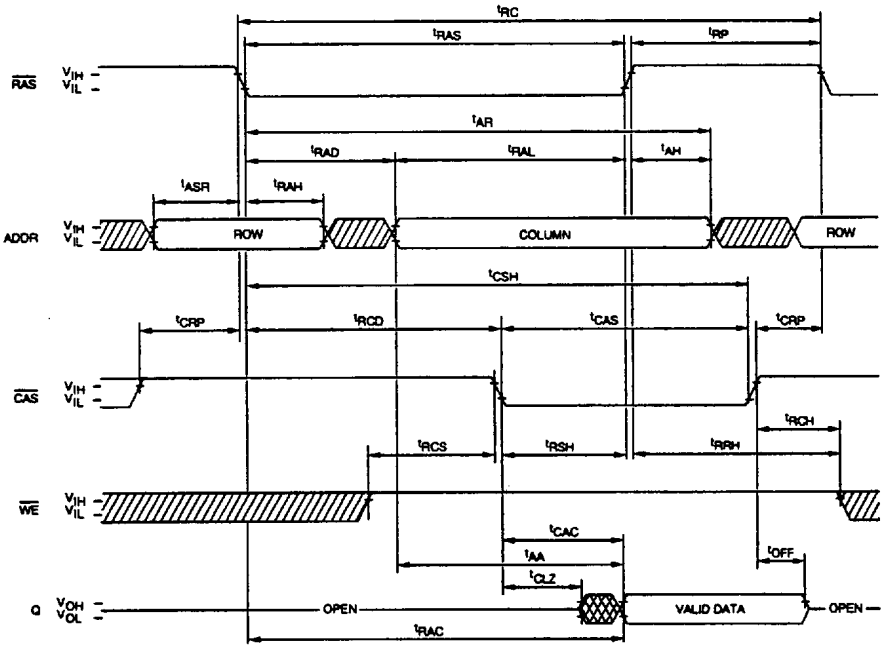
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by any eight $\overline{RAS}$ cycles before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
8. AC characteristics assume ^{t}T = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^{t}RCD < {}^{t}RCD$ (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
15. Assumes that $^{t}RCD \geq {}^{t}RCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^{t}CPN.
17. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, then access time is controlled exclusively by ^{t}CAC.
18. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, then access time is controlled exclusively by ^{t}AA.
19. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
20. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
21. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are restrictive operating parameters in LATE WRITE, and READ-MODIFY-WRITE cycles only. If $^{t}WCS \geq {}^{t}WCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^{t}RWD \geq {}^{t}RWD$ (MIN), $^{t}AWD \geq {}^{t}AWD$ (MIN) and $^{t}CWD \geq {}^{t}CWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of Q is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. The 3ns minimum is a parameter guaranteed by design.

Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

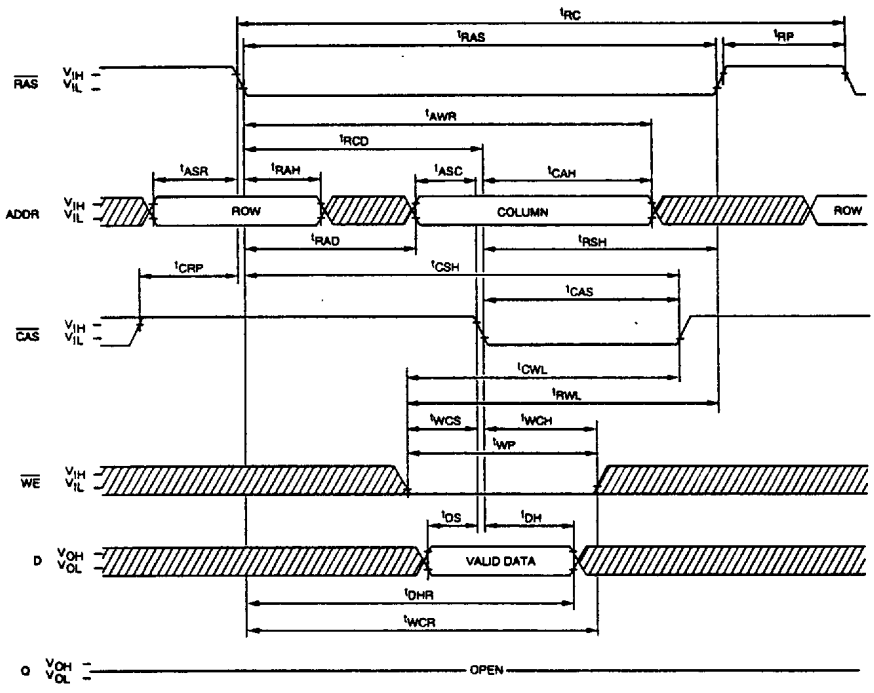
DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

READ CYCLE



EARLY WRITE CYCLE

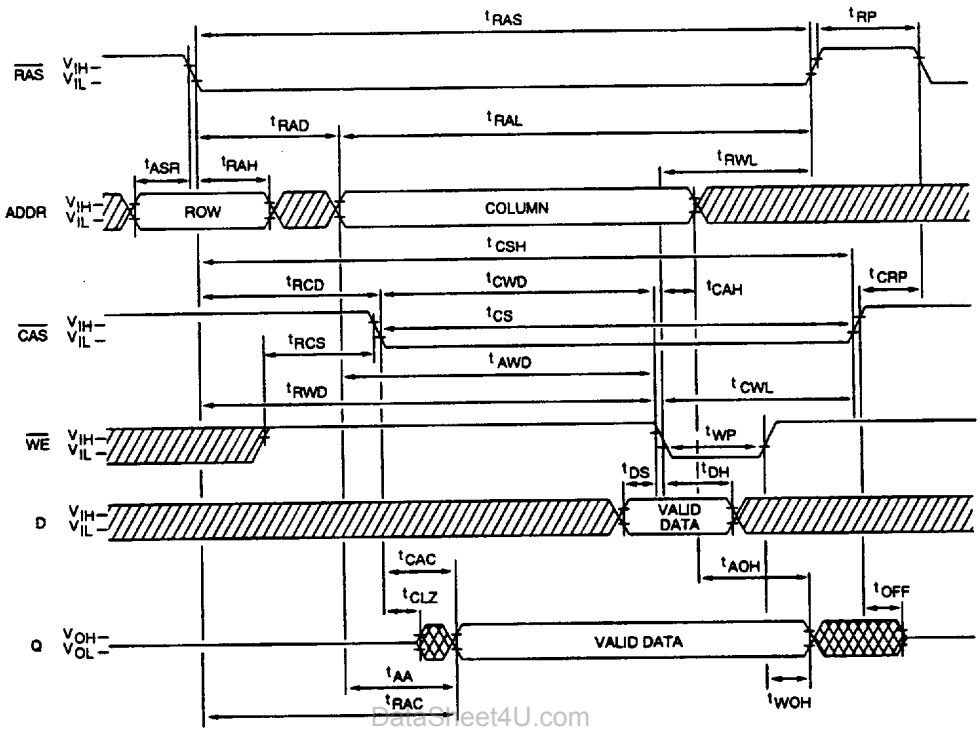


Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

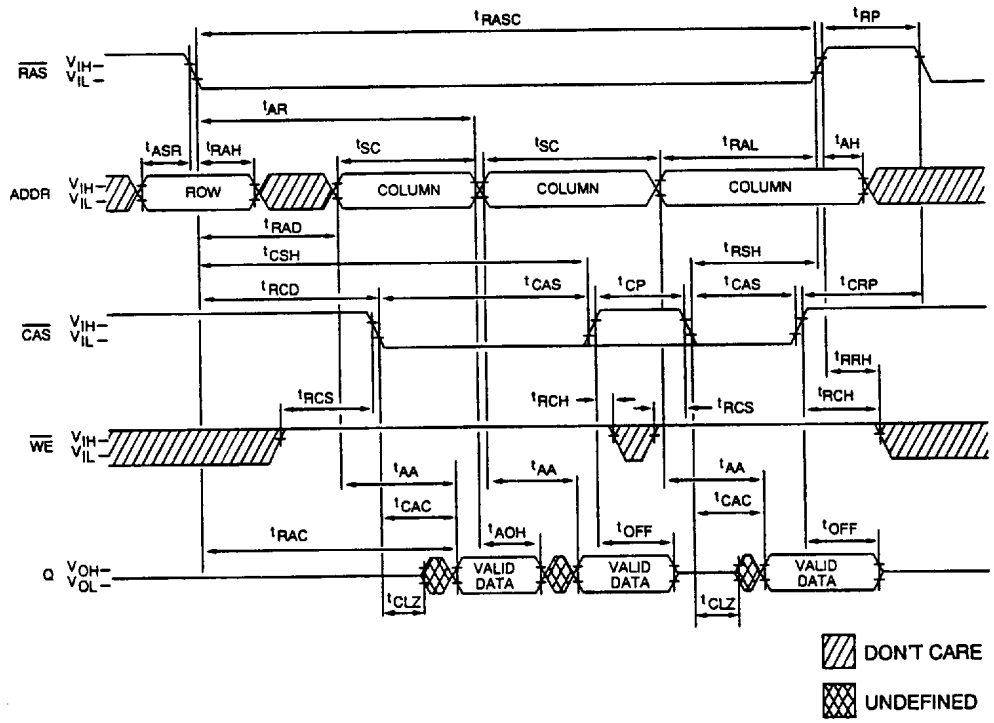
DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



STATIC-COLUMN READ CYCLE

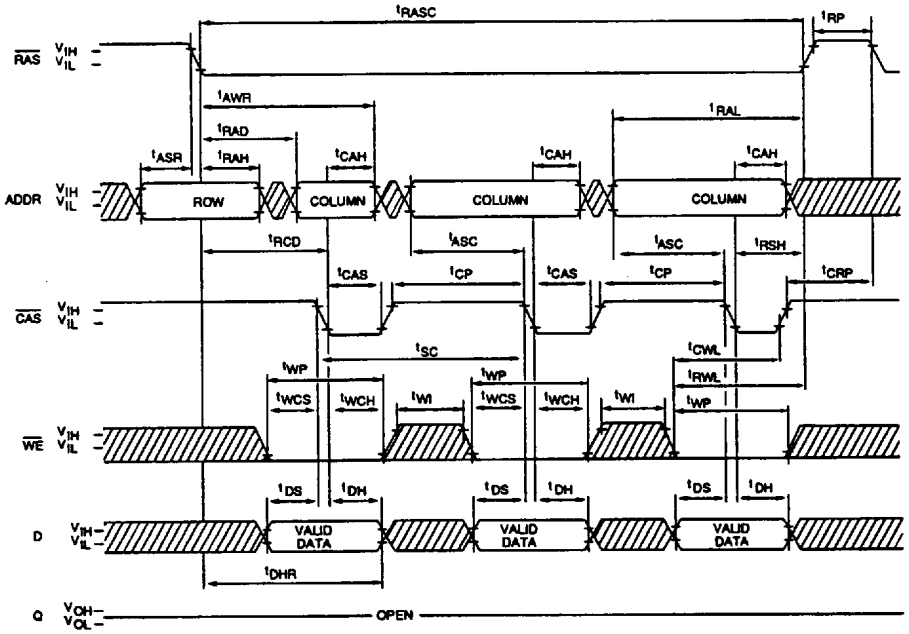


Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

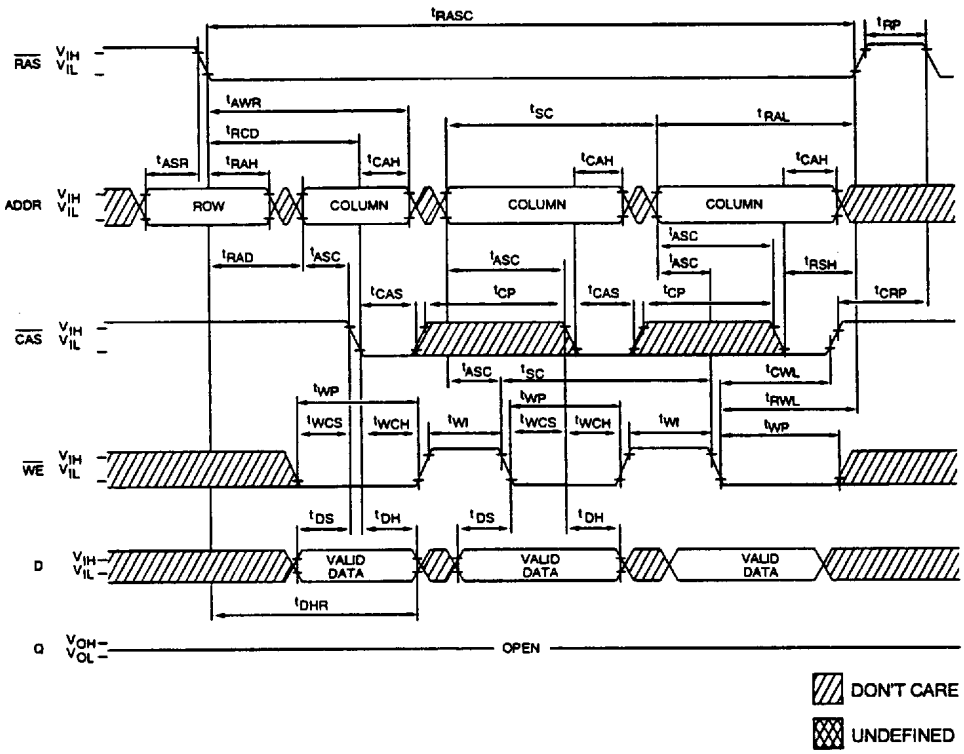
DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

STATIC-COLUMN EARLY-WRITE CYCLE
(CAS Controlled)



STATIC-COLUMN EARLY-WRITE CYCLE
(WE Controlled)

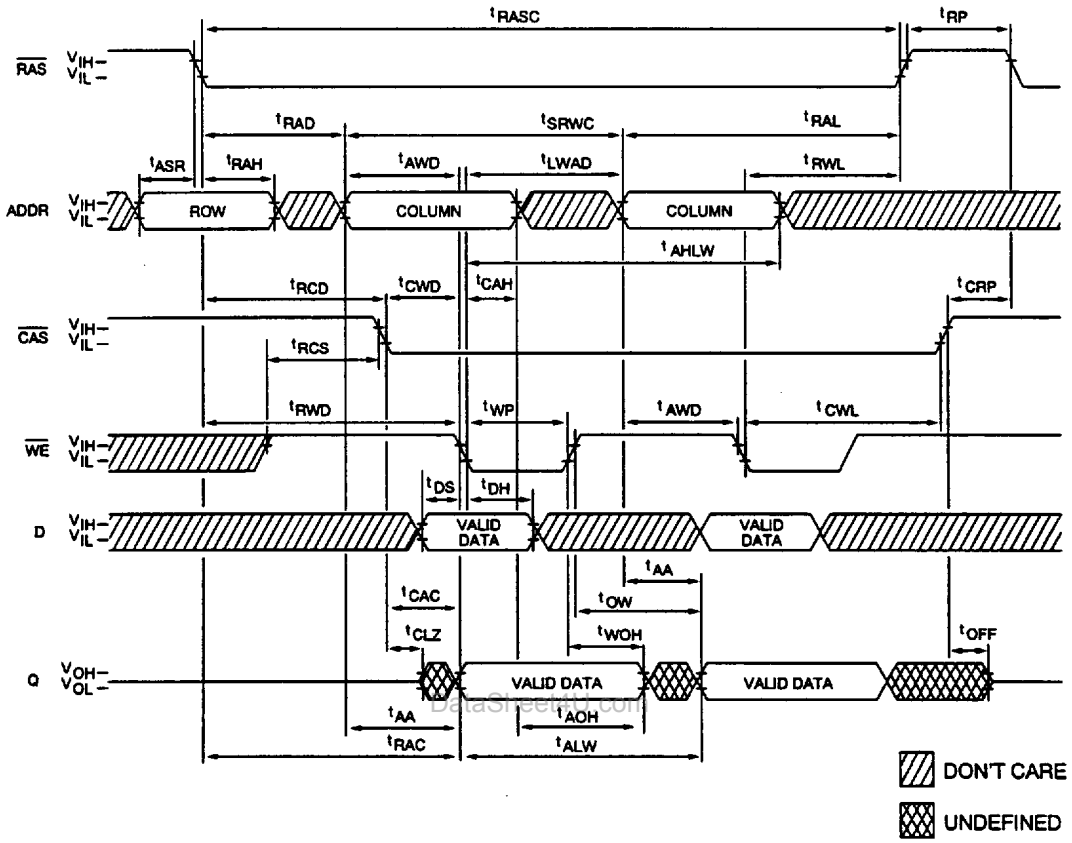


Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

STATIC-COLUMN READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)

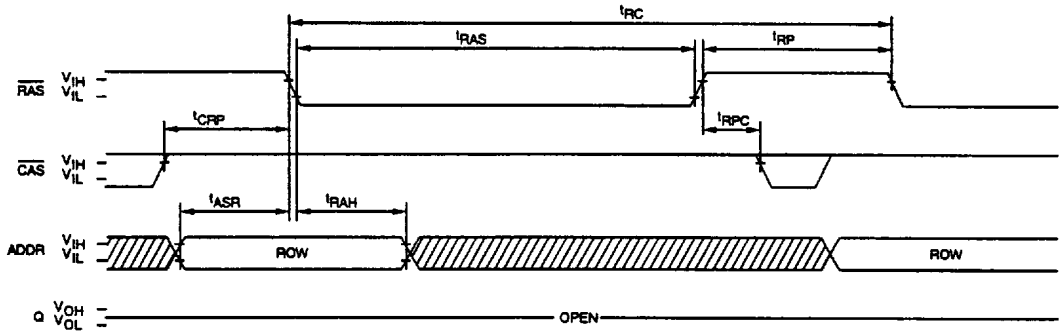


Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

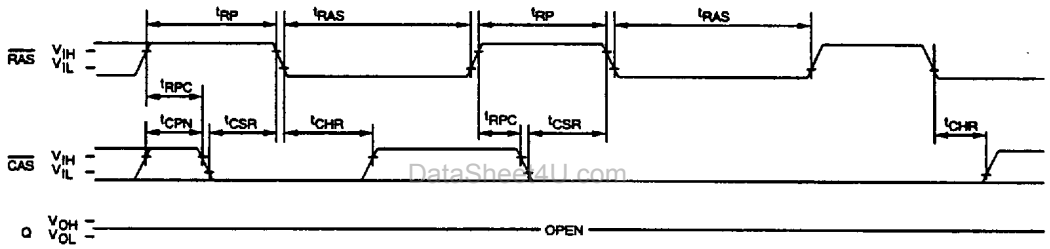
DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com

www.DataSheet4U.com

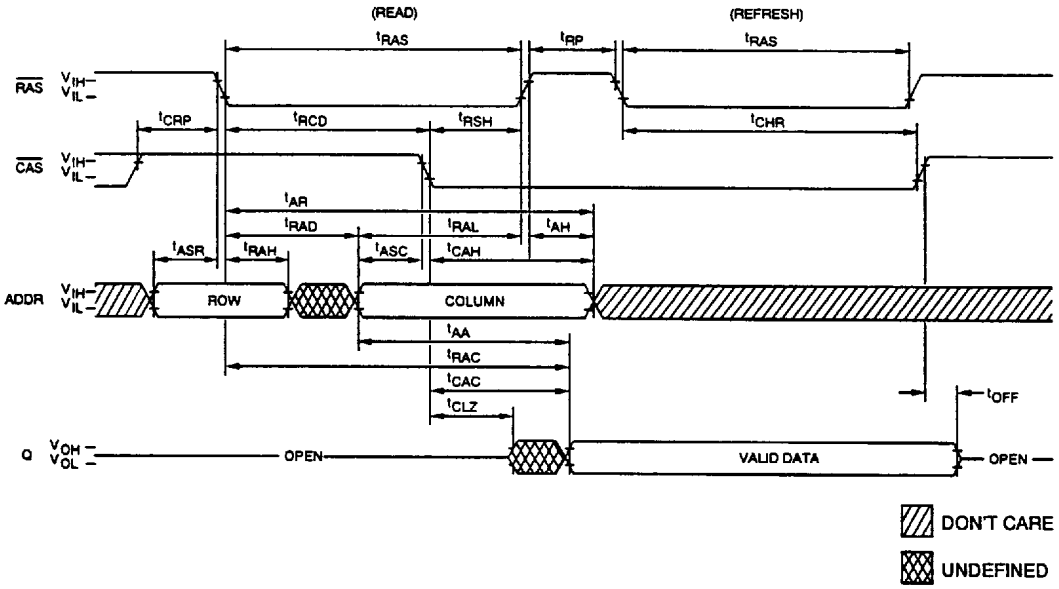
$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A8; A9 and $\overline{WE}$ = DON'T CARE)



CBR REFRESH CYCLE
(A0-A9 and $\overline{WE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)



Micron Semiconductor, Inc., reserves the right to change products or specifications without notice.
©1994, Micron Semiconductor, Inc.

DataSheet4U.com
www.DataSheet4U.com
DataSheet4U.com
DataSheet4U.com