MT4613

Dual N & P-Channel PowerTrench® MOSFET

MT Semiconductor®

http://www.mtsemi.com

General Description

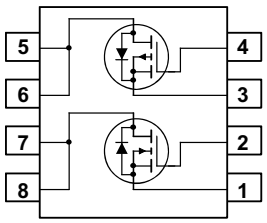
These dual N and P-Channel enhancement mode power field effect transistors are produced using MOS-TECH Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

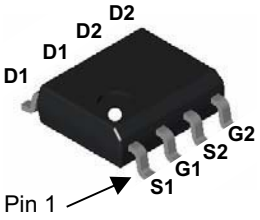
- N-Channel
  20V/5A
  $R_{DS(on)}$ = 0.017Ω @ V_{GS} = 4.5V
  $R_{DS(on)}$ = 0.020Ω @ V_{GS} = 2.5V
- P-Channel
  -15V/-4.5A
  $R_{DS(on)}$ = 0.028Ω @ V_{GS} = -4.5V
  $R_{DS(on)}$ = 0.038Ω @ V_{GS} = -2.5V

Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT

SO-8



Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Symbol	Parameter		N-CH	P-CH	Units
V_{DSS}	Drain-Source Voltage		20	-15	V
V_{GSS}	Gate-Source Voltage		±10	±12	V
I_D	Drain Current - Continuous	(Note 1)	5	-4.5	A
	- Pulsed		20	-18	
P_D	Power Dissipation for Dual Operation	(Note 1)	2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MT4613	MT4613	13"	12mm	2500 units

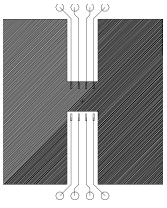
N-CH Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	20	21.5	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±10V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.5	0.70	1.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=2.5V, I_D=4.5 A	-	20	35	mΩ
		V_{GS}=4.5V, I_D=5A	-	17	28	mΩ
Forward Transconductance	g_{FS}	V_{DS}=15V,I_D=5A	25	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=10V,V_{GS}=0V, F=1.0MHz	-	780	-	PF
Output Capacitance	C_{oss}		-	140	-	PF
Reverse Transfer Capacitance	C_{rss}		-	80	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V,I_D=1A V_{GS}=4.5V,R_{GEN}=6Ω	-	9	-	nS
Turn-on Rise Time	t_r		-	30	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	35	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	V_{DS}=10V,I_D=5A,V_{GS}=4.5V	-	11.4	-	nC
Gate-Source Charge	Q_{gs}		-	2.3	-	nC
Gate-Drain Charge	Q_{gd}		-	2.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=1A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	5	A

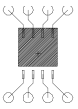
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

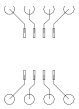
$R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°/W when mounted on a 0.5 in^2 pad of 2 oz copper



b) 125°/W when mounted on a .02 in^2 pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

P-CH Electrical Characteristics (T_A=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-15	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-15V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-0.45	-0.7	-1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-4 A	-	28	40	mΩ
		V_{GS}=-2.5V, I_D=-2A	-	38	55	
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-4A	-	13	-	S
Dynamic Characteristics (Note7)						
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz	-	1159	-	PF
Output Capacitance	C_{oss}		-	133	-	PF
Reverse Transfer Capacitance	C_{rss}		-	118	-	PF
Switching Characteristics (Note7)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-10V,I_D=-3.2A , R_L=2.2Ω,V_{GS}=-4.5V,R_g=1Ω	-	23	-	nS
Turn-on Rise Time	t_r		-	25	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	t_f		-	13	-	nS
Total Gate Charge	Q_g	V_{DS}=-10V,I_D=-4A,V_{GS}=-4.5V	-	14.5	-	nC
Gate-Source Charge	Q_{gs}		-	2.2	-	nC
Gate-Drain Charge	Q_{gd}		-	2.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	V_{GS}=0V,I_S=-5.3A	-	-	-1.2	V
Diode Forward Current (Note 5)	I_S		-	-	-5.3	A

Notes:

5. Surface Mounted on FR4 Board, t ≤ 10 sec.
6. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
7. Guaranteed by design, not subject to production

N- Channel Typical Electrical and Thermal Characteristics (Curves)

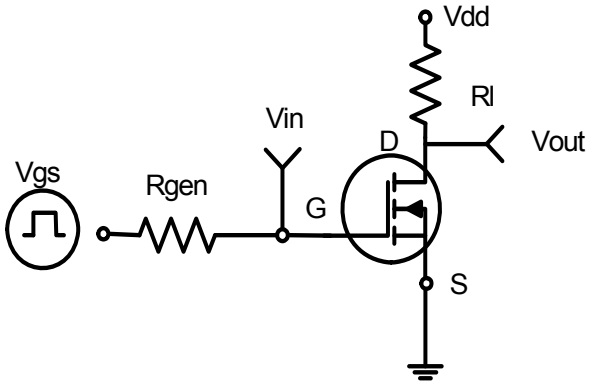


Figure 1:Switching Test Circuit

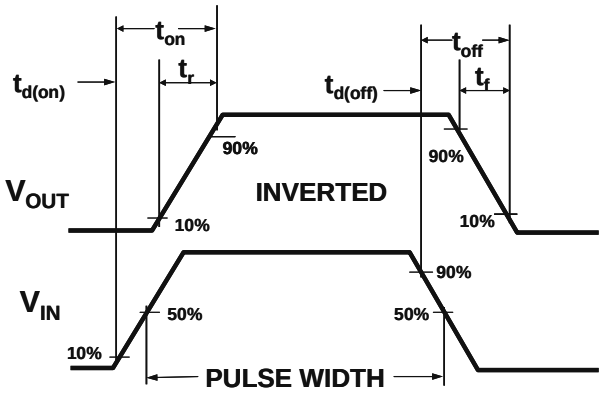


Figure 2:Switching Waveforms

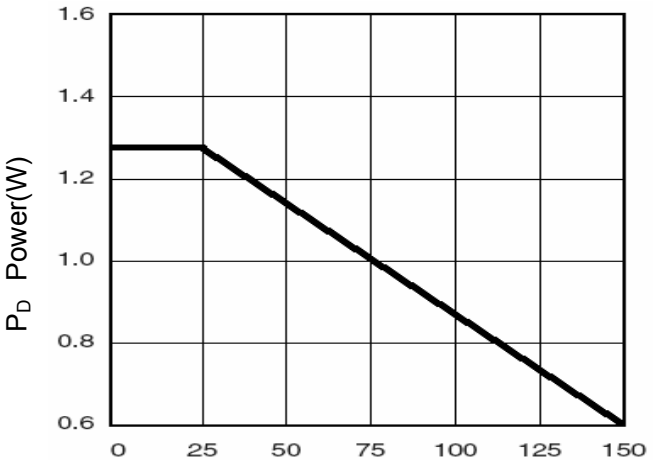


Figure 3 Power Dissipation

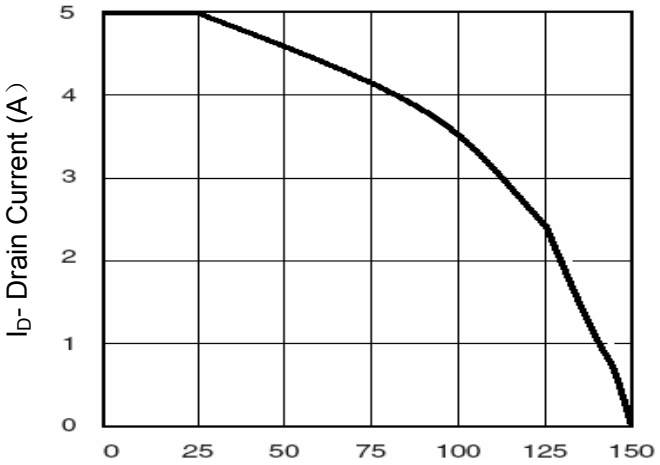


Figure 4 Drain Current

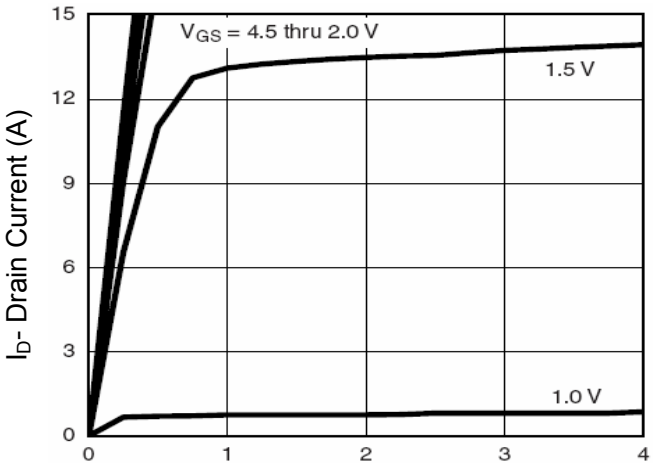


Figure 5 Output Characteristics

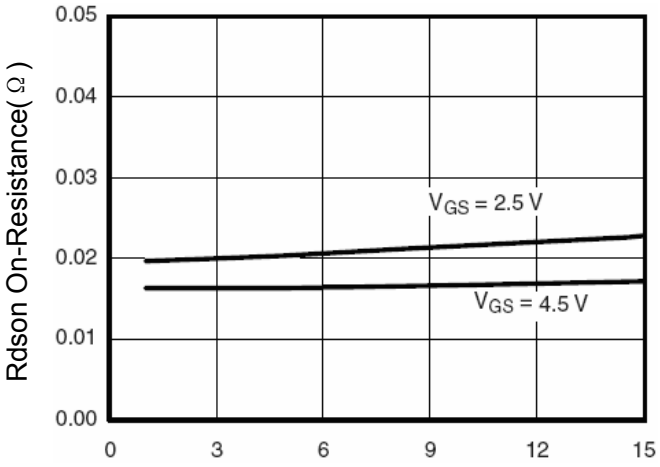


Figure 6 Drain-Source On-Resistance

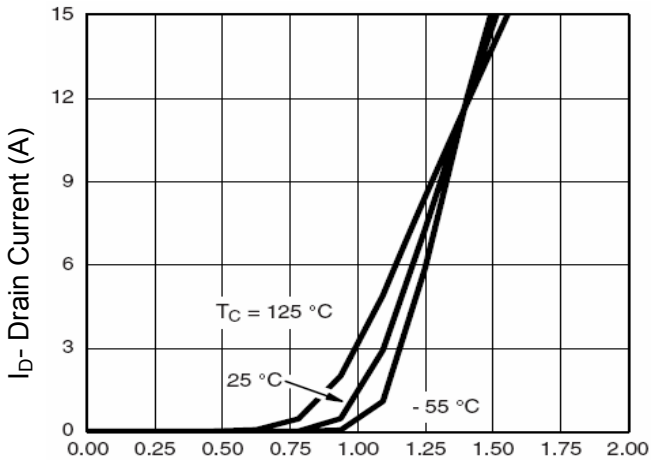


Figure 7 Transfer Characteristics

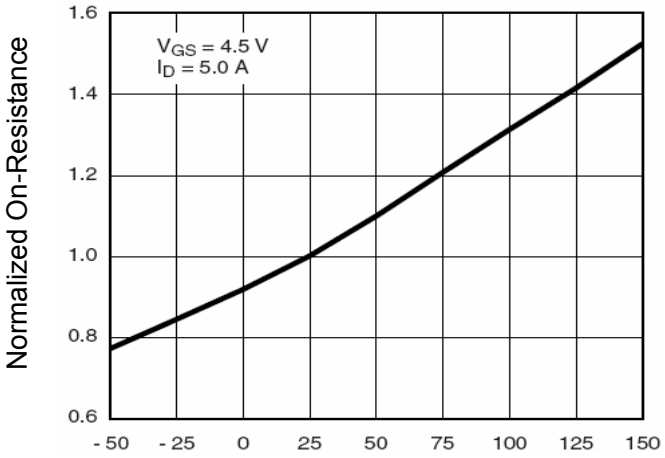


Figure 8 Drain-Source On-Resistance

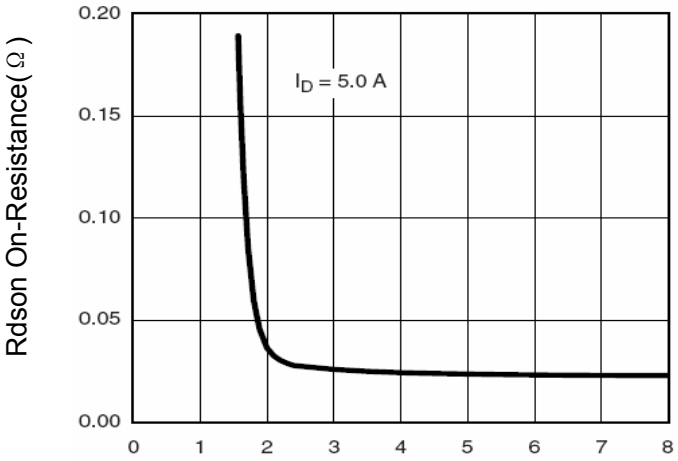


Figure 9 Rdson vs Vgs

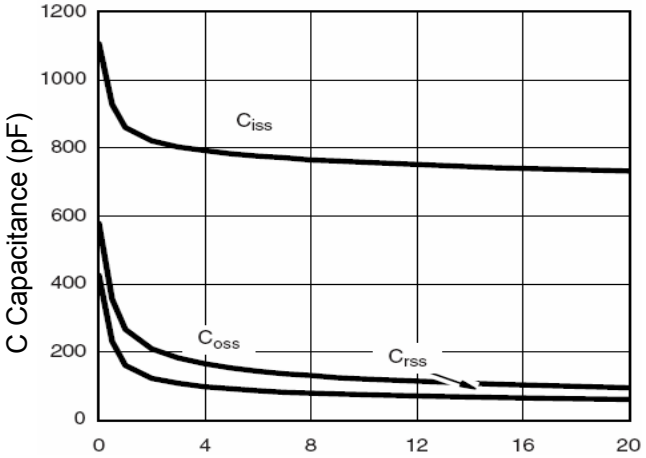


Figure 10 Capacitance vs Vds

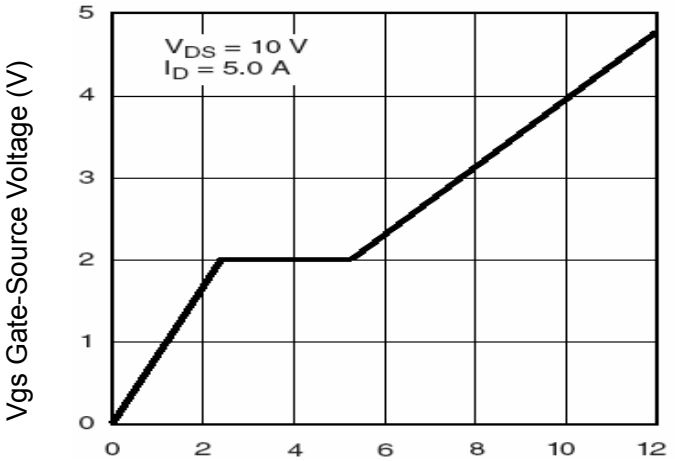


Figure 11 Gate Charge

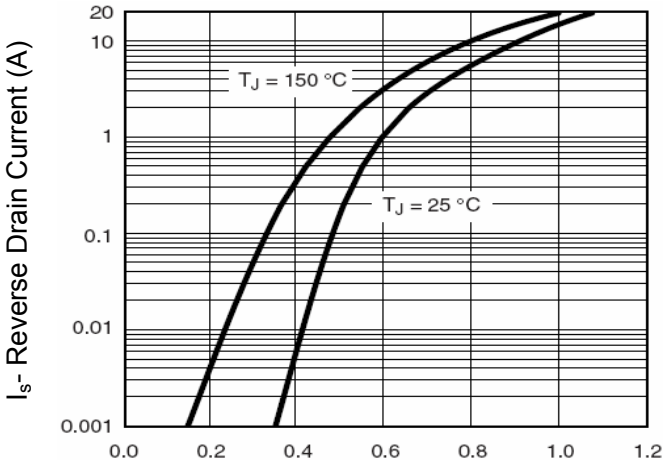


Figure 12 Source- Drain Diode Forward

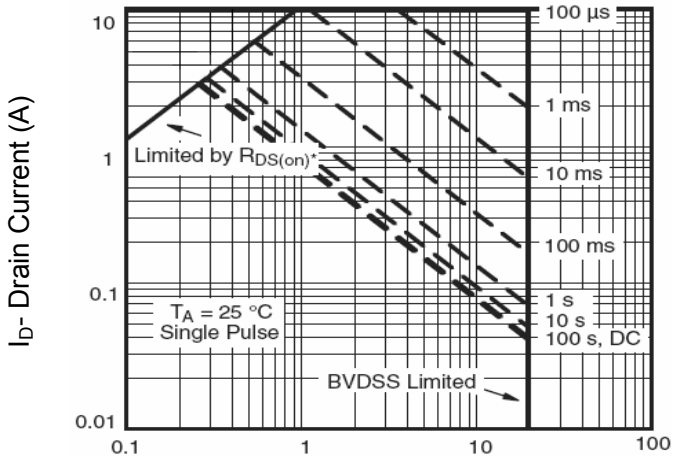


Figure 13 Safe Operation Area

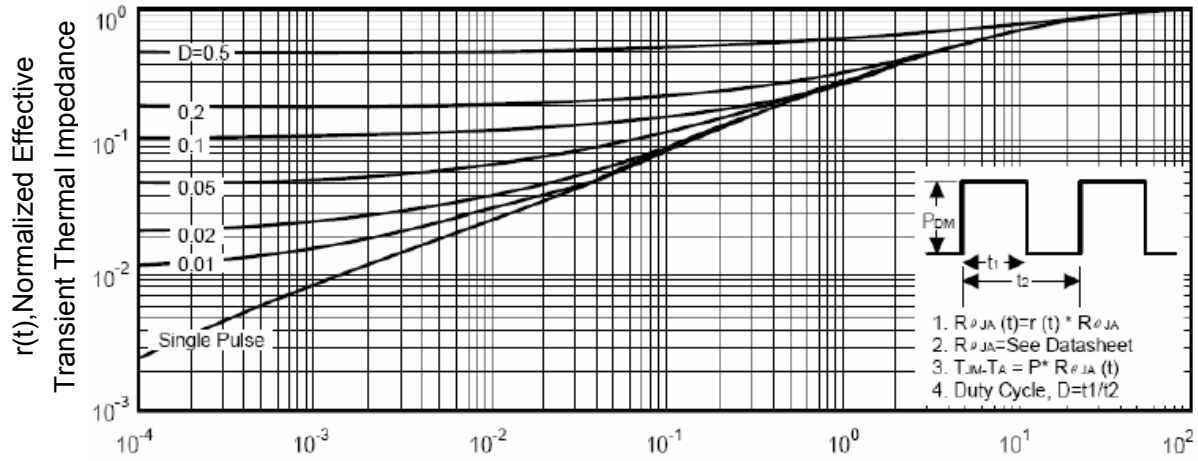


Figure 14 Normalized Maximum Transient Thermal Impedance

P- Channel Typical Electrical and Thermal Characteristics (Curves)

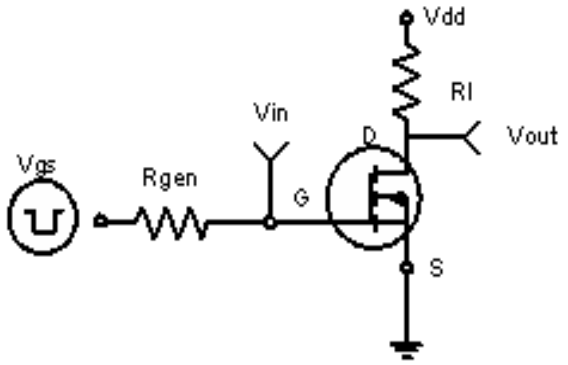


Figure 1:Switching Test Circuit

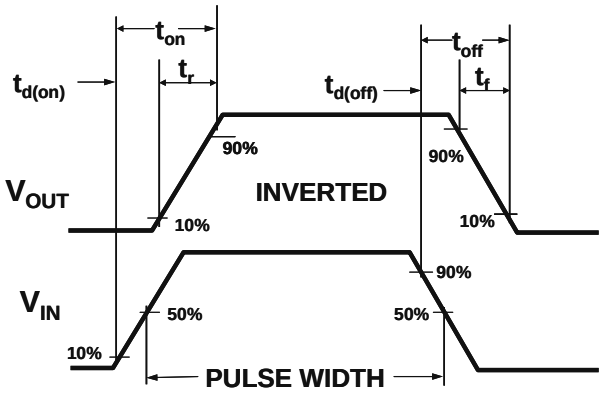


Figure 2:Switching Waveforms

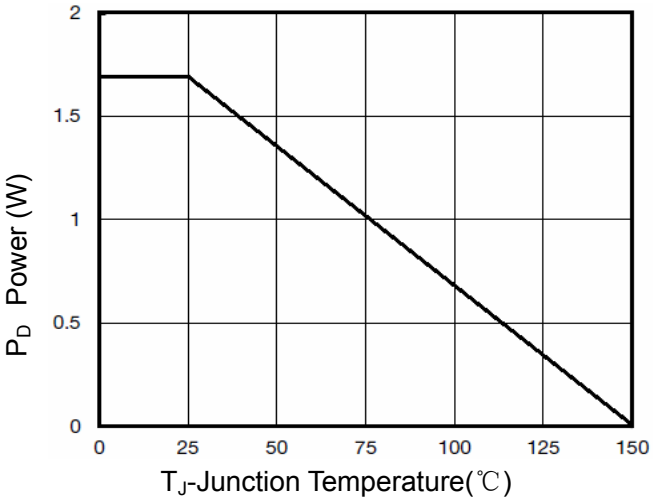


Figure 3 Power Dissipation

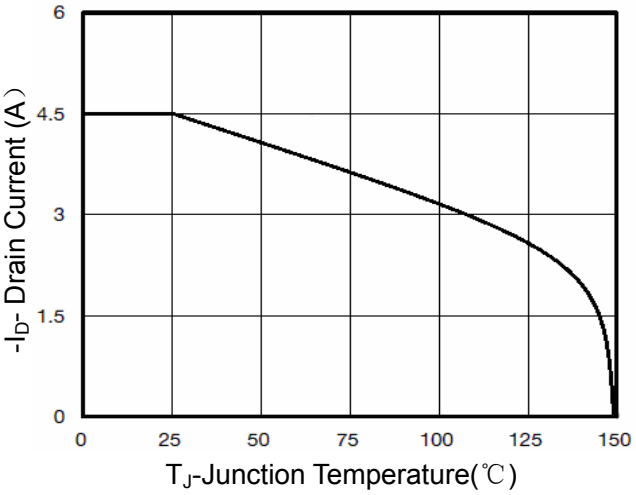


Figure 4 Drain Current

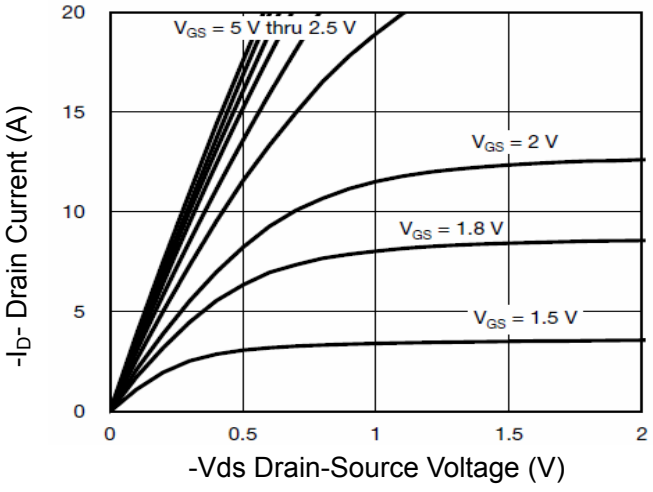


Figure 5 Output Characteristics

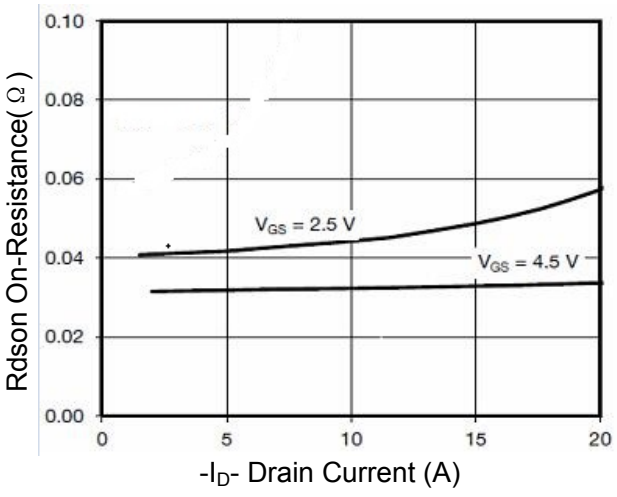


Figure 6 Drain-Source On-Resistance

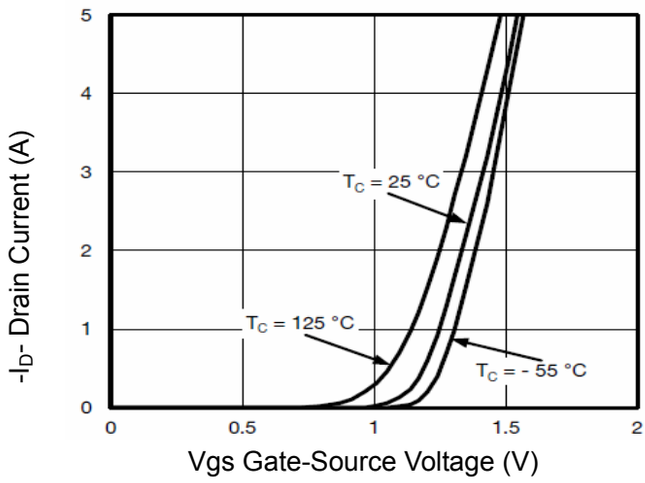


Figure 7 Transfer Characteristics

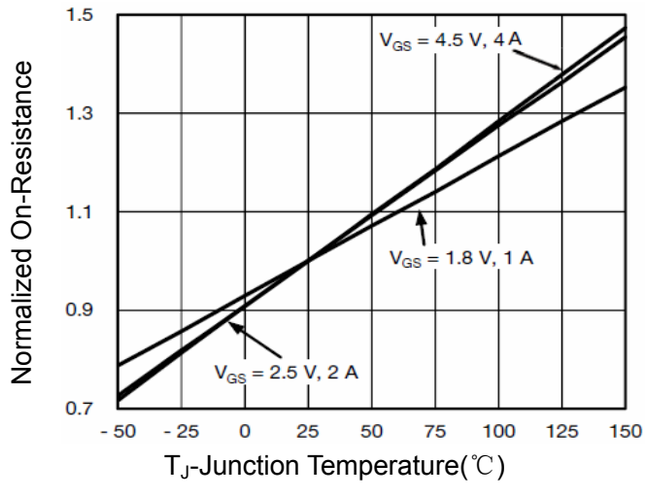


Figure 8 Drain-Source On-Resistance

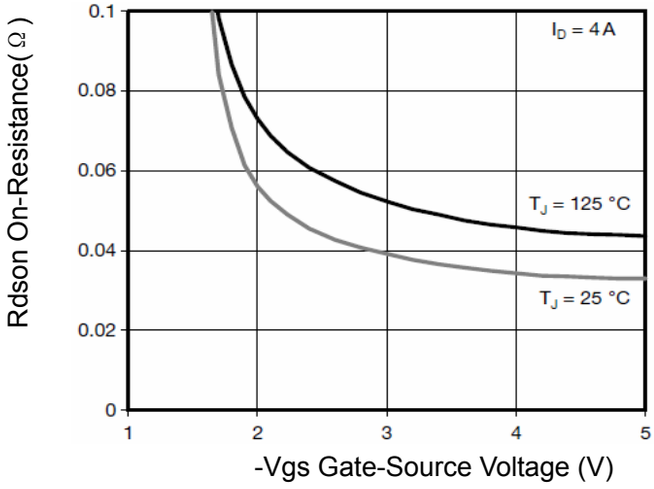


Figure 9 Rdson vs Vgs

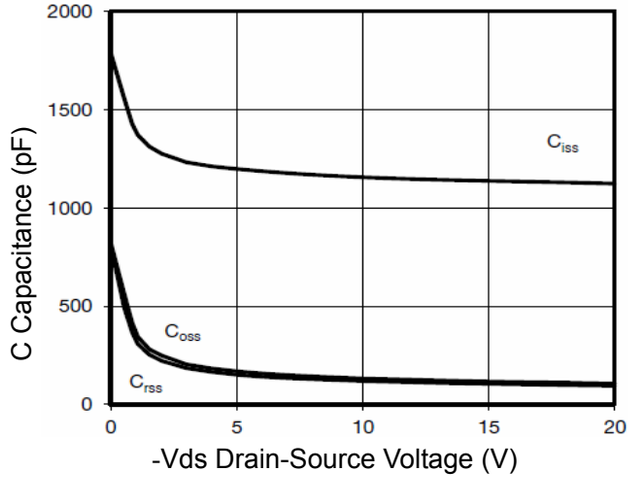


Figure 10 Capacitance vs Vds

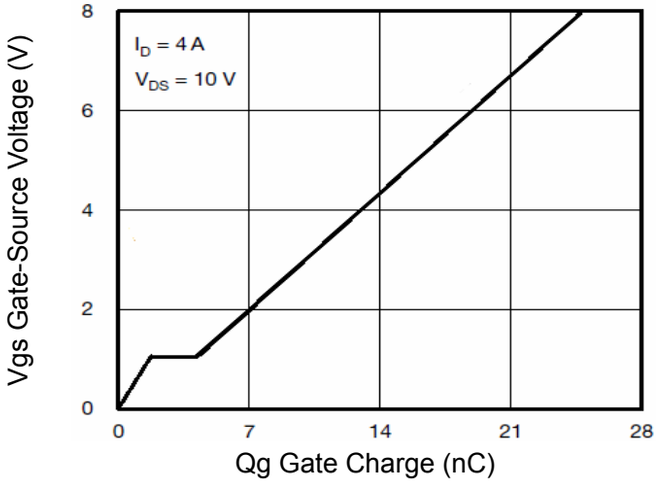


Figure 11 Gate Charge

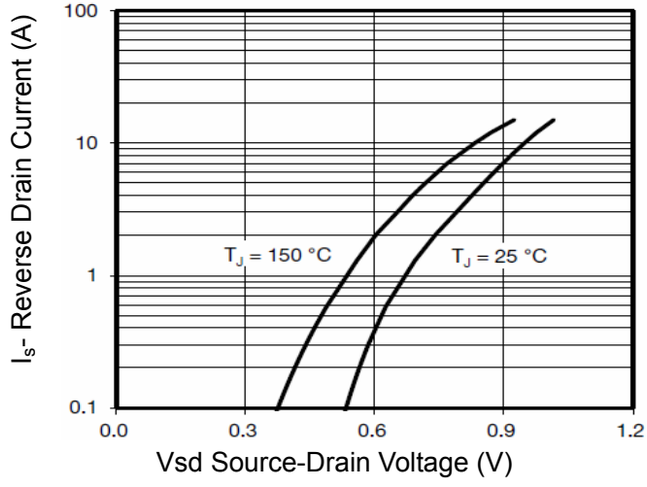


Figure 12 Source- Drain Diode Forward

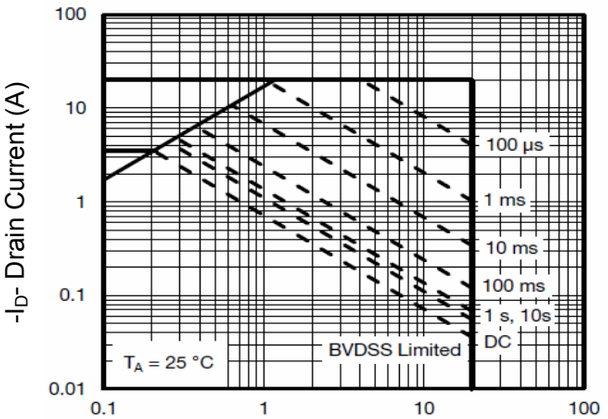


Figure 13 Safe Operation Area

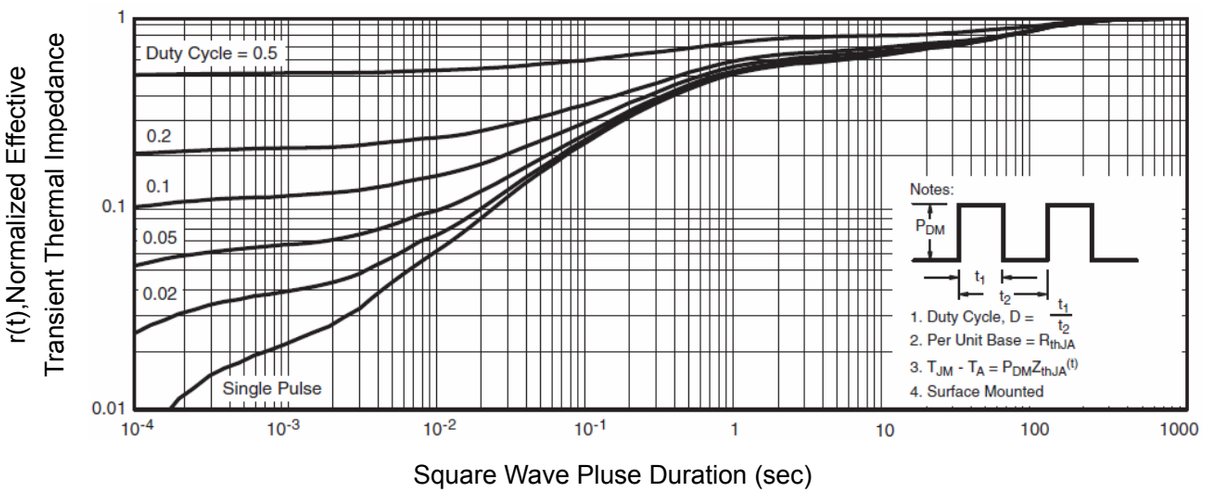


Figure 14 Normalized Maximum Transient Thermal Impedance

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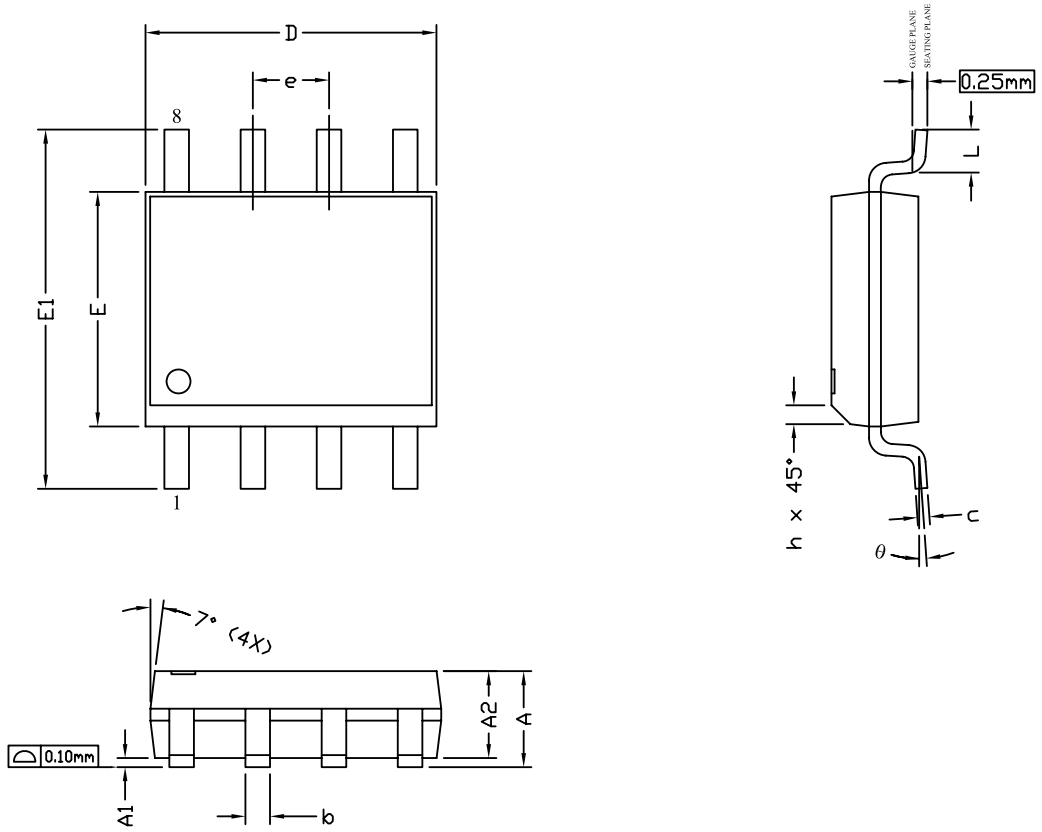
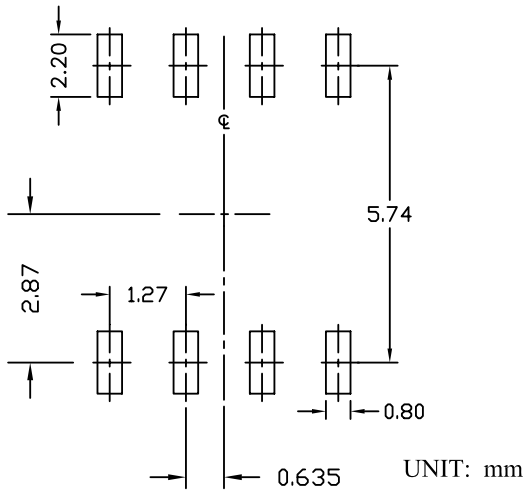
SO8 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.65	1.75	0.053	0.065	0.069
A1	0.10	----	0.25	0.004	----	0.010
A2	1.25	1.50	1.65	0.049	0.059	0.065
b	0.31	----	0.51	0.012	----	0.020
c	0.17	----	0.25	0.007	----	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	3.80	3.90	4.00	0.150	0.154	0.157
e	1.27 BSC			0.050 BSC		
E1	5.80	6.00	6.20	0.228	0.236	0.244
h	0.25	----	0.50	0.010	----	0.020
L	0.40	----	1.27	0.016	----	0.050
θ	0°	----	8°	0°	----	8°

NOTE
1. ALL DIMENSIONS ARE IN MILLMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
4. DIMENSION L IS MEASURED IN GAUGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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