BURST CellularRAM™

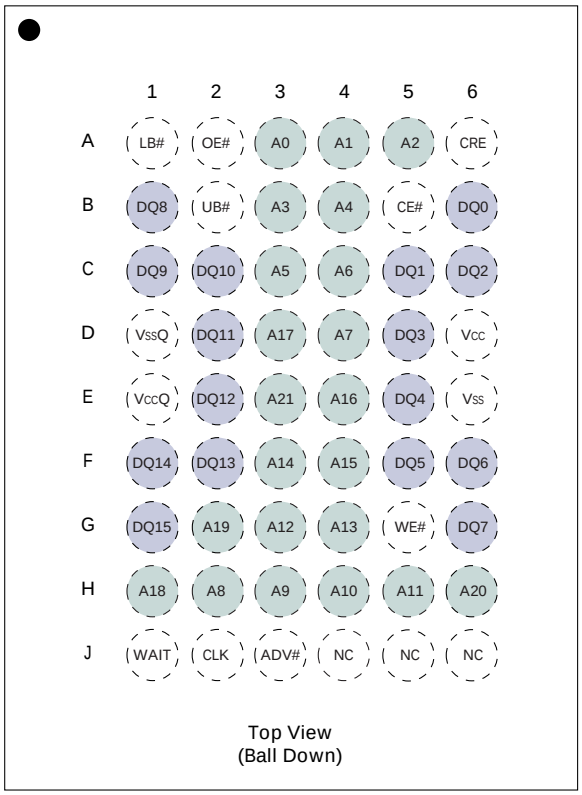
MT45W4MW16BFB
MT45W2MW16BFB

For the latest data sheet, please refer to Micron's Web site: www.micron.com/datasheets.

Features

- Single device supports asynchronous, page, and burst operations
- VCC, VCCQ Voltages
  1.70V–1.95V VCC
  1.70V–2.25V VCCQ (Option W)
- Random Access Time: 70ns
- Burst Mode Write Access
  Continuous burst
- Burst Mode Read Access
  4, 8, or 16 words, or continuous burst
  MAX clock rate: 104 MHz (^{t}CLK = 9.62ns)
  Burst initial latency: 39ns (4 clocks) @ 104 MHz
  ^{t}ACLK: 6.5ns @ 104 MHz
- Page Mode Read Access
  Sixteen-word page size
  Interpage read access: 70ns
  Intrapage read access: 20ns
- Low Power Consumption
  Asynchronous READ < 25mA
  Intrapage READ < 15mA
  Initial access, burst READ: (39ns [4 clocks] @ 104 MHz) < 35mA
  Continuous burst READ < 15mA
  Standby: 90µA (32Mb), 100µA (64Mb)
  Deep power-down < 10µA
- Low-Power Features
  Temperature Compensated Refresh (TCR)
  Partial Array Refresh (PAR)
  Deep Power-Down (DPD) Mode

Figure 1: Ball Assignment 54-Ball FBGA



NOTE:
See Table 1 on page 6 for ball descriptions, and Figure 40 on page 50 for 54-ball mechanical drawing.

Options	**Marking**
• VCC Core Voltage Supply:	
1.80V – MT45**W**xMx16BFB	W
• VCCQ I/O Voltage	
3.0V – MT45WxM**L**16BFB	(contact factory)
2.5V – MT45WxM**V**16BFB	(contact factory)
1.8V – MT45WxM**W**16BFB	W
• Timing	
60ns access	(contact factory)
70ns access	-70
85ns access	-85
• Frequency	
66 MHz	1
104 MHz	6

Options (continued)	**Marking**
• Configuration:	
4 Meg x 16	MT45W4Mx16BFB
2 Meg x 16	MT45W2Mx16BFB
• Package	
54-ball FBGA	FB
• Operating Temperature Range	
Wireless (-25°C to +85°C)	WT
Industrial (-40°C to +85°C)	IT (contact factory)

NOTE: A part marking guide for the FBGA devices can be found on Micron's Web site: www.micron.com/numberguide

Part Number Example:
MT45W2MW16BFB-701WT

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General Description

Micron® CellularRAM™ products are high-speed, CMOS dynamic random access memories developed for low-power, portable applications. The MT45W4MW16BFB is a 64Mb device organized as 4 Meg x 16 bits; the MT45W2MW16BFB is a 32Mb device organized as 2 Meg x 16 bits. These devices include an industry-standard burst mode Flash interface that dramatically increases read/write bandwidth compared with other low-power SRAM or Pseudo SRAM offerings.

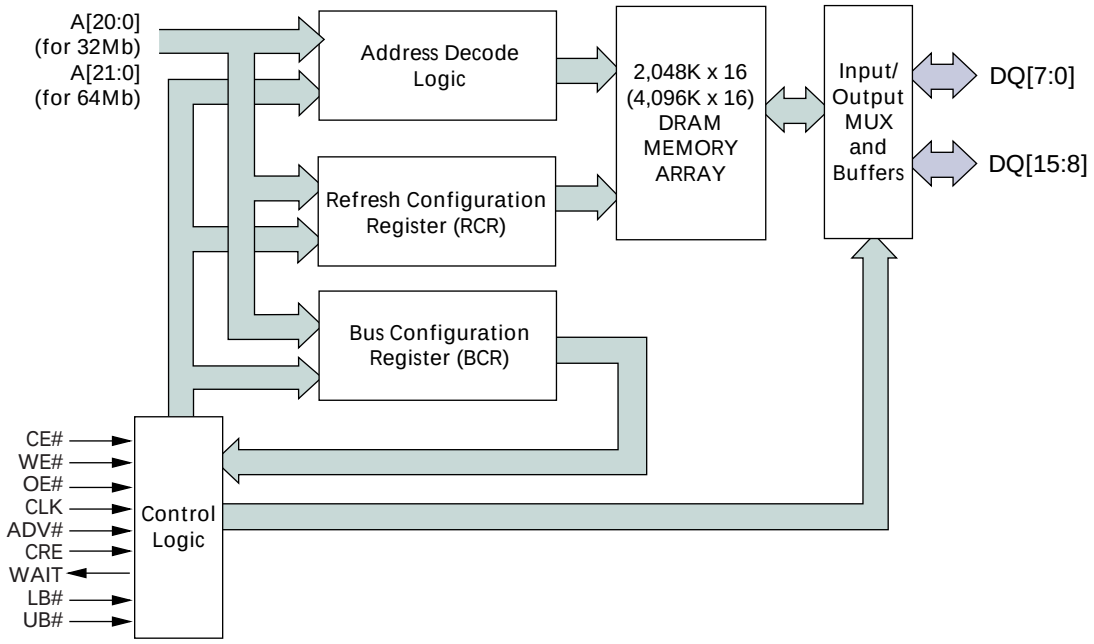
To operate seamlessly on a burst Flash bus, CellularRAM products have incorporated a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices.

The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

Special attention has been focused on standby current consumption during self refresh. CellularRAM products include three system-accessible mechanisms used to minimize standby current. Partial array refresh (PAR) limits refresh to only that part of the DRAM array that contains essential data. Temperature compensated refresh (TCR) is used to adjust the refresh rate according to the case temperature. The refresh rate can be decreased at lower temperatures to minimize current consumption during standby. Deep power-down (DPD) halts the refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are adjusted through the RCR.

Figure 2: Functional Block Diagram – 4 Meg x 16 and 2 Meg x 16



NOTE:

Functional block diagrams illustrate simplified device operation. See truth table, ball descriptions, and timing diagrams for detailed information.

Table 1: FBGA Ball Descriptions

FBGA ASSIGNMENT	SYMBOL	TYPE	DESCRIPTION
A3, A4, A5, B3, B4, C3, C4, D4, H2, H3, H4, H5, G3, G4, F3, F4, E4, D3, H1, G2, H6, E3	A[21:0]	Input	Address Inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the bus configuration register or the refresh configuration register. On the 32Mb device, A21 (ball E3) is not internally connected.
J2	CLK	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising (or falling, depending upon the bus configuration register setting) CLK edge when ADV# is active, or upon a rising ADV# edge, whichever occurs first. CLK is static during asynchronous access READ and WRITE operations and during PAGE READ ACCESS operations. CLK must be held LOW during asynchronous or page mode transactions.
J3	ADV#	Input	Address Valid: Indicates that a valid address is present on the address inputs. Addresses can be latched on the rising edge of ADV# during READ and WRITE operations. ADV# may be driven LOW during asynchronous READ and WRITE operations.
A6	CRE	Input	Configuration Register Enable: When CRE is HIGH, WRITE operations load the refresh configuration register or bus configuration register.
B5	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby or deep power-down mode.
A2	OE#	Input	Output Enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
G5	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
A1	LB#	Input	Lower Byte Enable. DQ[7:0]
B2	UB#	Input	Upper Byte Enable. DQ[15:8]
B6, C5, C6, D5, E5, F5, F6, G6, B1, C1, C2, D2, E2, F2, F1, G1	DQ[15:0]	Input/ Output	Data Inputs/Outputs.
J1	WAIT	Output	Wait: Provides data-valid feedback during burst READ and WRITE operations. The signal is gated by CE#. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is asserted when a burst crosses a row boundary. WAIT is also used to mask the delay associated with opening a new internal page. WAIT is asserted and should be ignored during asynchronous and page mode operations.
J4, J5, J6	NC	–	Not internally connected.
D6	V_{CC}	Supply	Device Power Supply: (1.70V–1.95V) Power supply for device core operation.
E1	V_{CCQ}	Supply	I/O Power Supply: (1.70V–1.95V) Power supply for input/output buffers.
E6	V_{SS}	Supply	V_{SS} must be connected to ground.
D1	V_{SSQ}	Supply	V_{SSQ} must be connected to ground.

NOTE:

The CLK and ADV# inputs can be tied to V_{SS} if the device is always operating in asynchronous or page mode. The WAIT signal will be driven to an undefined state when operating in asynchronous or page mode. Otherwise, during asynchronous operation, WAIT will be in a High-Z condition.

Table 2: Bus Operations – Asynchronous Mode

MODE	POWER	CLK	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[1]	DQ[15:0][2]	NOTES
Read	Active > Standby	L	L	L	L	H	L	L1	L	Data-Out	3
Write	Active > Standby	L	L	L	X	L	L	L1	L	Data-In	3
Standby	Standby	X	X	H	X	X	L	X	X	High-Z	4
Standby	Standby	X	X	L	X	X	L	X	X	X	3, 5
Configuration Register	Active	L	L	L	H	L	H	X	L	High-Z	
DPD	Deep Power-Down	L	X	H	X	X	X	X	X	High-Z	6

Table 3: Bus Operations – Burst Mode

MODE	POWER	CLK	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT[1]	DQ[15:0][2]	NOTES
Async Read	Active > Standby	L	L	L	L	H	L	L	L	Data-Out	2, 3
Async Write	Active > Standby	L	L	L	X	L	L	L	L	Data-In	2, 3
Standby	Standby	X	X	H	X	X	L	X	X	High-Z	4
Standby	Standby	X	X	L	X	X	L	X	X	X	3, 5
Initial Burst Read	Active > Standby		L	L	X	H	L	L	L	Data-Out	2, 3, 7, 8
Initial Burst Write	Active > Standby		L	L	H	L	L	X	L	Data-In	3, 7, 8
Burst Continue	Active > Standby		H	L	X	X	L	X	X	Data-In or Data-Out	3, 7, 8
Burst Suspend	Active > Standby	L	X	L	X	X	L	X	X	High-Z	3, 7
Configuration Register	Active		L	L	H	L	H	X	X	High-Z	7, 8
DPD	Deep Power-Down	L	X	H	X	X	X	X	X	High-Z	6

NOTE:

1. When LB# and UB# are in select mode (LOW), DQ[15:0] are affected. When only LB# is in select mode, DQ[7:0] are affected. When only UB# is in the select mode, DQ[15:8] are affected.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. The device will consume active power in this mode whenever addresses are changed.
4. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
5. V_{IN} = V_{CC} or 0V; all device balls must be static (unswitched) in order to achieve standby current.
6. DPD is maintained until RCR is reconfigured.
7. Burst mode operation is initialized through the bus configuration register (BCR[15]).
8. The clock polarity is configured through the bus configuration register (BCR[6]).

Table 4: Abbreviated Component Marks – CellularRAM FBGA-Packaged Components

PART NUMBER	ENGINEERING SAMPLE	QUALIFIED SAMPLE
MT45W4MW16BFB-701 WT	PX344	PW344
MT45W4MW16BFB-706 WT	PX340	PW340
MT45W4MW16BFB-856 WT	PX345	PW345
MT45W2MW16BFB-701 WT	PX244	PW244
MT45W2MW16BFB-706 WT	PX240	PW240
MT45W2MW16BFB-856 WT	PX245	PW245
MT45W4MW16BFB-706 IT	PX352[1]	PW352[1]
MT45W4MW16BFB-856 IT	PX354[1]	PW354[1]
MT45W4ML16BFB-856 IT	PX355[1]	PW355[1]
MT45W4ML16BFB-706 IT	PX357[1]	PW357[1]
MT45W2MW16BFB-706 IT	PX248[1]	PW248[1]
MT45W2MW16BFB-856 IT	PX250[1]	PW250[1]
MT45W2ML16BFB-856 IT	PX251[1]	PW251[1]
MT45W2ML16BFB-706 IT	PX253[1]	PW253[1]

NOTE:

1. Contact factory for availability.

Functional Description

In general, the MT45W4MW16BFB device and the MT45W2MW16BFB device are high-density alternatives to SRAM and Pseudo SRAM products, popular in low-power, portable applications.

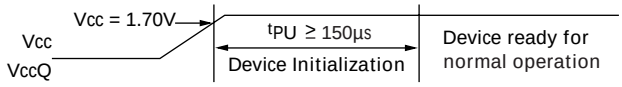
The MT45W4MW16BFB device contains 67,108,864 bits organized as 4,194,304 addresses by 16 bits. The MT45W2MW16BFB contains 33,554,432 bits organized as 2,097,152 addresses by 16 bits. Both devices implement the same high-speed bus interface found on burst mode Flash products.

The CellularRAM bus interface supports both asynchronous and burst mode transfers. Page mode accesses are also included as a bandwidth-enhancing extension to the asynchronous read protocol.

Power-Up Initialization

CellularRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings (see Table 5 on page 16 and Table 8 on page 21). VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.70V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

Figure 3: Power-Up Initialization Timing



Bus Operating Modes

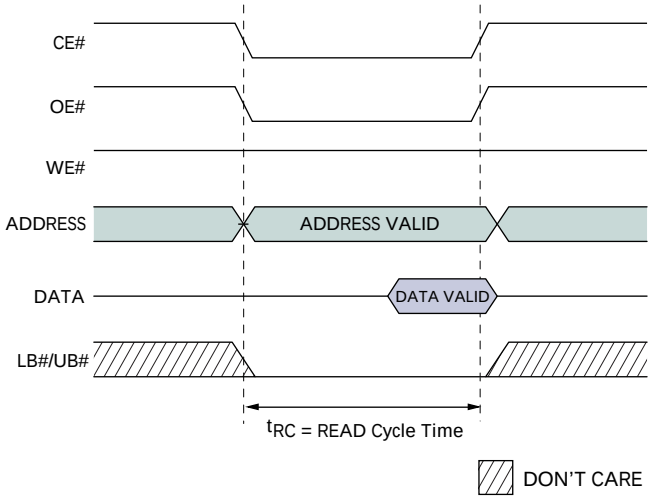
The MT45W4MW16BFB and MT45W2MW16BFB CellularRAM products incorporate a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, page mode, and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the bus configuration register. Page mode is controlled by the refresh configuration register (RCR[7]).

Asynchronous Mode

CellularRAM products power up in the asynchronous operating mode. This mode uses the industry-standard SRAM control bus (CE#, OE#, WE#, LB#/UB#). READ operations (Figure 4) are initiated by bringing CE#, OE#, and LB#/UB# LOW while keeping WE# HIGH. Valid data will be driven out of the I/Os after the specified access time has elapsed. WRITE operations (Figure 5) occur when CE#, WE#, and LB#/UB# are driven LOW. During asynchronous WRITE operations, the OE# level is a "Don't Care," and WE# will override OE#. The data to be written is latched on the rising edge of CE#, WE#, or LB#/UB# (whichever occurs first). Asynchronous operations (page mode disabled) can either use the ADV input to latch the address, or ADV can be driven LOW during the entire READ/WRITE operation.

During asynchronous operation, the CLK input should be held LOW. WAIT will be driven while the device is enabled and its state should be ignored.

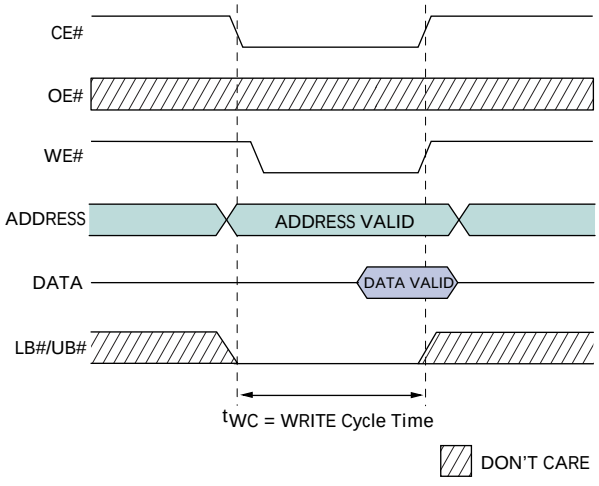
Figure 4: READ Operation (ADV = LOW)



NOTE:

ADV must remain LOW for page mode operation.

Figure 5: WRITE Operation (ADV = LOW)

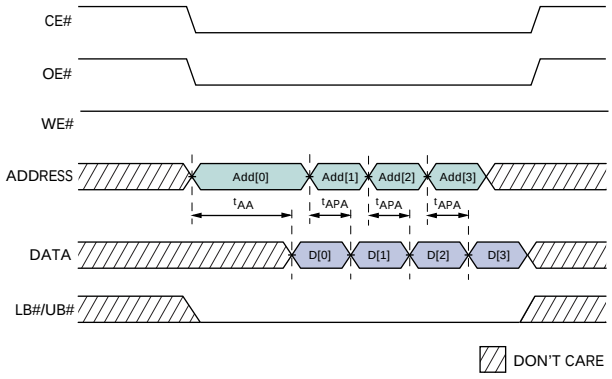


Page Mode READ Operation

Page mode is a performance-enhancing extension to the legacy asynchronous READ operation. In page-mode-capable products, an initial asynchronous read access is performed, then adjacent addresses can be read quickly by simply changing the low-order address. Addresses A[3:0] are used to determine the members of the 16-address CellularRAM page. Addresses A[4] and higher must remain fixed during the entire page mode access. Figure 6 shows the timing for a page mode access. Page mode takes advantage of the fact that adjacent addresses can be read in a shorter period of time than random addresses. WRITE operations do not include comparable page mode functionality.

During asynchronous page mode operation, the CLK input must be held LOW. CE# must be driven HIGH upon completion of a page mode access. WAIT will be driven while the device is enabled and its state should be ignored. Page mode is enabled by setting RCR[7] to HIGH. WRITE operations do not include comparable page mode functionality. ADV must be driven LOW during all page mode read accesses.

Figure 6: Page Mode READ Operation (ADV = LOW)



Burst Mode Operation

Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multiclock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the next rising edge of CLK or ADV# (whichever occurs first). During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH, Figure 7 on page 11) or WRITE (WE# = LOW, Figure 8 on page 11).

The size of a burst can be specified in the BCR as either a fixed length or continuous. Fixed-length bursts consist of four, eight, or sixteen words. Continuous bursts have the ability to start at a specified address and burst through the entire memory. The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and CellularRAM device.

The WAIT output will be asserted as soon as a burst is initiated, and will be de-asserted to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted if the burst crosses a row boundary. Once the CellularRAM device has restored the previous row's data and accessed the next row, WAIT will be de-asserted and the burst can continue (see Figure 28 on page 38).

Figure 7: Burst Mode READ (4-word burst)[1]

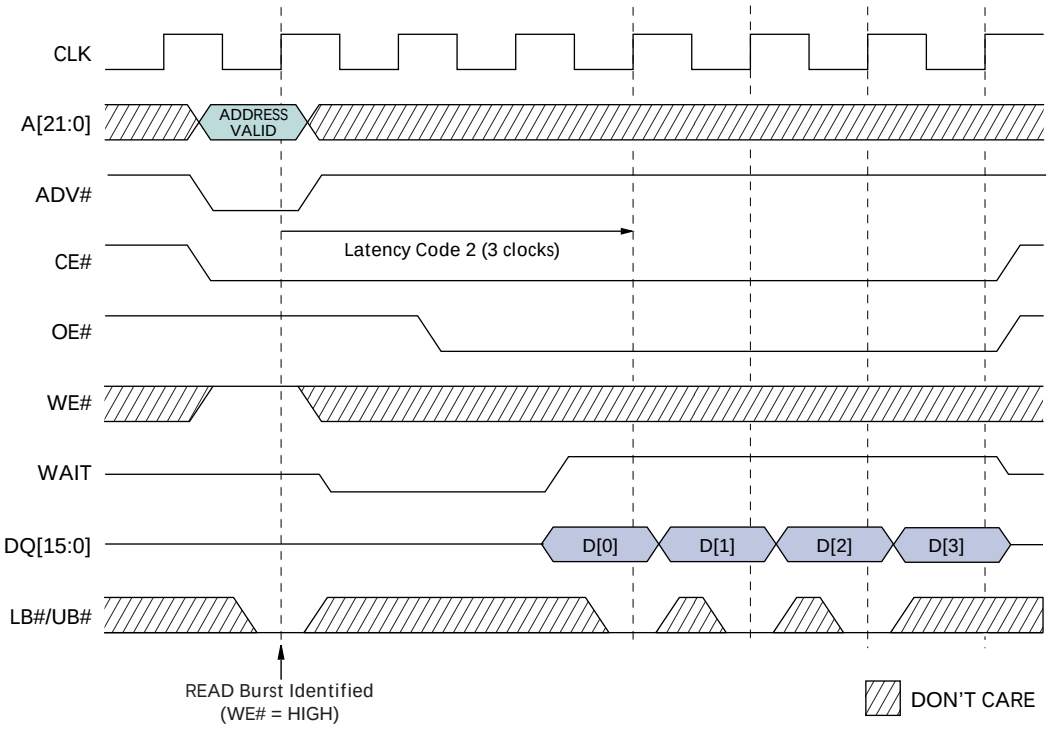
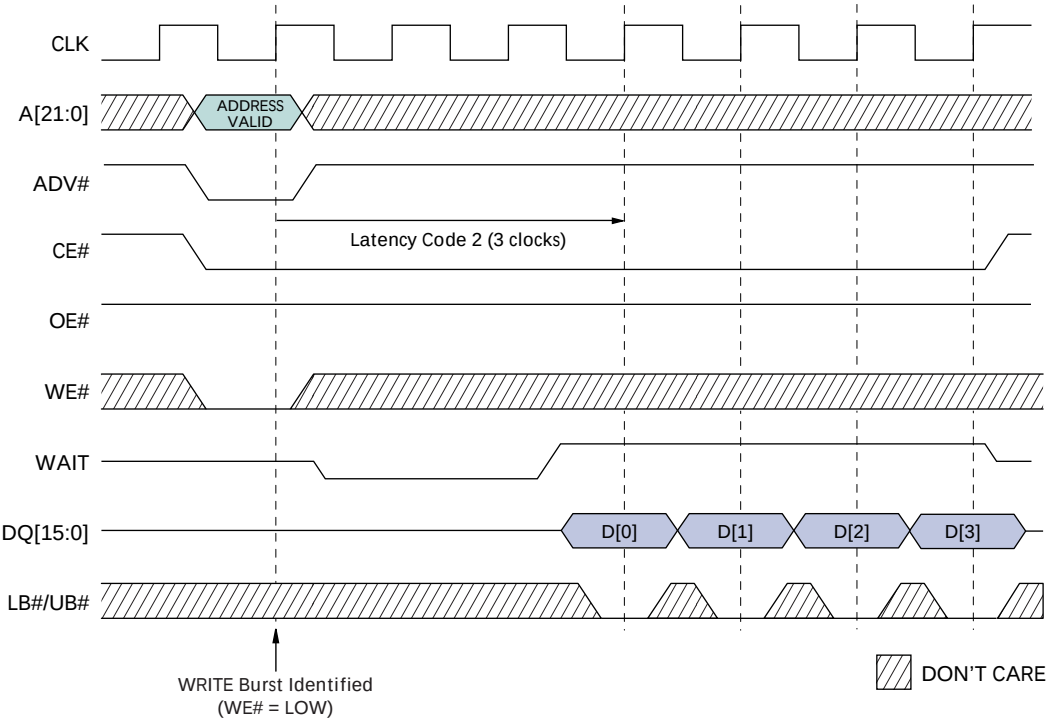


Figure 8: Burst Mode WRITE (4-word burst)[1]



NOTE:

1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; Hold data one clock; WAIT asserted during delay.

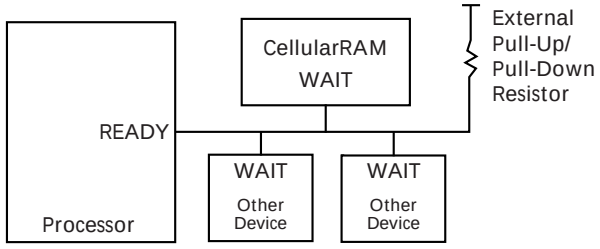
Mixed-Mode Operation

The device can support a combination of synchronous READ and asynchronous WRITE operations when the BCR is configured for synchronous operation. The asynchronous WRITE operation requires that the clock (CLK) remain LOW during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire WRITE operation. CE# must return HIGH when transitioning between mixed-mode operations. Note that the ^{t}CKA period is the same as a READ or WRITE cycle. This time is required to ensure adequate refresh. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers. See Figure 36 on page 46 for the "Asynchronous WRITE Followed by Burst READ" timing diagram.

Wait Operation

WAIT output on the CellularRAM device is typically connected to a shared, system-level WAIT signal (see Figure 9 below). The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

Figure 9: Wired or WAIT Configuration



Once a READ or WRITE operation has been initiated, WAIT goes active to indicate that the CellularRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the CellularRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

CE# must remain asserted at least as long as WAIT is asserted. Bringing CE# HIGH while WAIT is asserted may cause data corruption.

WAIT output also performs an arbitration role when a READ or WRITE operation is launched while an on-chip refresh is in progress. If a collision occurs, WAIT pin be asserted for additional clock cycles, until the refresh has completed (see Figures 10 and 11 on page 13). When the refresh operation has completed, the READ or WRITE operation will continue normally.

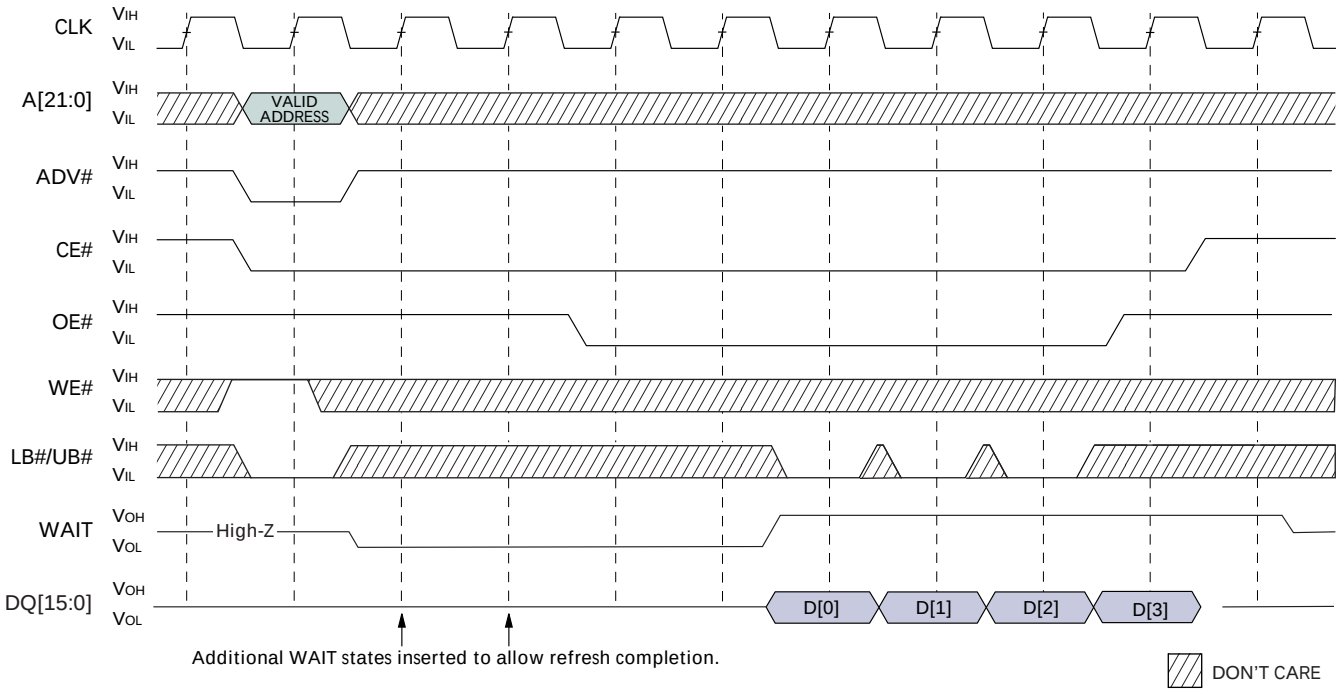
WAIT is also asserted when a continuous READ or WRITE burst crosses a row boundary. The WAIT assertion allows time for the new row to be accessed, and permits any pending refresh operations to be performed.

LB#/UB# Operation

The LB# enable and UB# enable signals support byte-wide data transfers. During READ operations, the enabled byte(s) are driven onto the DQs. The DQs associated with a disabled byte are put into a High-Z state during a READ operation. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

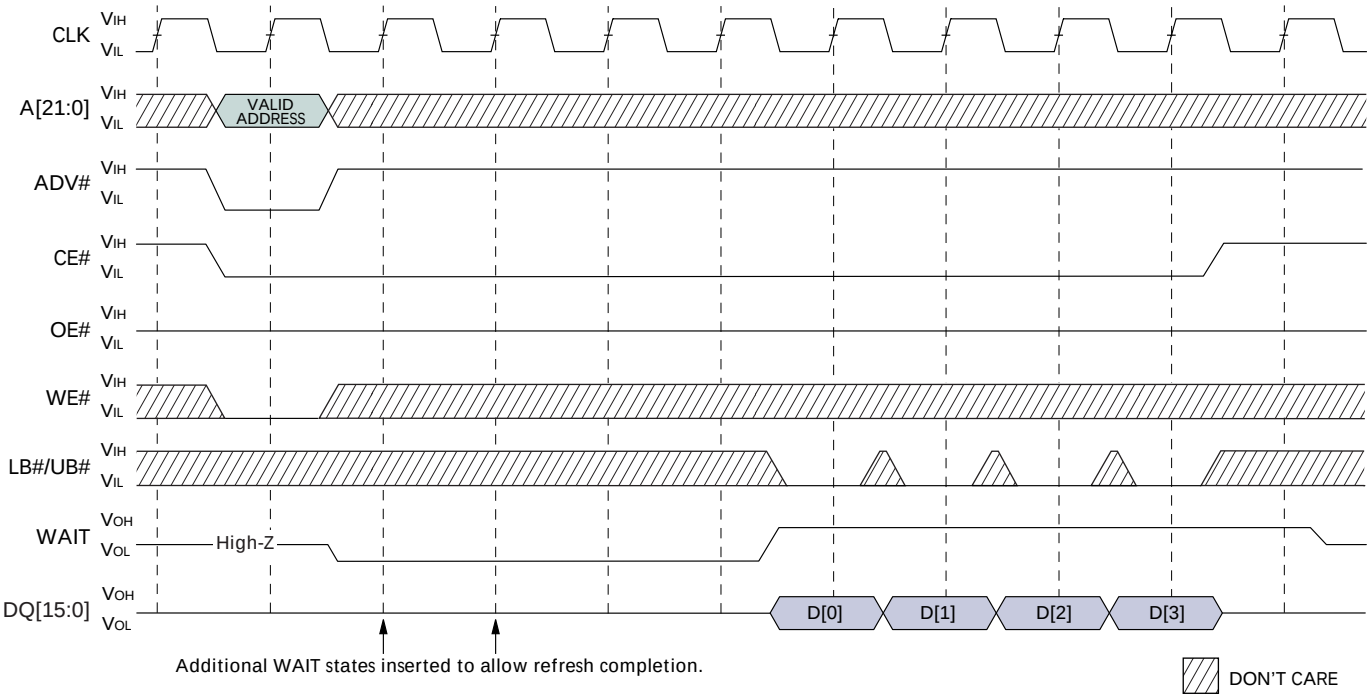
Figure 10: Refresh Collision During READ Operation[1]



NOTE:

1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; Hold Data one clock; WAIT asserted during delay.

Figure 11: Refresh Collision During WRITE Operation[1]



NOTE:

1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; Hold data one clock; WAIT asserted during delay.

Low-Power Operation

Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH and there are no transactions in progress.

The device will enter standby operation upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This "active" standby mode will continue until a change occurs to the address or control inputs.

Temperature Compensated Refresh

Temperature compensated refresh (TCR) is used to adjust the refresh rate depending on the device operating temperature. DRAM technology requires increasingly frequent refresh operations to maintain data integrity as temperatures increase. More frequent refresh is required due to increased leakage of the DRAM capacitive storage elements as temperatures rise. A decreased refresh rate at lower temperatures will facilitate a savings in standby current.

TCR allows for adequate refresh at four different temperature thresholds (+15°C, +45°C, +70°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +50°C, the system can minimize self refresh current consumption by selecting the +70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

Partial Array Refresh

Partial array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, three-quarters array, one-half array, one-quarter array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Tables 9 and 10 on page 21). READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted.

Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

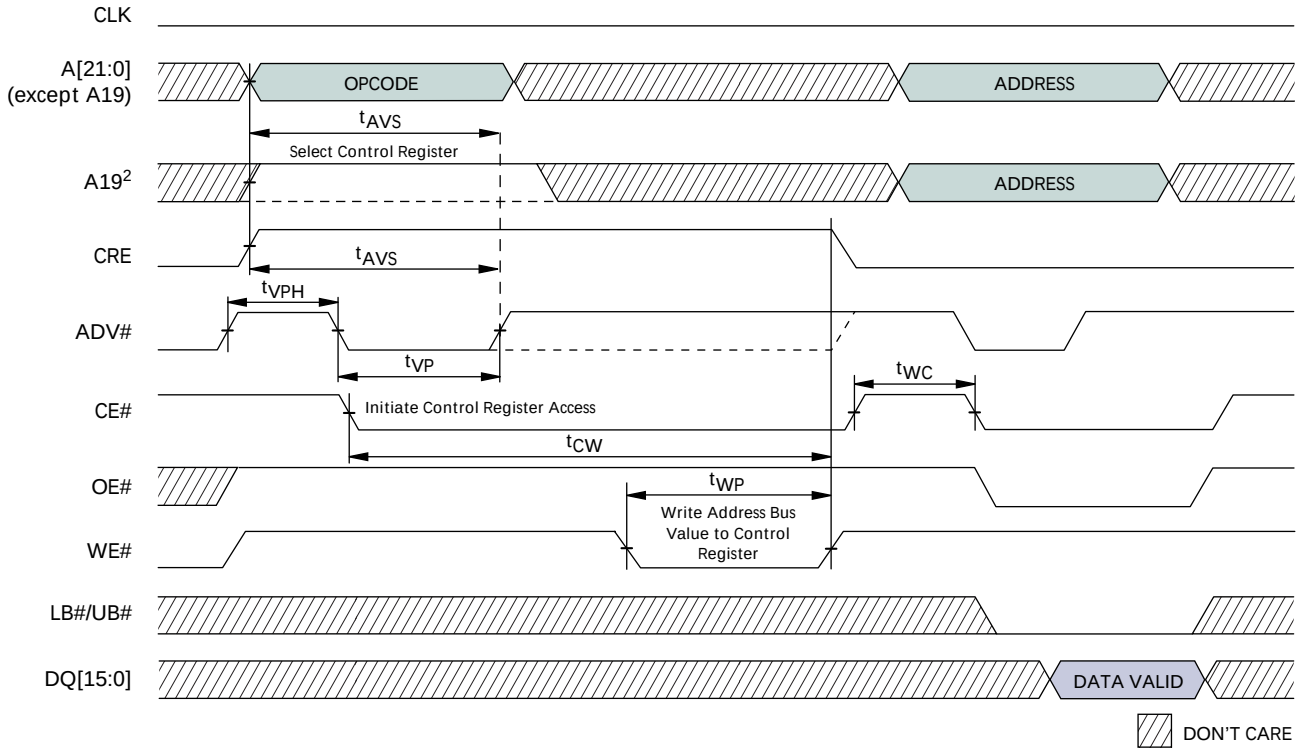
Configuration Registers

Two WRITE-only, user-accessible configuration registers have been included to define device operation. The bus configuration register (BCR) defines how the CellularRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

Bus Configuration Register

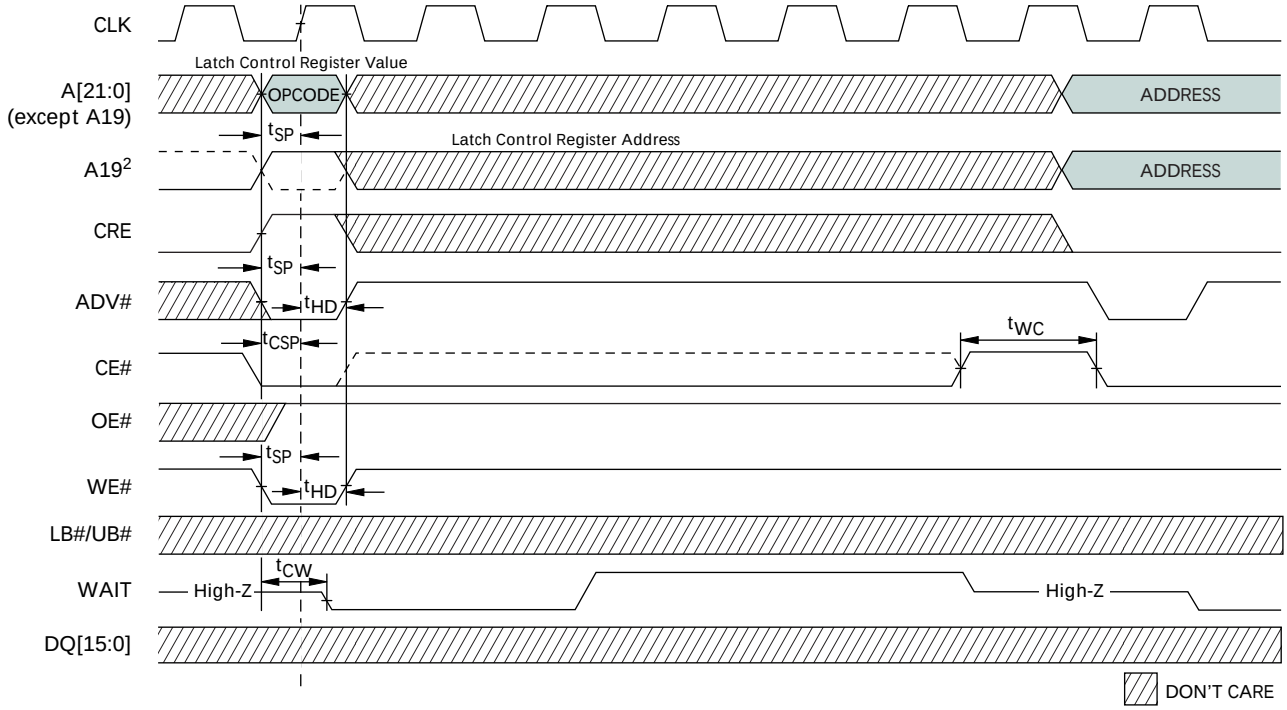
The BCR defines how the CellularRAM device interacts with the system memory bus. Page mode operation is enabled by a bit contained in the RCR. The BCR is loaded using either a synchronous or an asynchronous WRITE operation when A[19] is HIGH and the configuration register enable (CRE) input is also HIGH (see Figures 12 and 13 on page 15). When CRE is LOW, a READ or WRITE operation will access the memory array. The values placed on address pins A[21:0] are latched into the BCR on the rising edge of ADV#, CE#, or WE#, whichever occurs first. LB# and UB# are "Don't Care." Table 5 on page 16 describes the control bits in the BCR. At power-up, the BCR is set to 9F4Fh.

Figure 12: Configuration Register WRITE in Asynchronous Mode Followed by READ



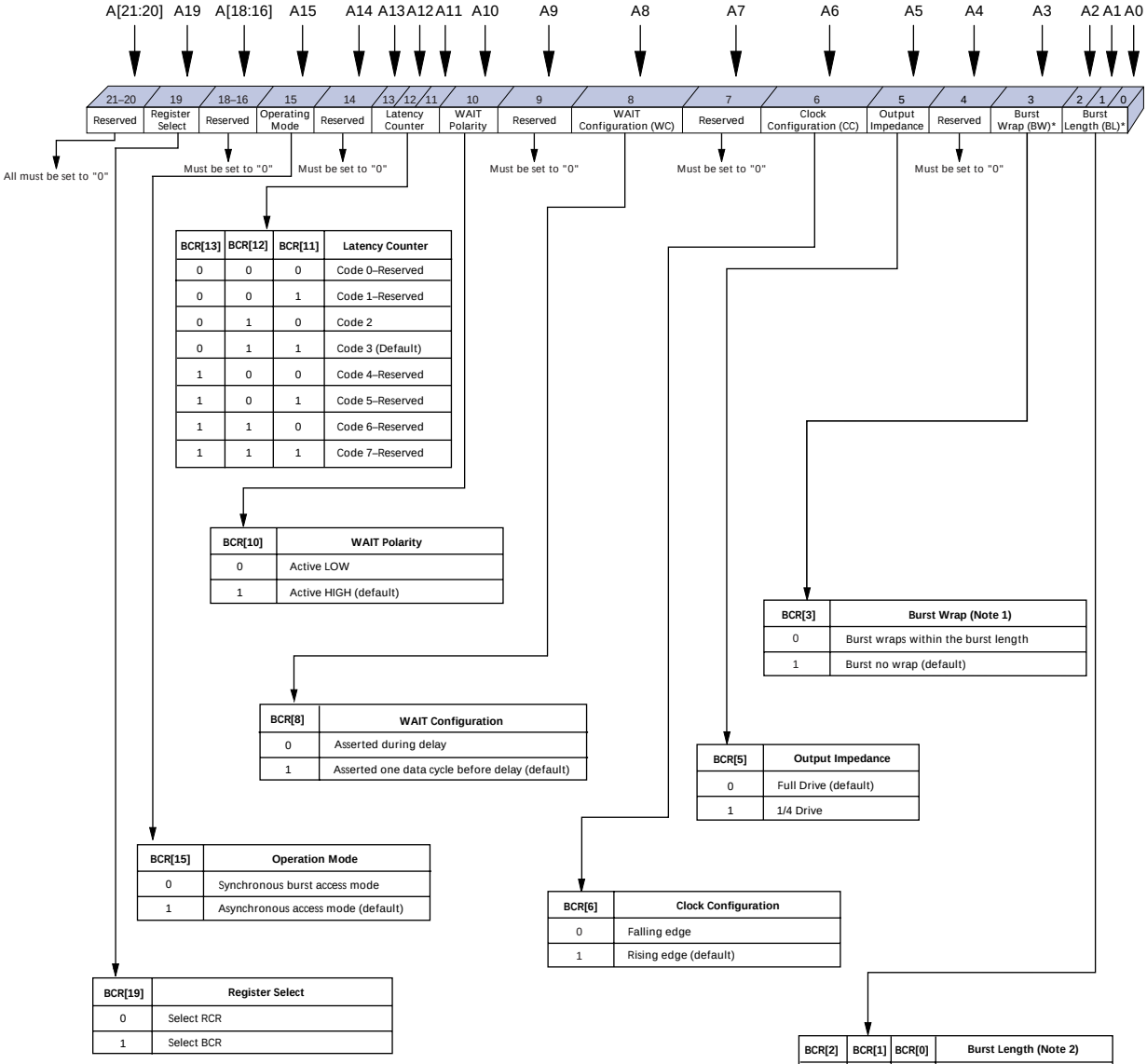
NOTE: 1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; Hold data one clock; WAIT asserted during delay.
2. A[19] = LOW to load RCR; A[19] = HIGH to load BCR.

Figure 13: Configuration Register WRITE in Synchronous Mode Followed by READ[1]



NOTE: 1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; Hold data one clock; WAIT asserted during delay.
2. A[19] = LOW to load RCR; A[19] = HIGH to load BCR.

Table 5: Bus Configuration Register Definition



BCR[13]	BCR[12]	BCR[11]	Latency Counter
0	0	0	Code 0–Reserved
0	0	1	Code 1–Reserved
0	1	0	Code 2
0	1	1	Code 3 (Default)
1	0	0	Code 4–Reserved
1	0	1	Code 5–Reserved
1	1	0	Code 6–Reserved
1	1	1	Code 7–Reserved

BCR[10]	WAIT Polarity
0	Active LOW
1	Active HIGH (default)

BCR[3]	Burst Wrap (Note 1)
0	Burst wraps within the burst length
1	Burst no wrap (default)

BCR[8]	WAIT Configuration
0	Asserted during delay
1	Asserted one data cycle before delay (default)

BCR[5]	Output Impedance
0	Full Drive (default)
1	1/4 Drive

BCR[15]	Operation Mode
0	Synchronous burst access mode
1	Asynchronous access mode (default)

BCR[6]	Clock Configuration
0	Falling edge
1	Rising edge (default)

BCR[19]	Register Select
0	Select RCR
1	Select BCR

BCR[2]	BCR[1]	BCR[0]	Burst Length (Note 2)
0	0	1	4 words
0	1	0	8 words
0	1	1	16 words
1	1	1	Continuous burst (default)

NOTE:

1. All burst WRITEs are continuous.

Table 6: Sequence and Burst Length

STARTING ADDRESS	WRAP	NO WRAP	4-WORD BURST LENGTH	8-WORD BURST LENGTH	16-WORD BURST LENGTH	CONTINUOUS BURST
-- (DEC)	BCR[3]	BCR3	LINEAR	LINEAR	LINEAR	LINEAR
0	0		0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-…
1	0		1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-4-5-6-7-…
2	0		2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-5-6-7-8-…
3	0		3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-6-7-8-9-…
4	0			4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-7-8-9-10-…
5	0			5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-8-9-10-11-…
6	0			6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-9-10-11-12-
7	0			7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-10-11-12-13-…
…	…	…	…	…	…	…
14	0				14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-17-18-19-20-..
15	0				15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20-21..
…	…	…	…		…	…
0		1	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6-…
1		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-4-5-6-7-…
2		1	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-5-6-7-8-…
3		1	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-6-7-8-9-…
4		1		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-7-8-9-10-…
5		1		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-…-15-16-17-18-19-20	5-6-7-8-9-10-11…
6		1		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-…-16-17-18-19-20-21	6-7-8-9-10-11-12…
7		1	…	7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-…-17-18-19-20-21-22	7-8-9-10-11-12-13…
…	…	…	…		…	…
14		1	…		14-15-16-17-18-19-…-23-24-25-26-27-28-29	14-15-16-17-18-19-20-…
15		1			15-16-17-18-19-20-…-24-25-26-27-28-29-30	15-16-17-18-19-20-21-…

Burst Length (BCR[2:0])
Default = Continuous Burst

Burst lengths define the number of words the device outputs during a burst READ operation. The device supports a burst length of 4, 8, or 16 words. The device can also be set in continuous burst mode where data is output sequentially without regard to address boundaries. WRITE bursts are always performed using continuous burst mode.

Burst Wrap (BCR[3])
Default = Burst Wraps Within Address Boundaries

The burst wrap option determines if a 4-, 8-, or 16-word burst READ wraps within the burst length or steps through sequential addresses. If the wrap option is not enabled, the device outputs data from sequential addresses without regard to burst boundaries. When continuous burst operation is selected, the internal address wraps to 000000h if the device is read past the last address.

Output Impedance (BCR[5])
Default = Outputs Use Full Drive Strength

The output driver strength can be altered to adjust for different data bus loading scenarios. The reduced-strength option will be more than adequate in stacked chip (Flash + CellularRAM) environments when there is a dedicated memory bus. The reduced-drive-strength option is included to minimize noise generated on the data bus during READ operations. Normal output impedance should be selected when using a discrete CellularRAM device in a more heavily loaded data bus environment. CellularRAM devices are tested using the full drive strength setting. Partial drive is approximately one-quarter full drive strength. Outputs are configured at full drive strength during testing.

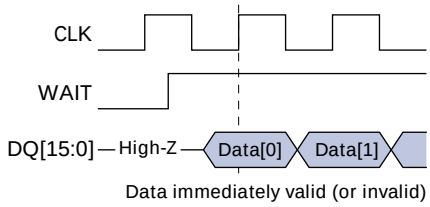
Clock Configuration (BCR[6])
Default = Transactions Processed on Rising Edge of Clock

The clock configuration bit indicates whether synchronous operations are dependant upon the rising or falling edge of the clock input. All of the timing diagrams in this data sheet show the bus interaction aligned with the rising edge of the clock.

WAIT Configuration (BCR[8])
Default = WAIT Transitions One Clock Before Data Valid/Invalid

The WAIT configuration bit is used to determine when WAIT transitions between the asserted and the de-asserted state with respect to valid data presented on the data bus. The memory controller will use the WAIT signal to coordinate data transfer during synchronous READ and WRITE operations. When BCR[8] = 0, data will be valid or invalid on the clock edge immediately after WAIT transitions to the de-asserted or asserted state, respectively (Figure 14, below, and Figure 16 on page 19). When A8 = 1, the WAIT signal transitions one clock period prior to the data bus going valid or invalid (Figures 15 below and 16 on page 18).

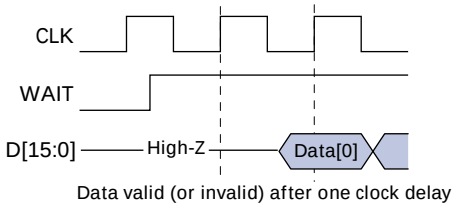
Figure 14: WAIT Configuration (BCR[8] = 0)



NOTE:

Data valid/invalid immediately after WAIT transitions (BCR[8] = 0). See Figure 15.

Figure 15: WAIT Configuration (BCR[8] = 1)



NOTE:

Valid/invalid data delayed for one clock after WAIT transitions (BCR[8] = 1). See Figure 16 on page 19.

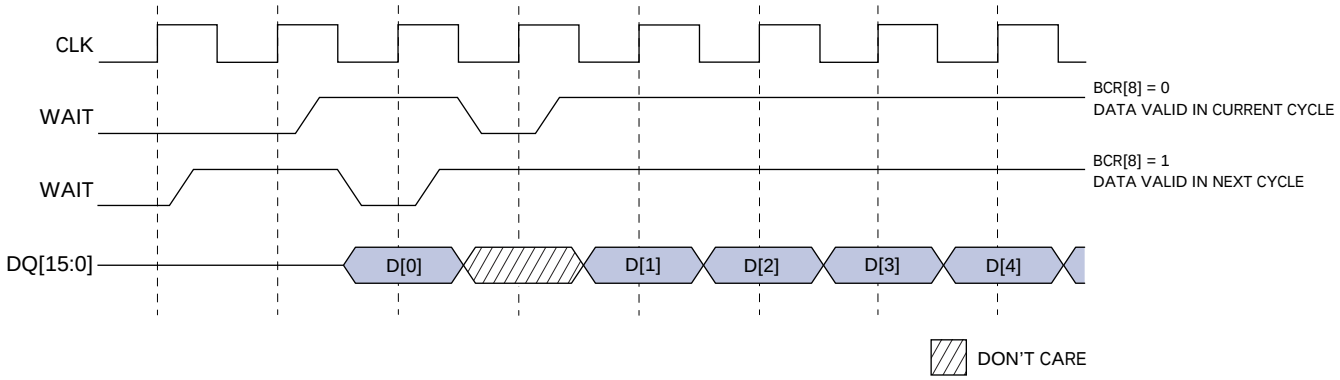
WAIT Polarity (BCR[10])
Default = WAIT Active HIGH

The WAIT polarity bit indicates whether an asserted WAIT output should be HIGH or LOW. This bit will determine whether the WAIT signal requires a pull-up or pull-down resistor to maintain the de-asserted state.

Latency Counter (BCR[13:11])
Default = Three-Clock Latency

The latency counter bits determine how many clocks occur between the beginning of a READ or WRITE operation and the first data value transferred. Only latency code two (three clocks) or latency code three (four clocks) is allowed (see Table 7 on page 20 and Figure 17 on page 20).

Figure 16: WAIT Configuration During Burst Operation[1]



NOTE:
1. Clocked on rising edge.

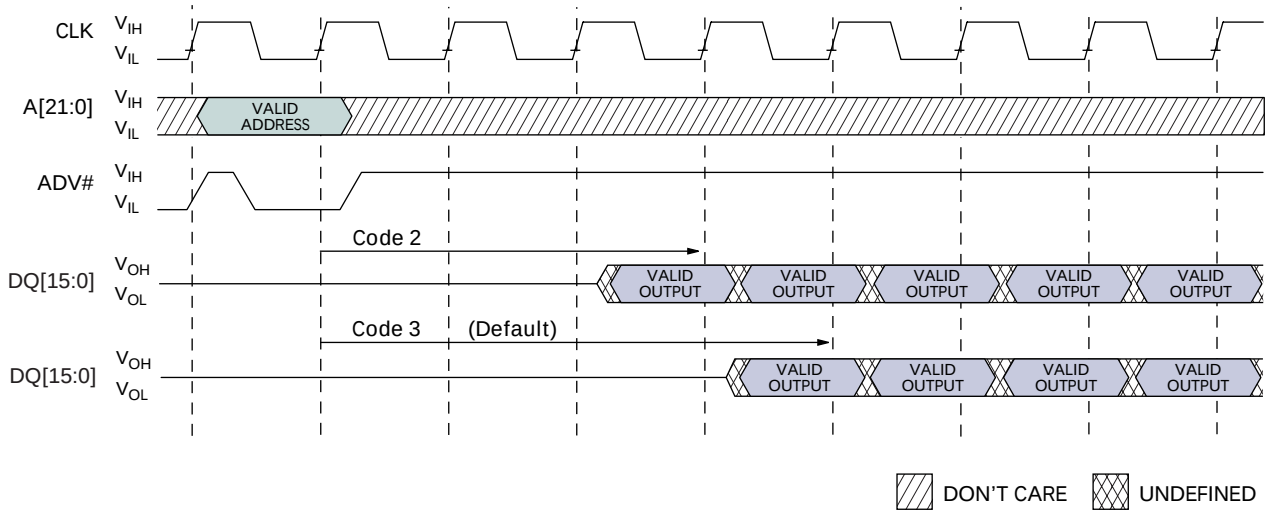
Table 7: Latency Configuration

LATENCY CONFIGURATION CODE	MAX INPUT CLK FREQUENCY (MHZ)	
	-701	-856
2 (3 clocks)	75 (13.3 ns)	44[1] (22.7 ns)
3 (4 clocks) – default	104 (9.62 ns)	66 (15.2 ns)

NOTE:

1. Clock rates below 50 MHz are allowed as long as ^{t}CSP specifications are met.

Figure 17: Latency Counter



Operating Mode (BCR[15])
Default = Asynchronous Operation

The operating mode bit selects either synchronous burst operation or the default asynchronous mode of operation.

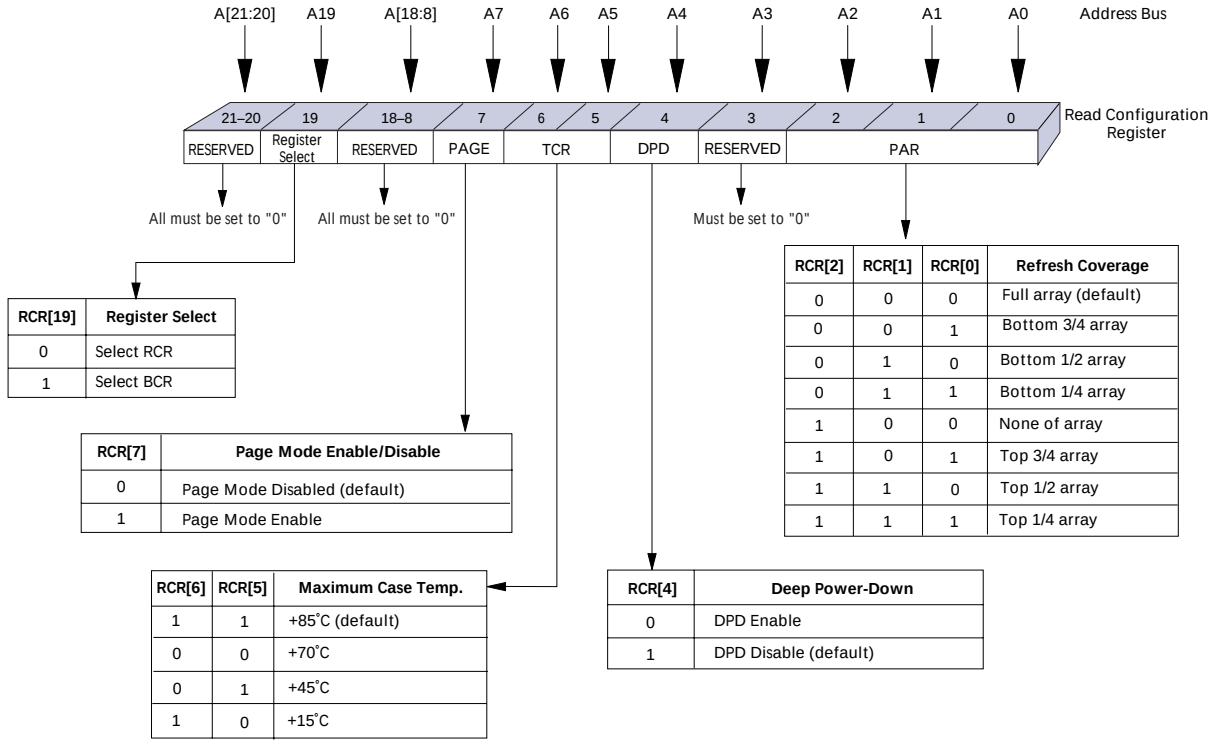
Refresh Configuration Register

The refresh configuration register (RCR) defines how the CellularRAM device performs its transparent self refresh. The RCR is loaded using either a synchronous or an asynchronous WRITE operation when A[19] is LOW and the configuration register enable (CRE) input is HIGH (see Figures 12 and 13 on page 15). When CRE is LOW, a READ or WRITE operation will access the memory array. The values placed on addresses A[21:0] are latched into the RCR on the rising edge of ADV#, CE#, or WE#, whichever occurs first. LB# and UB# are "Don't Care." Altering the refresh parameters can dramatically reduce current consumption during standby mode. Page mode control is also embedded into the RCR. Table 8 on page 21 describes the control bits used in the RCR. At power-up, the RCR is set to 0070h.

Partial Array Refresh (RCR[2:0])
Default = Full Array Refresh

The PAR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, three-quarters array, one-half array, one-quarter array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map (see Tables 9 and 10 on page 21).

Table 8: Refresh Configuration Register Mapping



RCR[19]	Register Select
0	Select RCR
1	Select BCR

RCR[7]	Page Mode Enable/Disable
0	Page Mode Disabled (default)
1	Page Mode Enable

RCR[6]	RCR[5]	Maximum Case Temp.
1	1	+85°C (default)
0	0	+70°C
0	1	+45°C
1	0	+15°C

RCR[4]	Deep Power-Down
0	DPD Enable
1	DPD Disable (default)

RCR[2]	RCR[1]	RCR[0]	Refresh Coverage
0	0	0	Full array (default)
0	0	1	Bottom 3/4 array
0	1	0	Bottom 1/2 array
0	1	1	Bottom 1/4 array
1	0	0	None of array
1	0	1	Top 3/4 array
1	1	0	Top 1/2 array
1	1	1	Top 1/4 array

Table 9: 64Mb Address Patterns for PAR (A4 = 1)

RCR[2]	RCR[1]	RCR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	000000h–3FFFFFh	4 Meg x 16	64Mb
0	0	1	Three-quarters of die	000000h–2FFFFFh	3 Meg x 16	48Mb
0	1	0	One-half of die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	1	1	One-quarter of die	000000h–0FFFFFh	1 Meg x 16	16Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	Three-quarters of die	100000h–3FFFFFh	3 Meg x 16	48Mb
1	1	0	One-half of die	200000h–3FFFFFh	2 Meg x 16	32Mb
1	1	1	One-quarter of die	300000h–3FFFFFh	1 Meg x 16	16Mb

Table 10: 32Mb Address Patterns for PAR (A4 = 1)

RCR[2]	RCR[1]	RCR[0]	ACTIVE SECTION	ADDRESS SPACE	SIZE	DENSITY
0	0	0	Full die	000000h–1FFFFFh	2 Meg x 16	32Mb
0	0	1	Three-quarters of die	000000h–17FFFFh	1.5 Meg x 16	24Mb
0	1	0	One-half of die	000000h–0FFFFFh	1 Meg x 16	16Mb
0	1	1	One-quarter of die	000000h–07FFFFh	512K x 16	8Mb
1	0	0	None of die	0	0 Meg x 16	0Mb
1	0	1	Three-quarters of die	080000h–1FFFFFh	1.5 Meg x 16	24Mb
1	1	0	One-half of die	100000h–1FFFFFh	1 Meg x 16	16Mb
1	1	1	One-quarter of die	180000h–1FFFFFh	512K x 16	8Mb

Deep Power-Down (RCR[4])
Default = DPD Disabled

The deep power-down bit enables and disables all refresh-related activity. This mode is used if the system does not require the storage provided by the CellularRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the CellularRAM device will require 150µs to perform an initialization procedure before normal operations can resume.

Deep power-down is enabled when RCR[4] = 0, and remains enabled until RCR[4] is set to "1."

Temperature Compensated Refresh (RCR[6:5])
Default = +85°C Operation

The TCR bits allow for adequate refresh at four different temperature thresholds (+15°C, +45°C, +70°C, and +85°C). The setting selected must be for a temperature higher than the case temperature of the CellularRAM device. If the case temperature is +50°C, the system can minimize self refresh current consumption by selecting the +70°C setting. The +15°C and +45°C settings would result in inadequate refreshing and cause data corruption.

Page Mode Operation (RCR[7])
Default = Disabled

The page mode operation bit determines whether page mode is enabled for asynchronous READ operations. In the power-up default state, page mode is disabled.

Absolute Maximum Ratings*

Voltage to Any Ball Except V_{CC}, V_{CCQ}
Relative to V_{SS} . . . . . .
. . . -0.50V to (4.0V or VccQ + 0.3V, whichever is less)
Voltage on V_{CC} Supply Relative to V_{SS}. . -0.2V to +2.45V
Voltage on V_{CCQ} Supply Relative to V_{SS} . -0.2V to +4.0V
Storage Temperature (plastic). . . . . -55ºC to +150ºC
Operating Temperature (case)
Wireless. . . . . -25ºC to +85ºC
Industrial . . . . . -40ºC to +85ºC
Soldering Temperature and Time
10s (lead only) . . . . . +260ºC

*Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 11: Electrical Characteristics and Operating Conditions

Wireless Temperature (-25ºC < T_C < +85ºC)
Industrial Temperature (-40ºC < T_C < +85ºC)

DESCRIPTION	CONDITIONS	SYMBOL	-70 (104 MHz)		-85 (66 MHz)		UNITS	NOTES
			MIN	MAX	MIN	MAX		
Supply Voltage		V_{CC}	1.70	1.95	1.70	1.95	V	
I/O Supply Voltage		V_{CCQ} (1.8V)	1.70	2.25	1.70	2.25	V	
Input High Voltage		V_{IH}	1.40	V_{CCQ} + 0.2	1.40	V_{CCQ} + 0.2	V	
Input Low Voltage		V_{IL}	-0.20	0.4	-0.20	0.4	V	
Output High Voltage	I_{OH} = -0.2mA	V_{OH}	0.80 V_{CCQ}		0.80 V_{CCQ}		V	
Output Low Voltage	I_{OL} = +0.2mA	V_{OL}		0.20 V_{CCQ}		0.20 V_{CCQ}	V	
Input Leakage Current	V_{IN} = 0 to V_{CCQ}	I_{LI}		1		1	µA	
Output Leakage Current	OE# = V_{IH} or Chip Disabled	I_{LO}		1		1	µA	2
READ Operating Current Asynchronous Random READ Asynchronous Page READ Initial Access, Burst READ Continuous Burst READ	V_{IN} = V_{CCQ} or 0V Chip Enabled, I_{OUT} = 0	I_{CC1}		 25 15 35 11		 25 15 35 11	mA	1, 2
WRITE Operating Current	V_{IN} = V_{CCQ} or 0V Chip Enabled	I_{CC2}		25		25	mA	1, 2
Standby Current (32Mb)	V_{IN} = V_{CCQ} or 0V Chip Disabled	I_{SB}		90		90	µA	2, 3
Standby Current (64Mb)	V_{IN} = V_{CCQ} or 0V Chip Disabled	I_{SB}		100		100	µA	2, 3

NOTE:

1. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected in the actual system.
2. This device assumes a standby mode if the chip is disabled (CE# HIGH). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling), regardless of the state of CE#. In order to achieve low standby current, all inputs must be driven to either V_{CCQ} or V_{SS}.
3. I_{SB} (MAX) values measured with PAR set to FULL ARRAY and TCR set to +85°C.

Table 12: Temperature Compensated Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	DENSITY	MAX CASE TEMPERATURES	TYP	MAX	UNITS
Temperature Compensated Refresh Standby Current	V_{IN} = V_{CC} or 0V Chip Disabled	I_{TCR}	64Mb	+85°C		100	µA
				+70°C		TBD	µA
				+45°C		TBD	µA
				+15°C		50	µA
			32Mb	+85°C		90	µA
				+70°C		TBD	µA
				+45°C		TBD	µA
				+15°C		50	µA

NOTE:

I_{TCR} (MAX) values measured with PAR set to FULL ARRAY.

Table 13: Partial Array Refresh Specifications and Conditions

DESCRIPTION	CONDITIONS	SYMBOL	DENSITY	ARRAY PARTITION	TYP	MAX	UNITS
Partial Array Refresh Standby Current	V_{IN} = V_{CC} or 0V, Chip Disabled	I_{PAR}	64Mb	Full		100	µA
				3/4		TBD	µA
				1/2		TBD	µA
				1/4		TBD	µA
				0		50	µA
			32Mb	Full		90	µA
				3/4		TBD	µA
				1/2		TBD	µA
				1/4		TBD	µA
				0		50	µA

NOTE:

I_{PAR} (MAX) values measured with TCR set to 85°C.

Table 14: Deep Power-Down Specifications

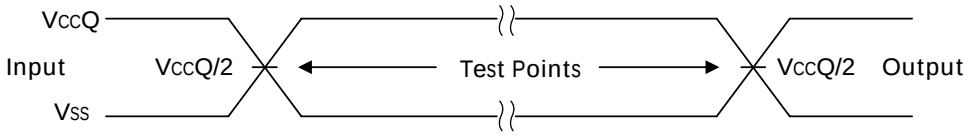
DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
Deep Power-Down	V_{IN} = V_{CC} or 0V; +25°C	I_{ZZ}		10	µA

Table 15: Capacitance

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T_C = +25ºC; f = 1 MHz;	C_{IN}	–	6	pF	1
Input/Output Capacitance (DQ)	V_{IN} = 0V	$C_{I/O}$	–	6	pF	1

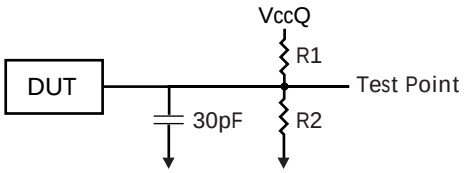
NOTE:
1. These parameters are verified in device characterization and are not 100% tested.

Figure 18: AC Input/Output Reference Waveform



NOTE:
AC test inputs are driven at VccQ for a logic 1 and Vss for a logic 0. Input timing begins at VccQ/2, and output timing ends at VccQ/2. Input rise and fall times (10% to 90%) < 1.6ns.

Figure 19: Output Load Circuit



NOTE:
All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).

Table 16: Output Load Circuit

VccQ	R1/R2
1.8V	2.7Ω
2.5V	3.7Ω
3.0V	4.5Ω

Table 17: Asynchronous READ Cycle Timing Requirements[1]

PARAMETER	SYMBOL	-701, -706		-856		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Access Time	t_{AA}		70		85	ns	
ADV# Access Time	t_{AADV}		70		85	ns	
Page Access Time	t_{APA}		20		25	ns	
Address Hold from ADV# HIGH	t_{AVH}	5		5		ns	
Address Setup to ADV# HIGH	t_{AVS}	10		10		ns	
LB#/UB# Access Time	t_{BA}		70		85	ns	
LB#/UB# Disable to High-Z Output	t_{BHZ}	0	8	0	8	ns	4
LB#/UB# Enable to Low-Z Output	t_{BLZ}	10		10		ns	3
CE# HIGH between Subsequent Mixed-Mode Operations	t_{CBPH}	5		5		ns	
Maximum CE# Pulse Width	t_{CEM}		10		10	µs	2
CE# LOW to WAIT Valid	t_{CEW}	1	7.5	1	7.5	ns	
Chip Select Access Time	t_{CO}		70		85	ns	
CE# LOW to ADV# HIGH	t_{CVS}	10		10		ns	
Chip Disable to High-Z Output	t_{HZ}	0	8	0	8	ns	4
Chip Enable to Low-Z Output	t_{LZ}	10		10		ns	3
Output Enable to Valid Output	t_{OE}		20		20	ns	
Output Hold from Output Disable	t_{OH}	5		5		ns	
Output Hold from Address Change	t_{OHA}	5		5		ns	
Output Disable to High-Z Output	t_{OHZ}	0	8	0	8	ns	4
Output Enable to Low-Z Output	t_{OLZ}	5		5		ns	3
Page Cycle Time	t_{PC}	20		25		ns	
READ Cycle Time	t_{RC}	70		85		ns	
Address Setting Time	t_{S}		10		10	µs	2
ADV# Pulse Width LOW	t_{VP}	10		10		ns	
ADV# Pulse Width HIGH	t_{VPH}	10		10		ns	

NOTE:

1. All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).
2. See the Appendix at the end of this data sheet.
3. High-Z to Low-Z timings are tested with the circuit shown in Figure 19 on page 25. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
4. Low-Z to High-Z timings are tested with the circuit shown in Figure 19 on page 25. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.

Table 18: Burst READ Cycle Timing Requirements[1]

PARAMETER	SYMBOL	-701		-706, -856		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Burst to READ Access Time	^tABA		33		55	ns	
CLK to Output Delay	^tACLK		6.5		10	ns	
Address Setup to ADV# HIGH	^tAVS	10		10		ns	
Burst OE# LOW to Output Delay	^tBOE		20		20	ns	
CE# HIGH between Subsequent Mixed-Mode Operations	^tCBPH	5		5		ns	
CE# LOW to WAIT Valid	^tCEW	1	7.5	1	7.5	ns	
CLK Period	^tCLK	9.62	20	15	20	ns	4
CE# Setup Time to Active CLK Edge	^tCSP	4	20	4	20	ns	
Hold Time from Active CLK Edge	^tHD	1		1		ns	
Chip Disable to High-Z Output	^tHZ	0	8	0	8	ns	2
CLK Rise or Fall Time	^tKHKL		1.6		1.6	ns	
CLK to WAIT Valid	^tKHTL		6.5		10	ns	
CLK to High-Z Output	^tKHZ	3	8	3	8	ns	
CLK to Low-Z Output	^tKLZ	2	5	2	5	ns	
Output HOLD from CLK	^tKOH	2		2		ns	
CLK HIGH or LOW Time	^tKP	3		3		ns	
Output Disable to High-Z Output	^tOHZ	0	8	0	8	ns	2
Output Enable to Low-Z Output	^tOLZ	5		5		ns	3
Setup Time to Active CLK Edge	^tSP	3		3		ns	

NOTE:

1. All tests are performed with the outputs configured for full drive strength (BCR[5] = 0).
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 19 on page 25. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.
3. High-Z to Low-Z timings are tested with the circuit shown in Figure 19 on page 25. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.
4. Clock rates below 50 MHz (^tCLK > 20ns) are allowed as long as ^tCSP specifcations are met.

Table 19: Asynchronous WRITE Cycle Timing Requirements

PARAMETER	SYMBOL	-701, -706		-856		UNITS	NOTES
		MIN	MAX	MIN	MAX		
Address Hold from ADV# Going HIGH	^tAVH	5		5		ns	
Address Setup to ADV# Going HIGH	^tAVS	10		10		ns	
Address Valid to End of Write	^tAW	70		85		ns	
LB#/UB# Select to End of Write	^tBW	70		85		ns	
Maximum CE# Pulse Width	^tCEM		10		10	µs	1
CE# LOW to WAIT Valid	^tCEW	1	7.5	1	7.5	ns	
Async Address-to-Burst Transition Time	^tCKA	70		85		ns	
CE# Low to ADV# HIGH	^tCVS	10		10		ns	
Chip Enable to End of Write	^tCW	70		85		ns	
Data Hold from Write Time	^tDH	0		0		ns	
Data Hold from Write Time	^tDH	0		0		ns	
Data to WRITE Time Overlap	^tDW	23		23		ns	1
Chip Enable to Low-Z Output	^tLZ	10		10		ns	3
End WRITE to Low-Z Output	^tOW	5		5		ns	3
Address Setup Time	^tAS	0		0		ns	1
ADV# Pulse Width	^tVP	10		10		ns	
ADV# Pulse Width HIGH	^tVPH	10		10		ns	
ADV# Setup to End of WRITE	^tVS	70		85		ns	
WRITE Cycle Time	^tWC	70		85		ns	
WRITE to High-Z Output	^tWHZ	0	8	0	8	ns	2
WRITE Pulse Width	^tWP	46		55		ns	1
WRITE Pulse Width HIGH	^tWPH	10		10		ns	
WRITE Recovery Time	^tWR	0		0		ns	

NOTE:

1. See the Appendix at the end of this data sheet.
2. Low-Z to High-Z timings are tested with the circuit shown in Figure 19 on page 25. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward $V_{CC}Q/2$.
3. High-Z to Low-Z timings are tested with the circuit shown in Figure 19 on page 25. The Low-Z timings measure a 100mV transition away from the High-Z ($V_{CC}Q/2$) level toward either V_{OH} or V_{OL}.

Table 20: Burst WRITE Cycle Timing Requirements

PARAMETER	SYMBOL	-701		-706, -856		UNITS	NOTES
		MIN	MAX	MIN	MAX		
CE# HIGH between Subsequent Mixed-Mode Operations	$^{t}CBPH$	5		5		ns	
CE# LOW to WAIT Valid	^{t}CEW	1	7.5	1	7.5	ns	
Clock Period	^{t}CLK	9.62	20	15	20	ns	1
CE# Setup to CLK Active Edge	^{t}CSP	4	20	4	20	ns	
Hold Time from Active CLK Edge	^{t}HD	1		1		ns	
CLK Rise or Fall Time	$^{t}KHKL$		1.6		1.6	ns	
Clock to WAIT Valid	$^{t}KHTL$		6.5		10	ns	
CLK HIGH or LOW Time	^{t}KP	3		3		ns	
Setup Time to Activate CLK Edge	^{t}SP	3		3		ns	

NOTE:

1. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 21: Initialization Timing Requirements

PARAMETER	SYMBOL	-701, -706		-856		UNITS	NOTE
		MIN	MAX	MIN	MAX		
Initialization Period (required before normal operations)	^{t}PU		150		150	µs	

Burst CellularRAM Timing Diagrams

Figure 20: Initialization Period

Table 22: Initialization Timing Parameters

PARAMETER	SYMBOL	-701, -706		-856		UNITS	NOTE
		MIN	MAX	MIN	MAX		
Initialization Period	t_{PU}		150		150	µs	

Figure 21: Asynchronous READ

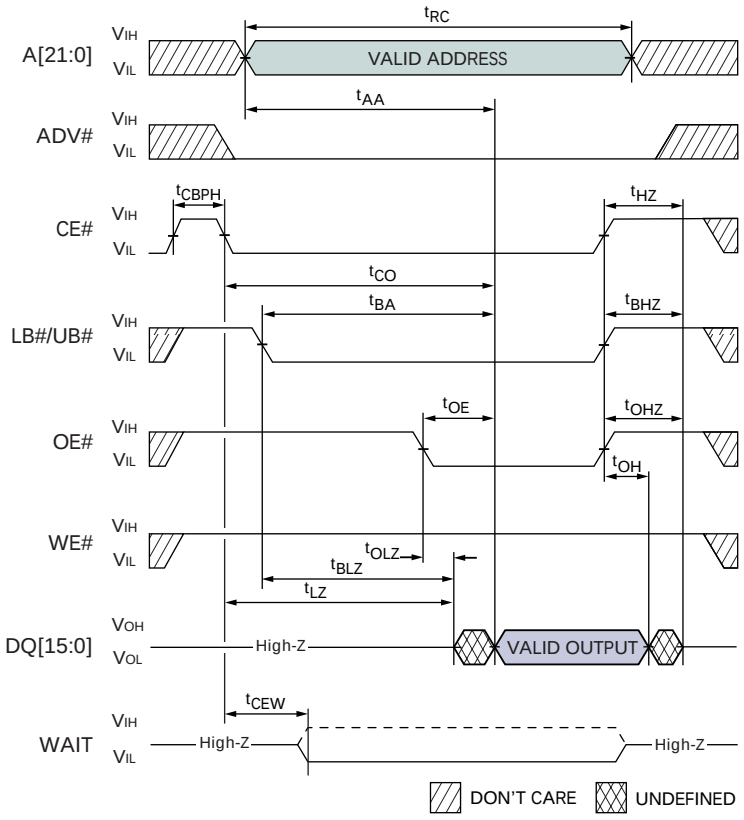


Table 23: Asynchronous READ Timing Parameters

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		70		85	ns
t_{BA}		70		85	ns
t_{BHZ}	0	8	0	8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEW}	1	7.5	1	7.5	ns
t_{CO}		70		85	ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{HZ}	0	8	0	8	ns
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OH}	5		5		ns
t_{OHZ}	0	8	0	8	ns
t_{OLZ}	5		5		ns
t_{RC}	70		85		ns

Figure 22: Asynchronous READ Using ADV#

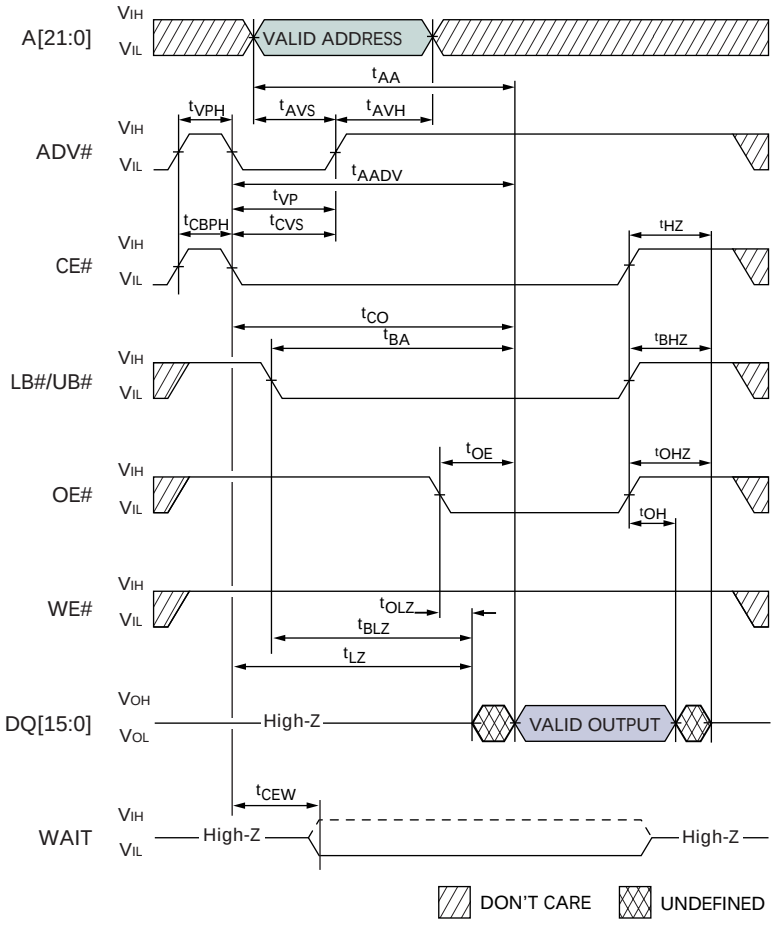


Table 24: Asynchronous READ Timing Parameters

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
tAA		70		85	ns
tAADV		70		85	ns
tAVH	5		5		ns
tAVS	10		10		ns
tBA		70		85	ns
tBHZ	0	8	0	8	ns
tBLZ	10		10		ns
tCBPH	5		5		ns
tCEW	1	7.5	1	7.5	ns
tCO		70		85	ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
tCVS	10		10		ns
tHZ	0	8	0	8	ns
tLZ	10		10		ns
tOE		20		20	ns
tOH	5		5		ns
tOHZ	0	8	0	8	ns
tOLZ	5		5		ns
tVP	10		10		ns
tVPH	10		10		ns

Figure 23: Page Mode READ

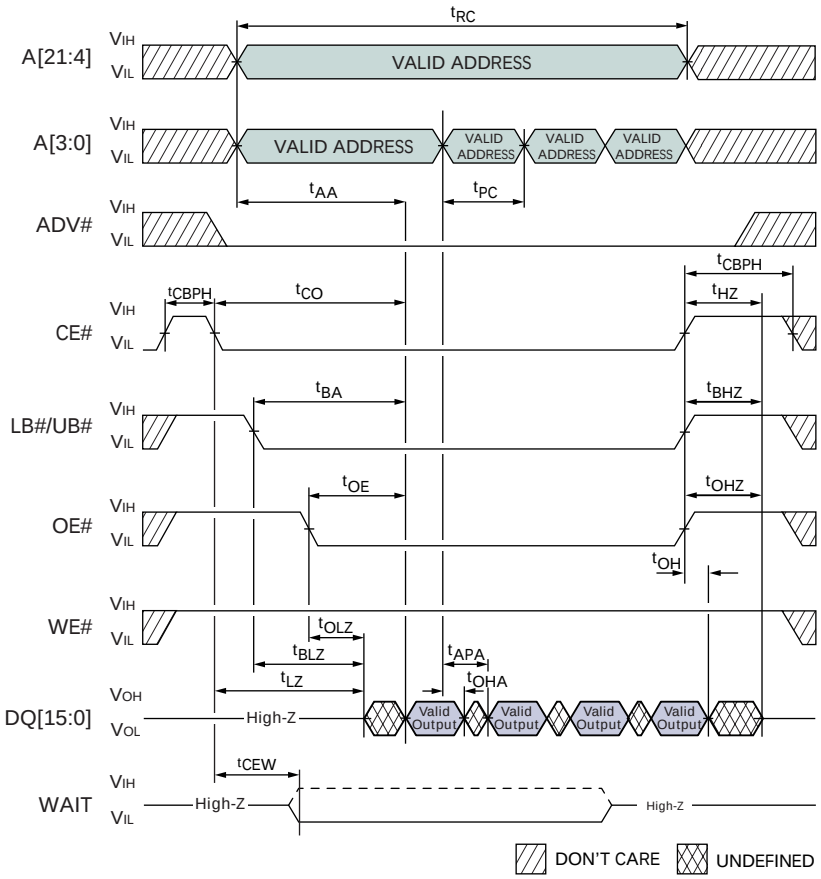
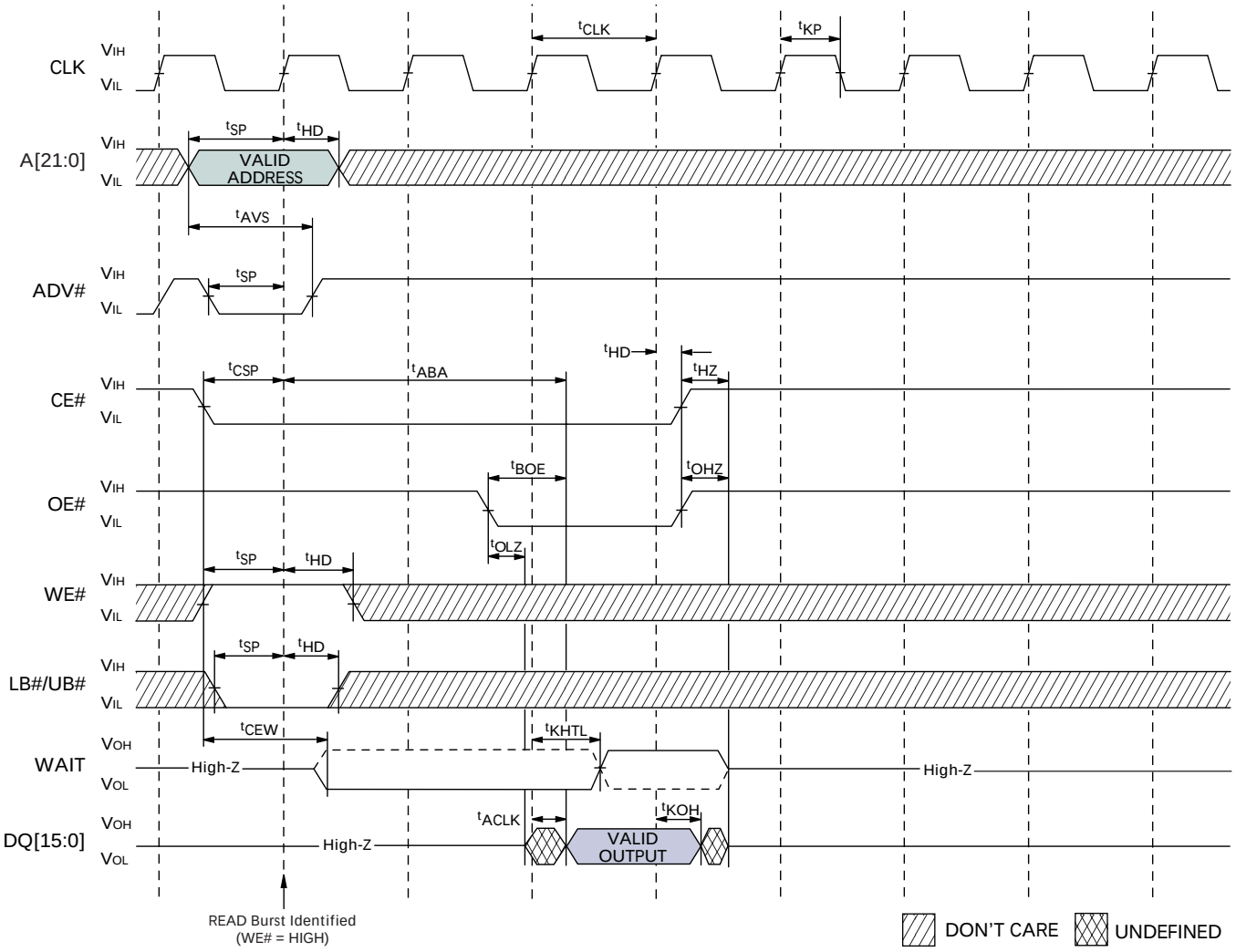


Table 25: Asynchronous READ Timing Parameters (Page Mode Operation)

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
tAA		70		85	ns
tAPA		20		25	ns
tBA		70		85	ns
tBHZ	0	8	0	8	ns
tBLZ	10		10		ns
tCBPH	5		5		ns
tCEW	1	7.5	1	7.5	ns
tCO		70		85	ns
tHZ	0	8	0	8	ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
tLZ	10		10		ns
tOE		20		20	ns
tOH	5		5		ns
tOHA	5		5		ns
tOHZ	0	8	0	8	ns
tOLZ	5		5		ns
tPC	20		25		ns
tRC	70		85		ns

Figure 24: Single-Access Burst READ Operation[1]



NOTE:

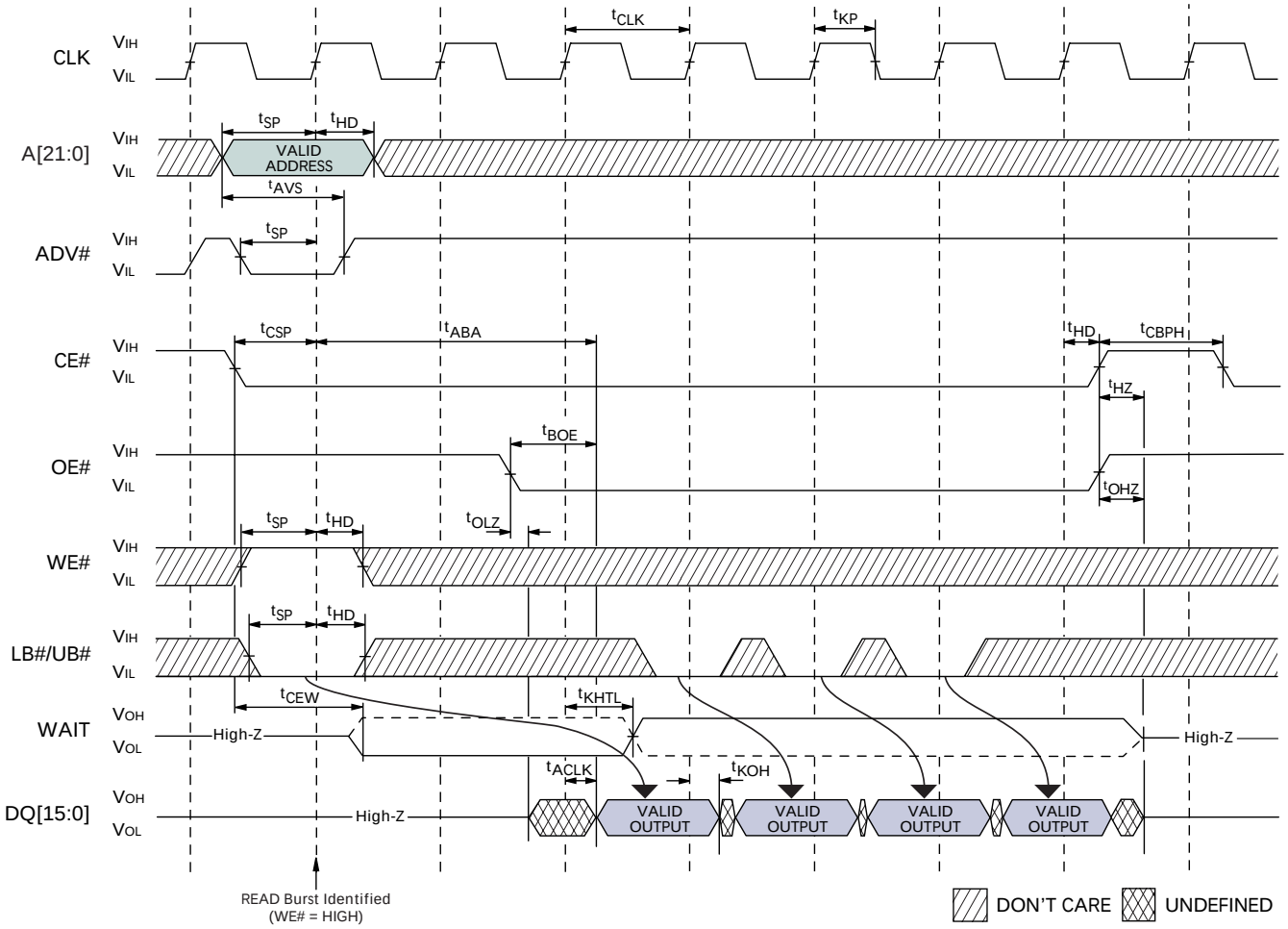
1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 26: Burst READ Timing Parameters

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}ABA		33		55	ns
^{t}ACLK		6.5		10	ns
^{t}AVS	10		10		ns
^{t}BOE		20		20	ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	4	20	ns
^{t}HD	1		1		ns

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}HZ	0	8	0	8	ns
^{t}KHTL		6.5		10	ns
^{t}KOH	2		2		ns
^{t}KP	3		3		ns
^{t}OHZ	0	8	0	8	ns
^{t}OLZ	5		5		ns
^{t}SP	3		3		ns

Figure 25: 4-Word Burst READ Operation[1]



NOTE:

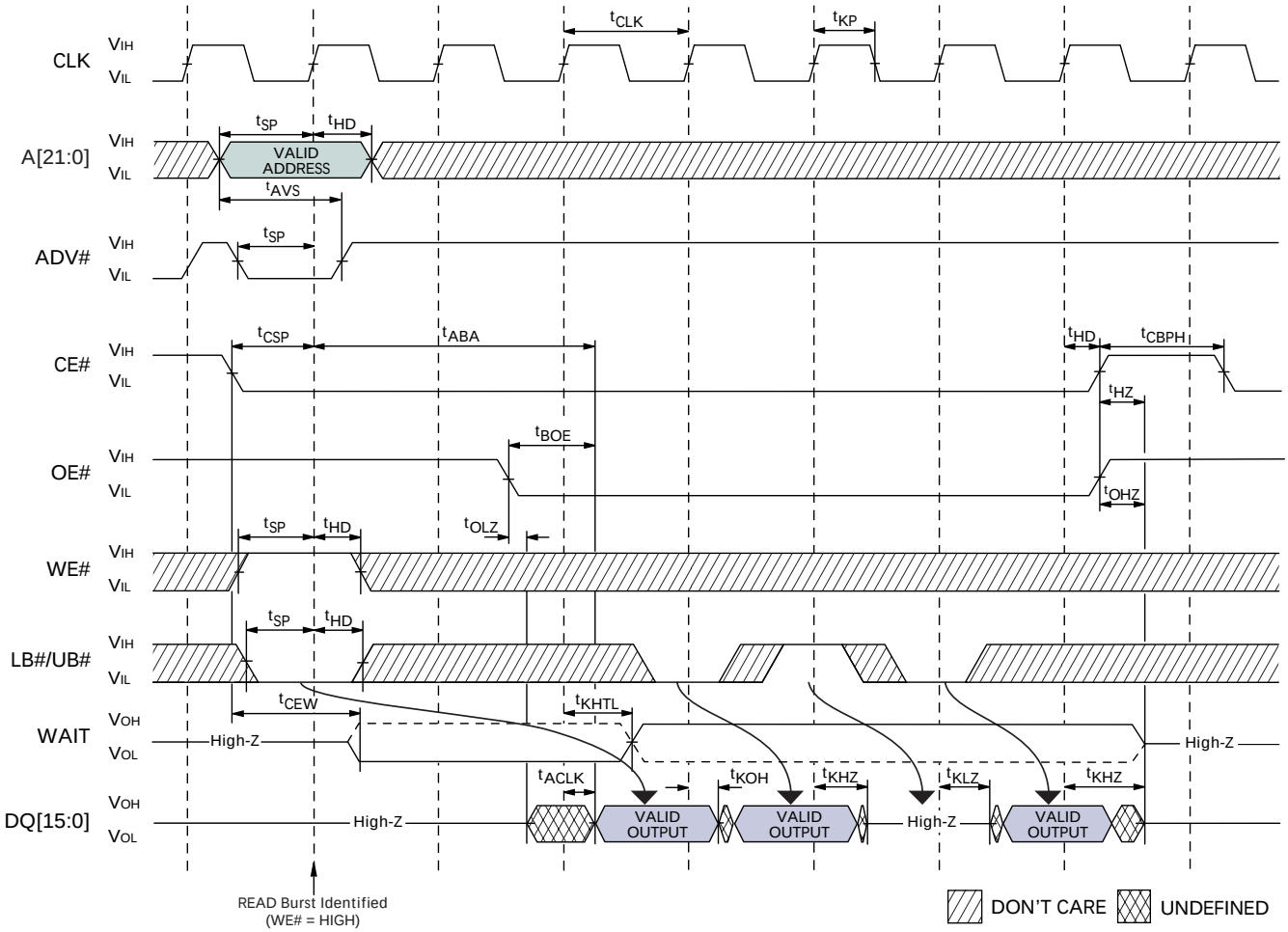
1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 27: Burst READ Timing Parameters

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}ABA		33		55	ns
^{t}ACLK		6.5		10	ns
^{t}AVS	10		10		ns
^{t}BOE		20		20	ns
^{t}CBPH	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	4	20	ns

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}HD	1		1		ns
^{t}HZ	0	8	0	8	ns
^{t}KHTL		6.5		10	ns
^{t}KOH	2		2		ns
^{t}KP	3		3		ns
^{t}OHZ	0	8	0	8	ns
^{t}OLZ	5		5		ns
^{t}SP	3		3		ns

Figure 26: 4-Word Burst READ Operation (with LB#/UB#)[1]



NOTE:

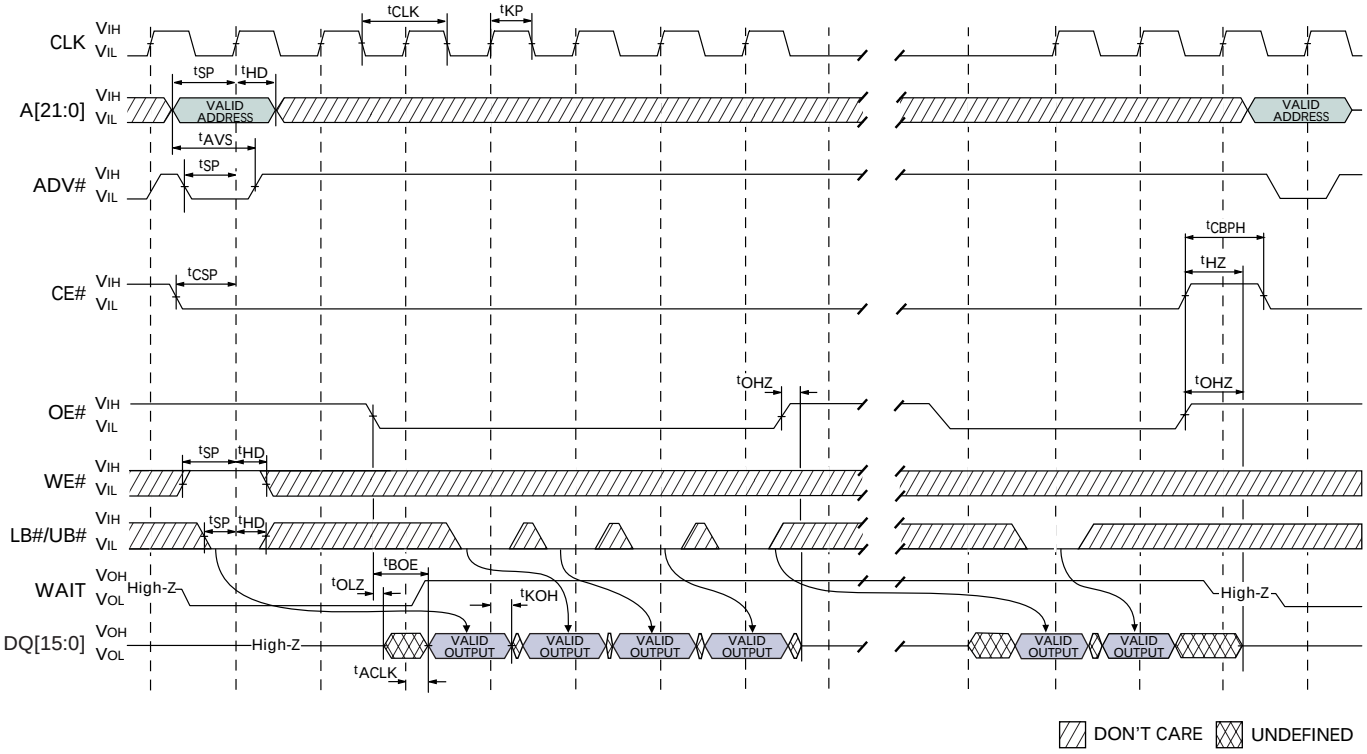
1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met. BCR configured with a burst length of four.

Table 28: Burst READ Timing Parameters (with LB#/UB#)

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}ABA		33		55	ns
^{t}ACLK		6.5		10	ns
^{t}AVS	10		10		ns
^{t}BOE		20		20	ns
^{t}CBPH	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	4	20	ns
^{t}HD	1		1		ns

SYMBOL	-701 MIN	-701 MAX	-706, -856 MIN	-706, -856 MAX	UNITS
^{t}HZ	0	8	0	8	ns
^{t}KHTL		6.5		10	ns
^{t}KHZ	3	8	3	8	ns
^{t}KLZ	2	5	2	5	ns
^{t}KOH	2		2		ns
^{t}KP	3		3		ns
^{t}OHZ	0	8	0	8	ns
^{t}OLZ	5		5		ns
^{t}SP	3		3		ns

Figure 27: READ Burst Suspend[1]



NOTE:

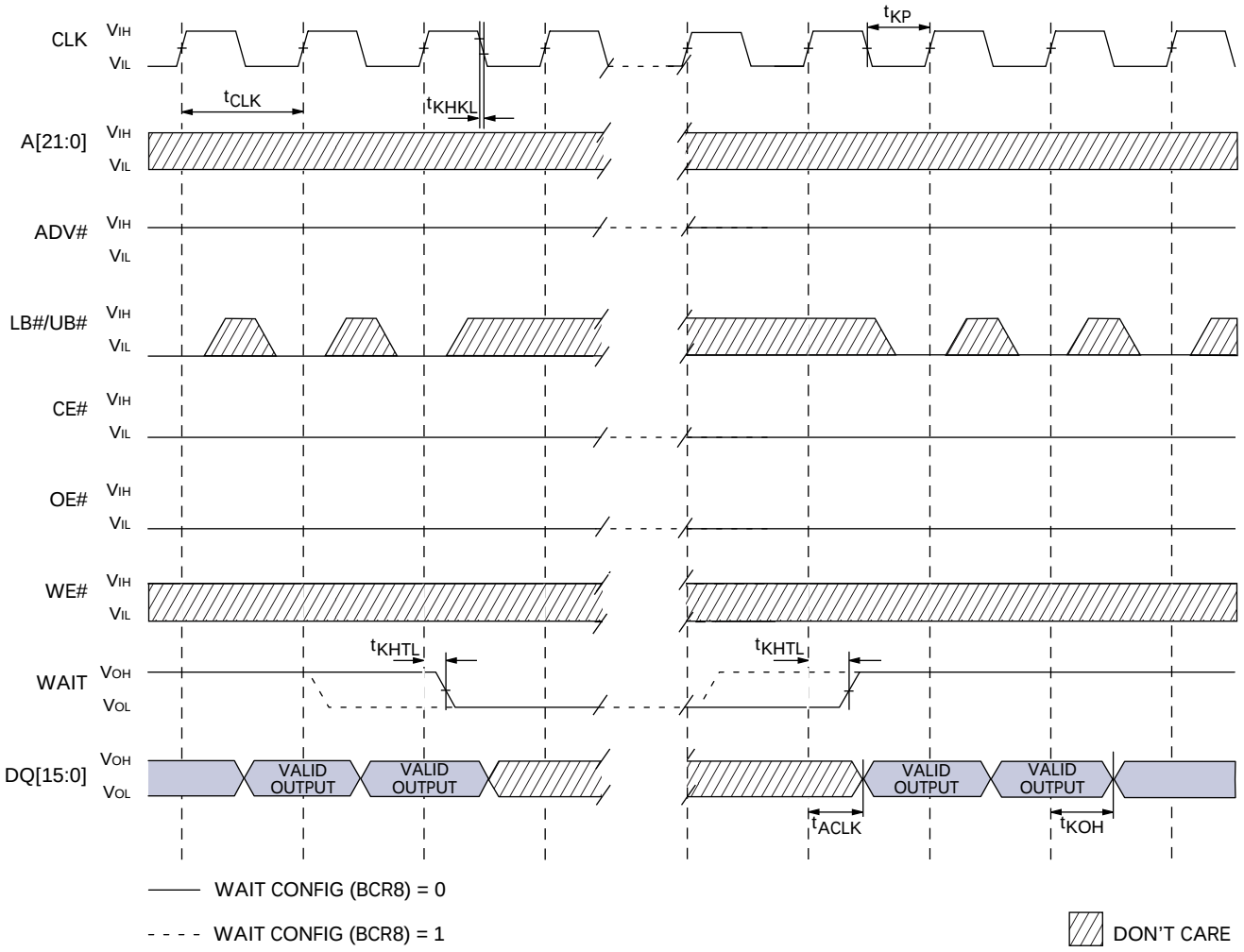
1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 29: Burst READ Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}ACLK		6.5		10	ns
^{t}AVS	10		10		ns
^{t}BOE		20		20	ns
^{t}CBPH	5		5		ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	4	20	ns
^{t}HD	1		1		ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}HZ	0	8	0	8	ns
^{t}KOH	2		2		ns
^{t}KP	3		3		ns
^{t}OHZ	0	8	0	8	ns
^{t}OLZ	5		5		ns
^{t}SP	3		3		ns

Figure 28: Continuous Burst READ Showing an Output Delay with BCR[8] = 0(1) for End-of-Row Condition[1]



NOTE:
1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 30: Burst READ Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}ACLK		6.5		10	ns
^{t}CLK	9.62	20	15	20	ns
^{t}KHKL		1.6		1.6	ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}KHTL		6.5		10	ns
^{t}KOH	2		2		ns
^{t}KP	3		3		ns

Figure 29: CE#-Controlled Asynchronous WRITE

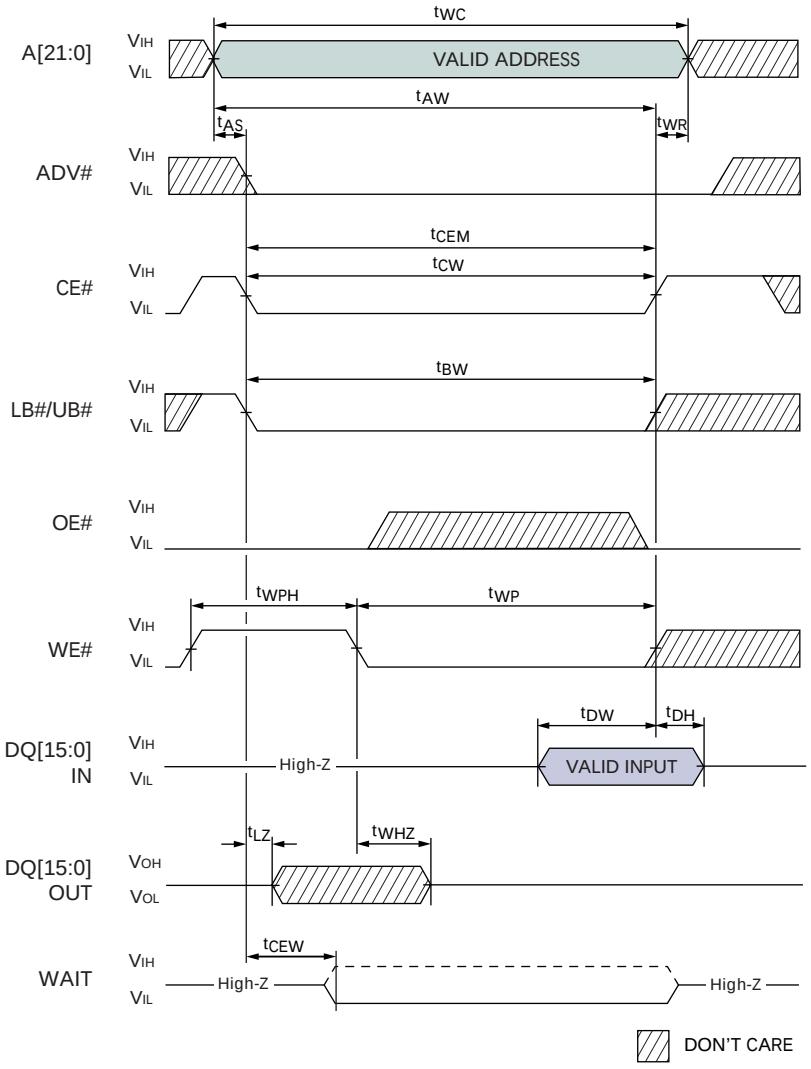


Table 31: Asynchronous WRITE Timing Parameters

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		10		10	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{DW}	23		23		ns
t_{LZ}	10		10		ns
t_{WC}	70		85		ns
t_{WHZ}	0	8	0	8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Figure 30: LB#/UB#-Controlled Asynchronous WRITE

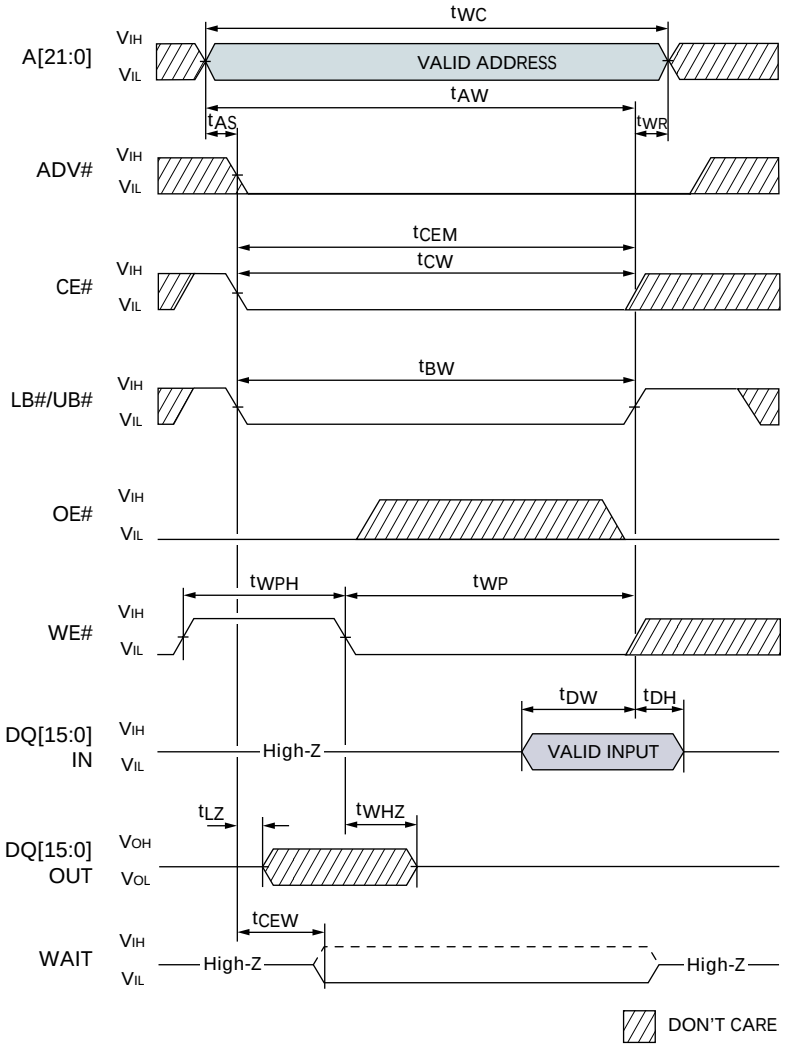


Table 32: Asynchronous WRITE Timing Parameters

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		10		10	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{DW}	23		23		ns
t_{LZ}	10		10		ns
t_{WC}	70		85		ns
t_{WHZ}	0	8	0	8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Figure 31: WE#-Controlled Asynchronous WRITE

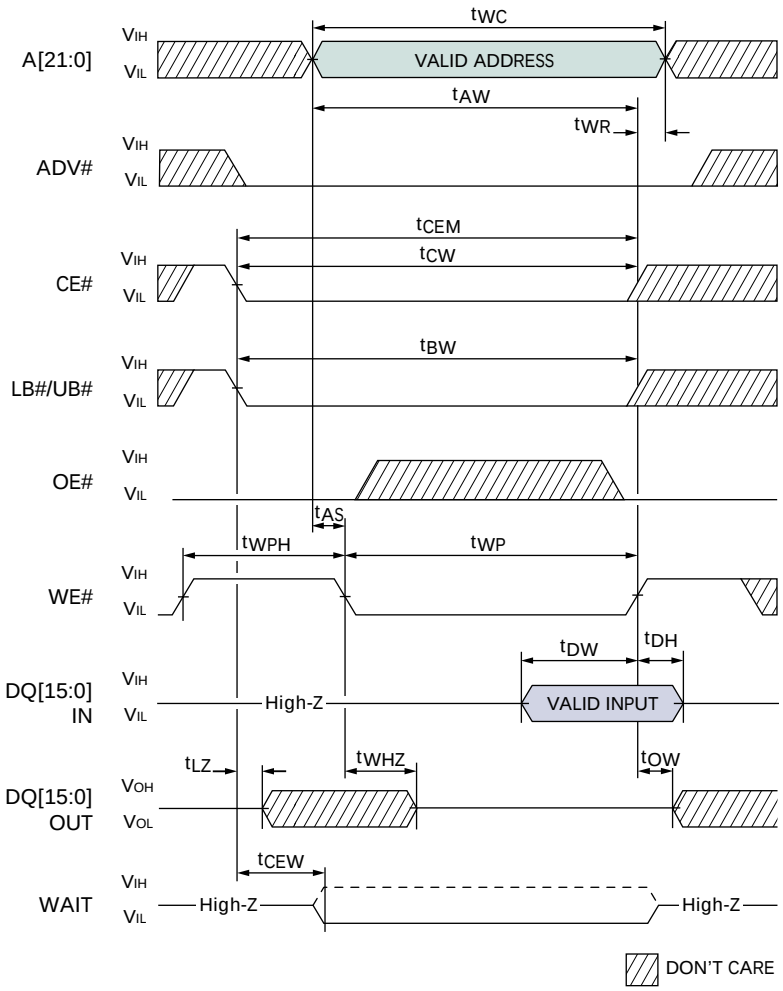


Table 33: Asynchronous WRITE Timing Parameters

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{AS}	0		0		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		10		10	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{LZ}	10		10		ns
t_{OW}	5		5		ns
t_{WC}	70		85		ns
t_{WHZ}	0	8	0	8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Figure 32: Asynchronous WRITE Using ADV#

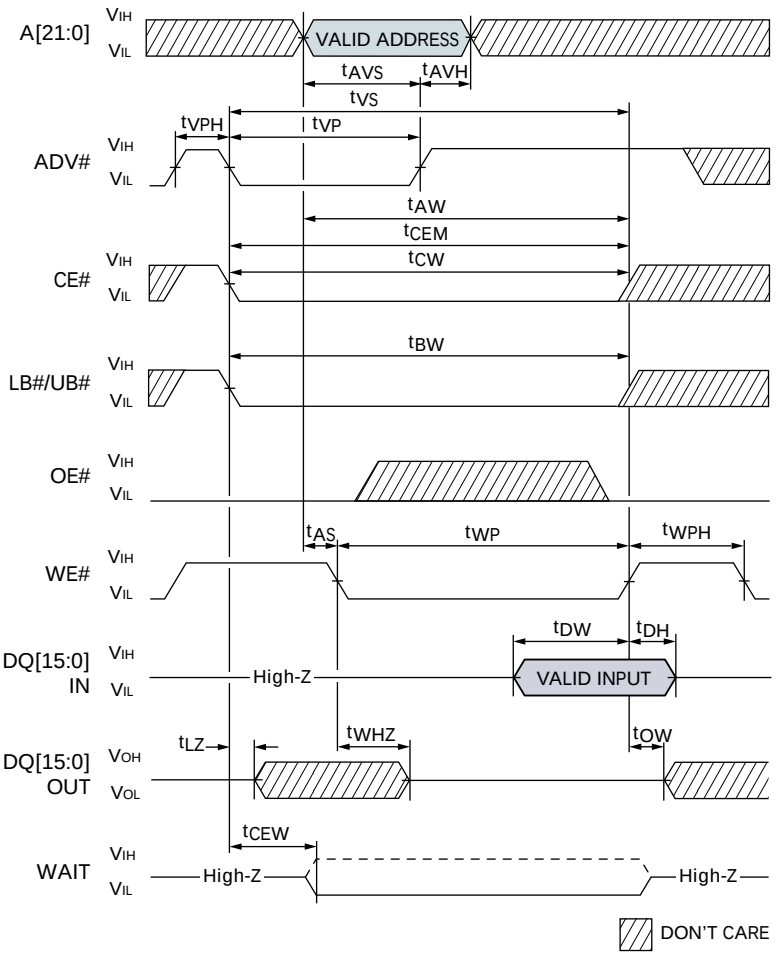
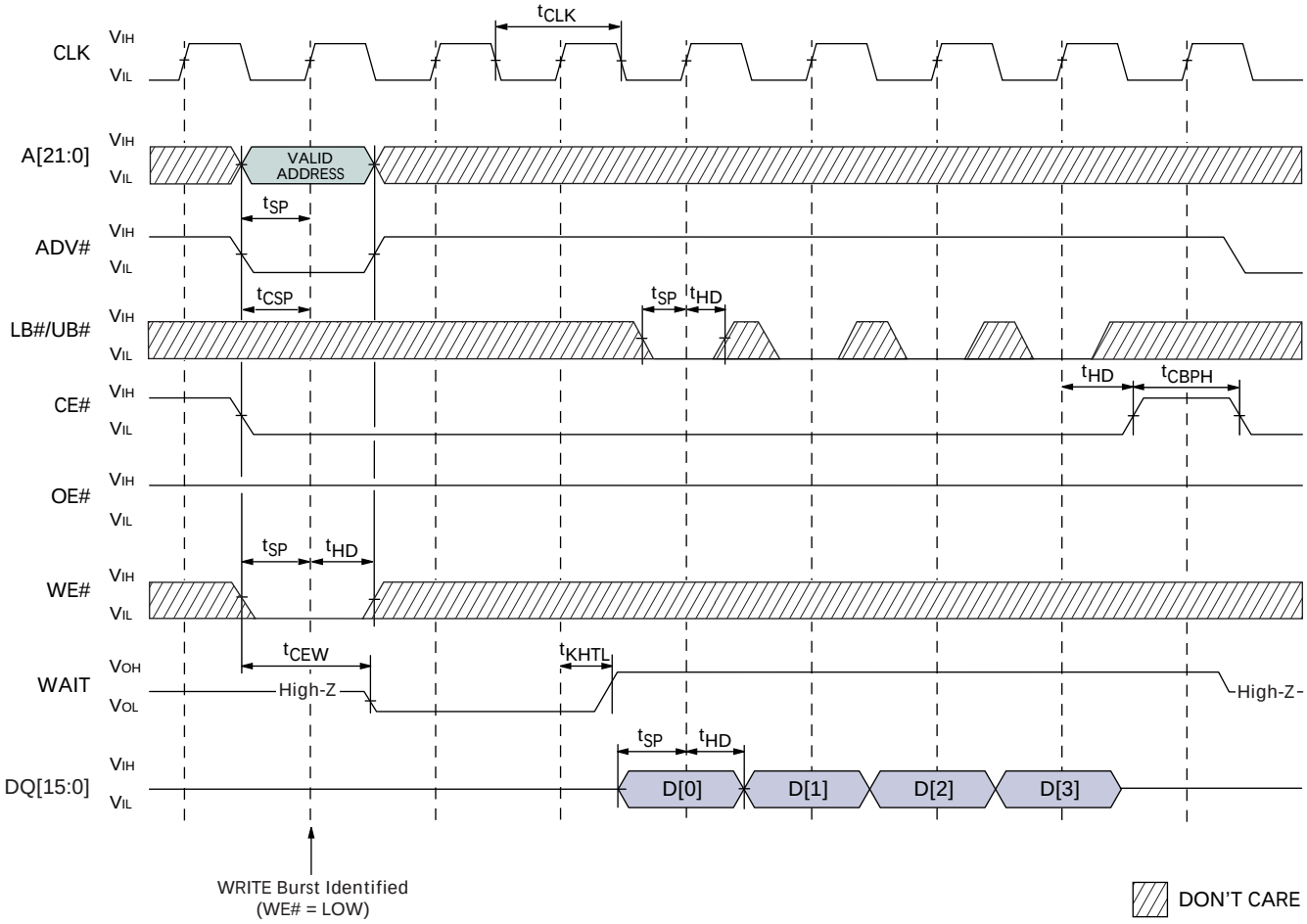


Table 34: Asynchronous WRITE Timing Parameters

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{AS}	0		0		ns
t_{AVH}	5		5		ns
t_{AVS}	10		10		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CEM}		10		10	µs
t_{CEW}	1	7.5	1	7.5	ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
t_{DW}	23		23		ns
t_{LZ}	10		10		ns
t_{OW}	5		5		ns
t_{VP}	10		10		ns
t_{VPH}	10		10		ns
t_{VS}	70		85		ns
t_{WHZ}	0	8	0	8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns

Figure 33: Burst WRITE Operation[1]



NOTE:

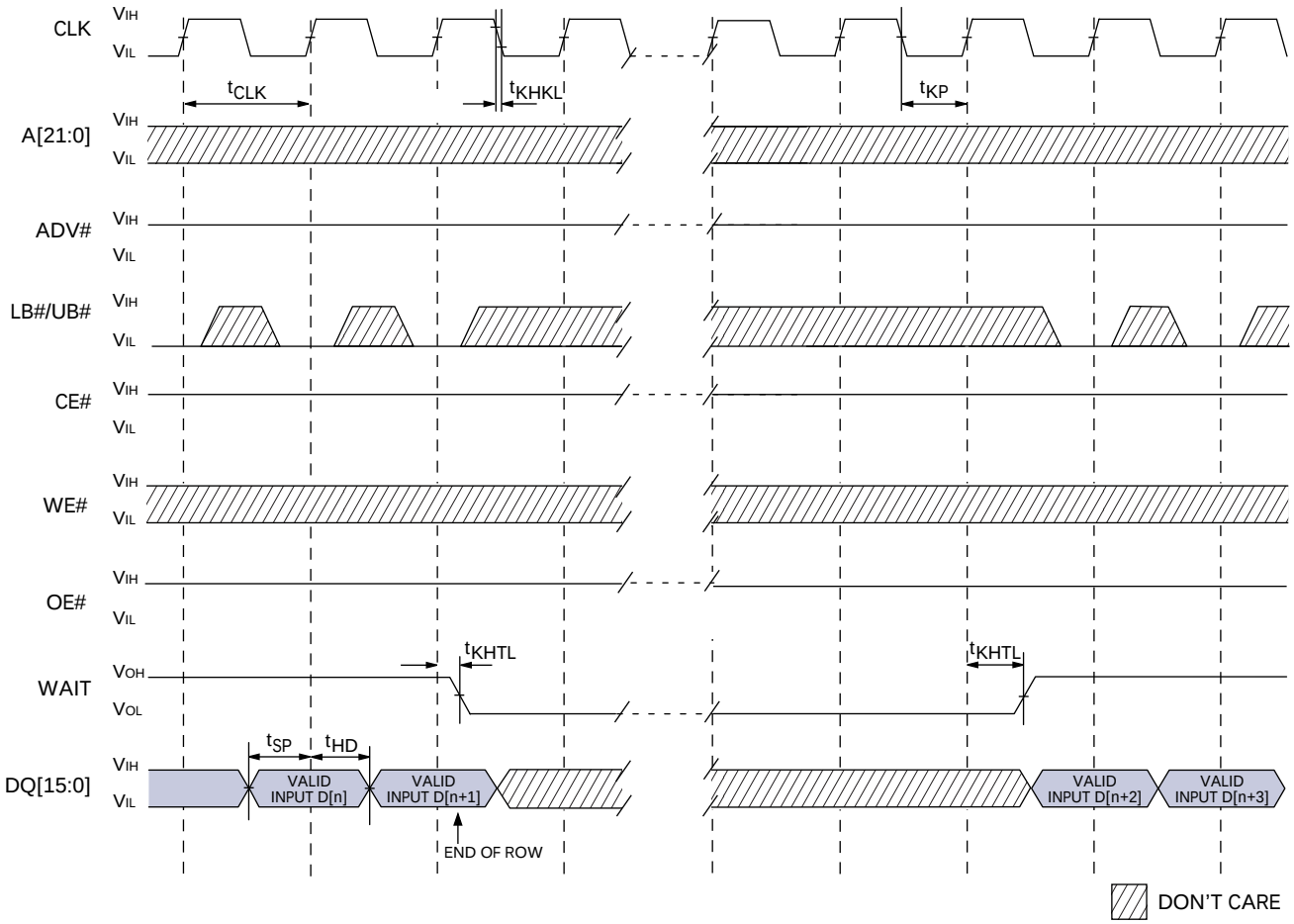
1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 35: Burst WRITE Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}CBPH	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	4	20	ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}HD	1		1		ns
^{t}KHTL		6.5		10	ns
^{t}SP	3		3		ns

Figure 34: Continuous Burst WRITE Showing an Output Delay with BCR[8] = 0(1) for End-of-Row Condition[1]



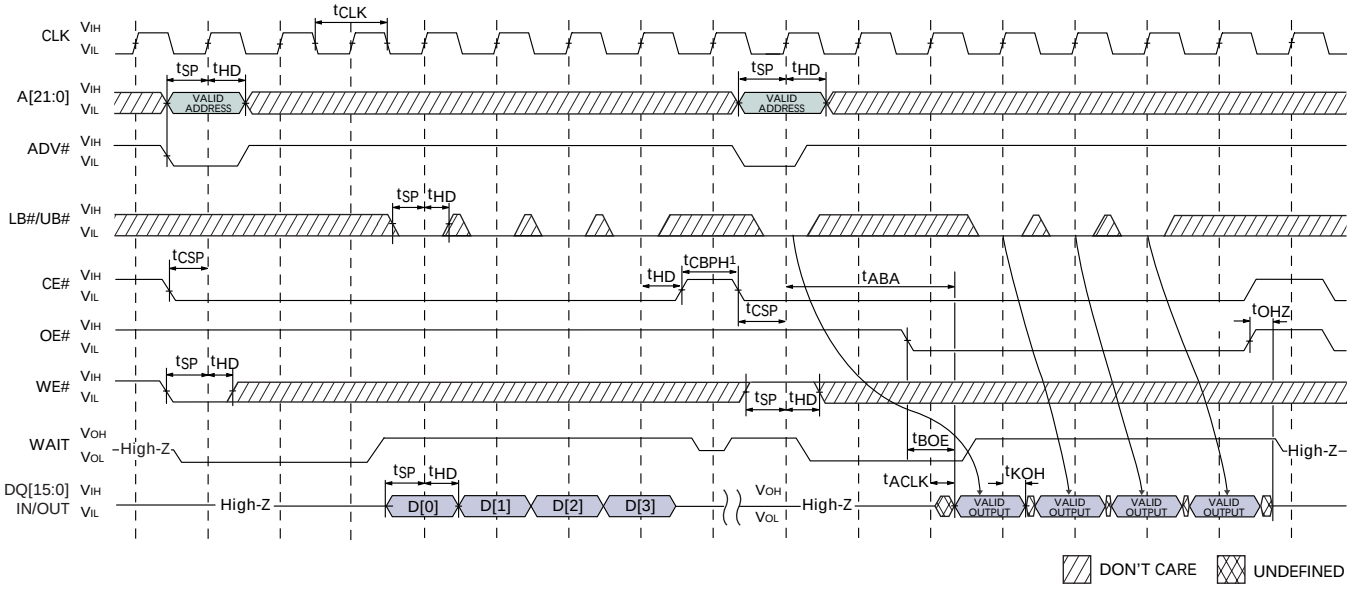
NOTE:
1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 36: Burst WRITE Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}CLK	9.62	20	15	20	ns
^{t}HD	1		1		ns
^{t}KHKL		1.6		1.6	ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}KHTL		6.5		10	ns
^{t}KP	3		3		ns
^{t}SP	3		3		ns

Figure 35: Burst WRITE Followed by Burst READ[1]



NOTE:

1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. To allow self-refresh operations to occur between transactions, CE# must remain HIGH for at least 5ns (^{t}CBPH) to schedule the appropriate internal refresh operation.
3. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 37: WRITE Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}CBPH	5		5		ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	4	20	ns

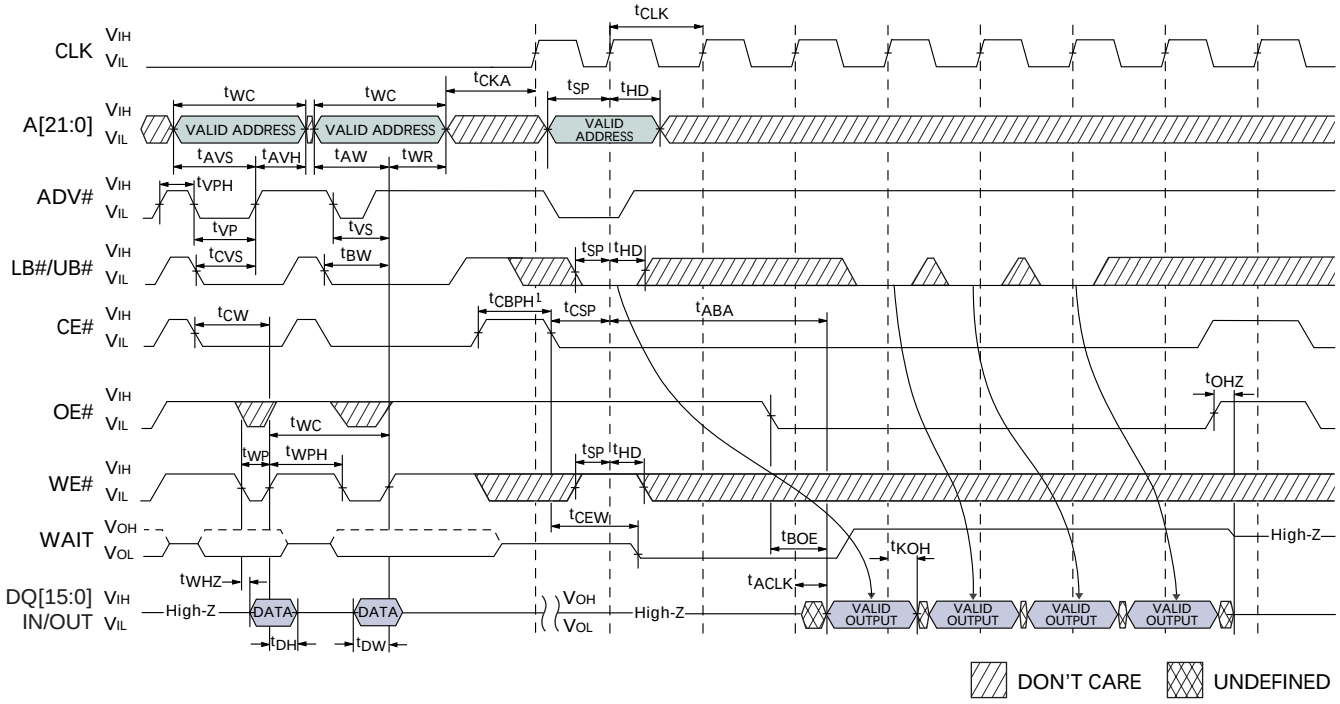
SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}HD	1		1		ns
^{t}SP	3		3		ns

Table 38: READ Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}ABA		33		55	ns
^{t}ACLK		6.5		10	ns
^{t}BOE		20		20	ns
^{t}CLK	9.62	20	15	20	ns
^{t}CSP	4	20	4	20	ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}HD	1		1		ns
^{t}KOH	2		2		ns
^{t}OHZ	0	8	0	8	ns
^{t}OHZ	0	8	0	8	ns
^{t}SP	3		3		ns

Figure 36: Asynchronous WRITE Followed by Burst READ[1]



NOTE:

1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and burst operations, CE# must go HIGH. CE# must remain HIGH for at least 5ns (tCBPH) to schedule the appropriate internal refresh operation.
3. Clock rates below 50 MHz (tCLK > 20ns) are allowed as long as tCSP specifications are met.

Table 39: WRITE Timing Parameters

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
tAVH	5		5		ns
tAVS	10		10		ns
tAW	70		85		ns
tBW	70		85		ns
tCKA	70		85		ns
tCVS	10		10		ns
tCW	70		85		ns
tDH	0		0		ns
tDW	20		23		ns

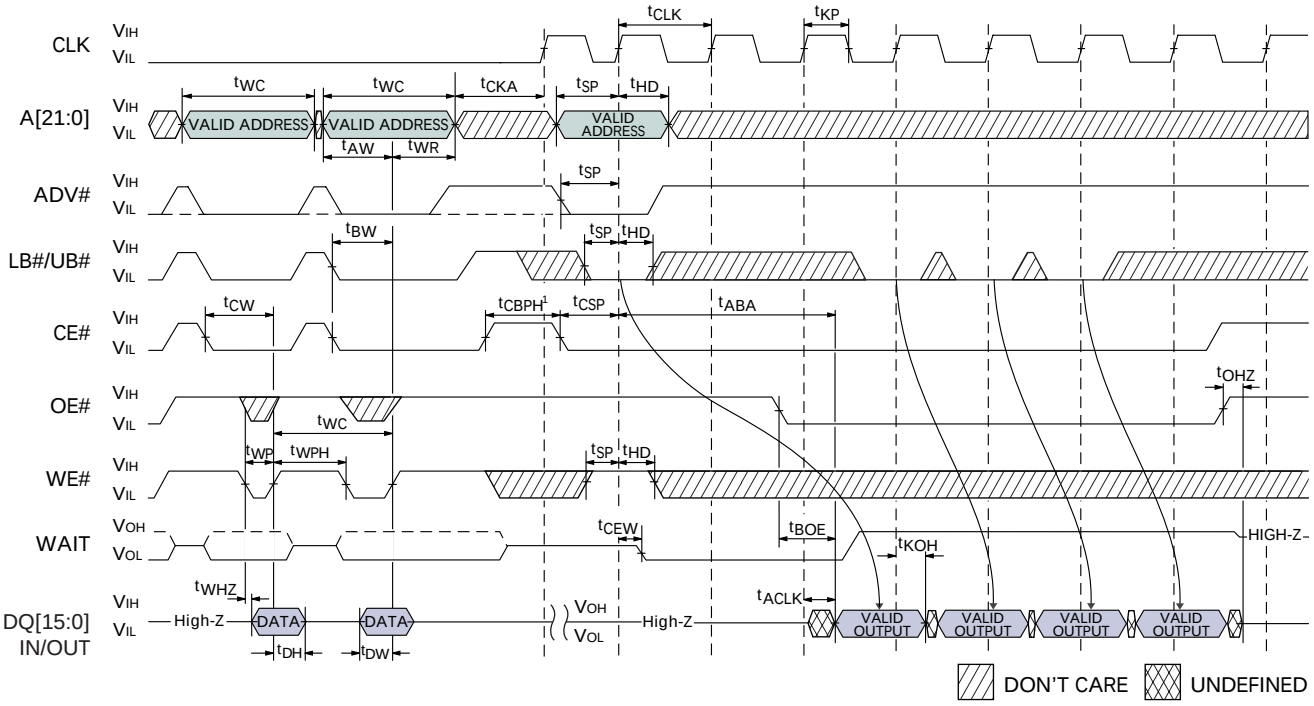
SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
tVP	10		10		ns
tVPH	10		10		ns
tVS	70		85		ns
tWC	70		85		ns
tWHZ	0	8	0	8	ns
tWP	46		55		ns
tWPH	10		10		ns
tWR	0		0		ns

Table 40: READ Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
tABA		33		55	ns
tACLK		6.5		10	ns
tBOE		20		20	ns
tCBPH	5		5		ns
tCEW	1	7.5	1	7.5	ns
tCLK	9.62	20	15	20	ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
tCSP	4	20	4	20	ns
tHD	1		1		ns
tKOH	2		2		ns
tOHZ	0	8	0	8	ns
tSP	3		3		ns

Figure 37: Asynchronous WRITE Followed By Burst READ—ADV# LOW[1]



NOTE:

1. Nondefault BCR settings: Latency code two (three clocks); WAIT active LOW; WAIT asserted during delay.
2. When transitioning between asynchronous and burst operations, CE# must go HIGH. CE# must remain HIGH for at least 5ns (^{t}CBPH) to schedule the appropriate internal refresh operation.
3. Clock rates below 50 MHz (^{t}CLK > 20ns) are allowed as long as ^{t}CSP specifications are met.

Table 41: WRITE Timing Parameters

SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}AW	70		85		ns
^{t}BW	70		85		ns
^{t}CKA	70		85		ns
^{t}CW	70		85		ns
^{t}DH	0		0		ns
^{t}DW	23		23		ns

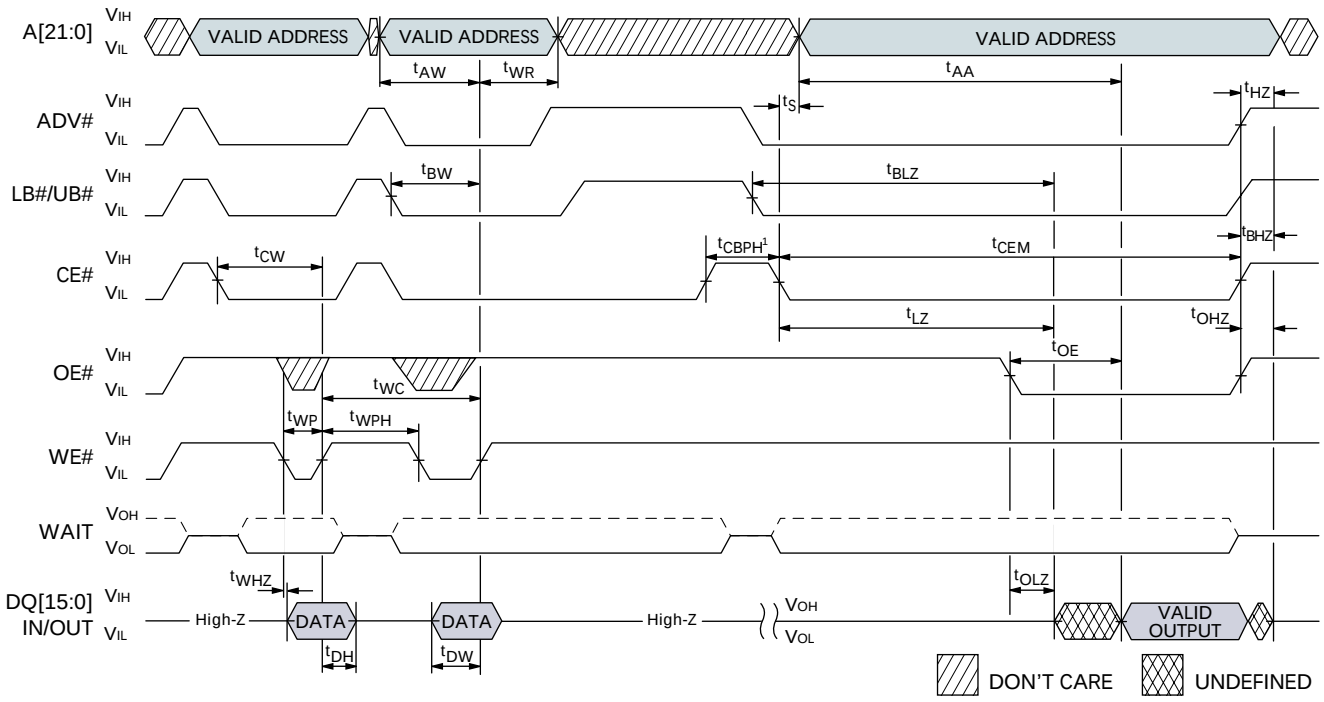
SYMBOL	-701, -706		-856		UNITS
	MIN	MAX	MIN	MAX	
^{t}WC	70		85		ns
^{t}WHZ	0	8	0	8	ns
^{t}WP	46		55		ns
^{t}WPH	10		10		ns
^{t}WR	0		0		ns

Table 42: READ Timing Parameters

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}ABA		33		55	ns
^{t}ACLK		6.5		10	ns
^{t}BOE		20		20	ns
^{t}CBPH	5		5		ns
^{t}CEW	1	7.5	1	7.5	ns
^{t}CLK	9.62	20	15	20	ns

SYMBOL	-701		-706, -856		UNITS
	MIN	MAX	MIN	MAX	
^{t}CSP	4	20	4	20	ns
^{t}HD	1		1		ns
^{t}KOH	2		2		ns
^{t}KP	3		3		ns
^{t}OHZ	0	8	0	8	ns
^{t}SP	3		3		ns

Figure 38: Asynchronous WRITE Followed by Asynchronous READ—ADV# LOW



NOTE:

CE# must remain HIGH for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.

Table 43: WRITE Timing Parameters

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns

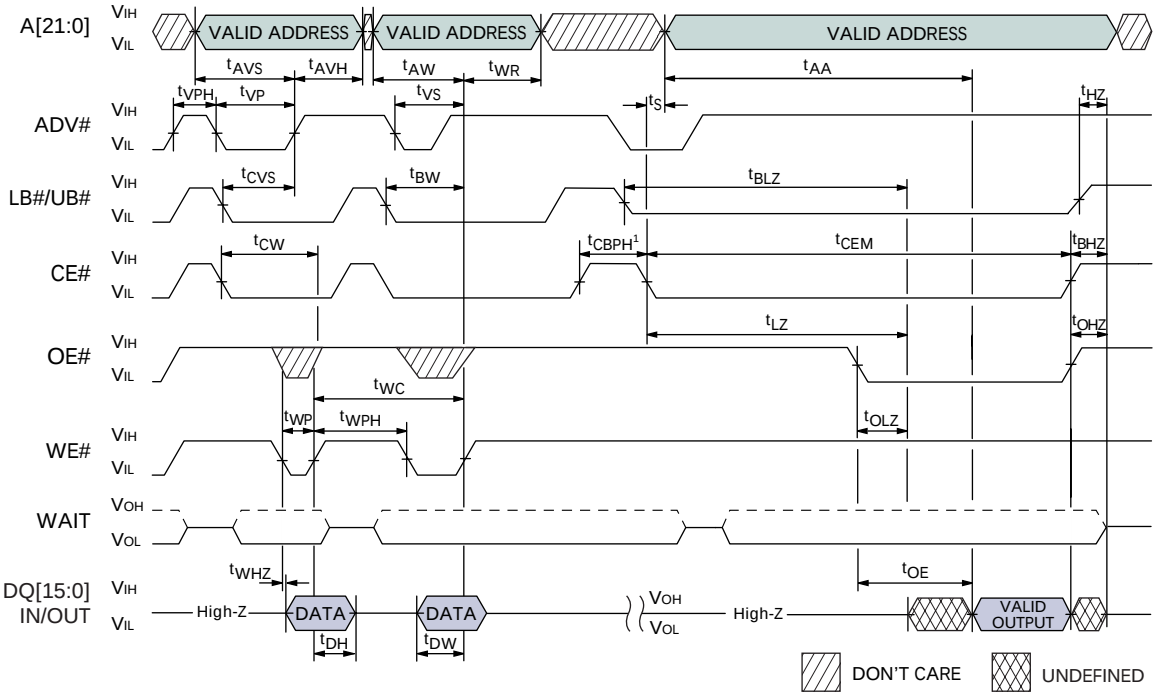
SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{WC}	70		85		ns
t_{WHZ}	0	8	0	8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Table 44: READ Timing Parameters

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AA}		70		85	ns
t_{BHZ}	0	8	0	8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEM}		10		10	µs
t_{HZ}	0	8	0	8	ns

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OHZ}	0	8	0	8	ns
t_{OLZ}	5		5		ns
t_{S}		10		10	µs

Figure 39: Asynchronous WRITE Followed by Asynchronous READ



NOTE:

CE# must remain HIGH for at least 5ns (t_{CBPH}) to schedule the appropriate internal refresh operation.

Table 45: WRITE Timing Parameters

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AVH}	5		5		ns
t_{AVS}	10		10		ns
t_{AW}	70		85		ns
t_{BW}	70		85		ns
t_{CVS}	10		10		ns
t_{CW}	70		85		ns
t_{DH}	0		0		ns
t_{DW}	23		23		ns

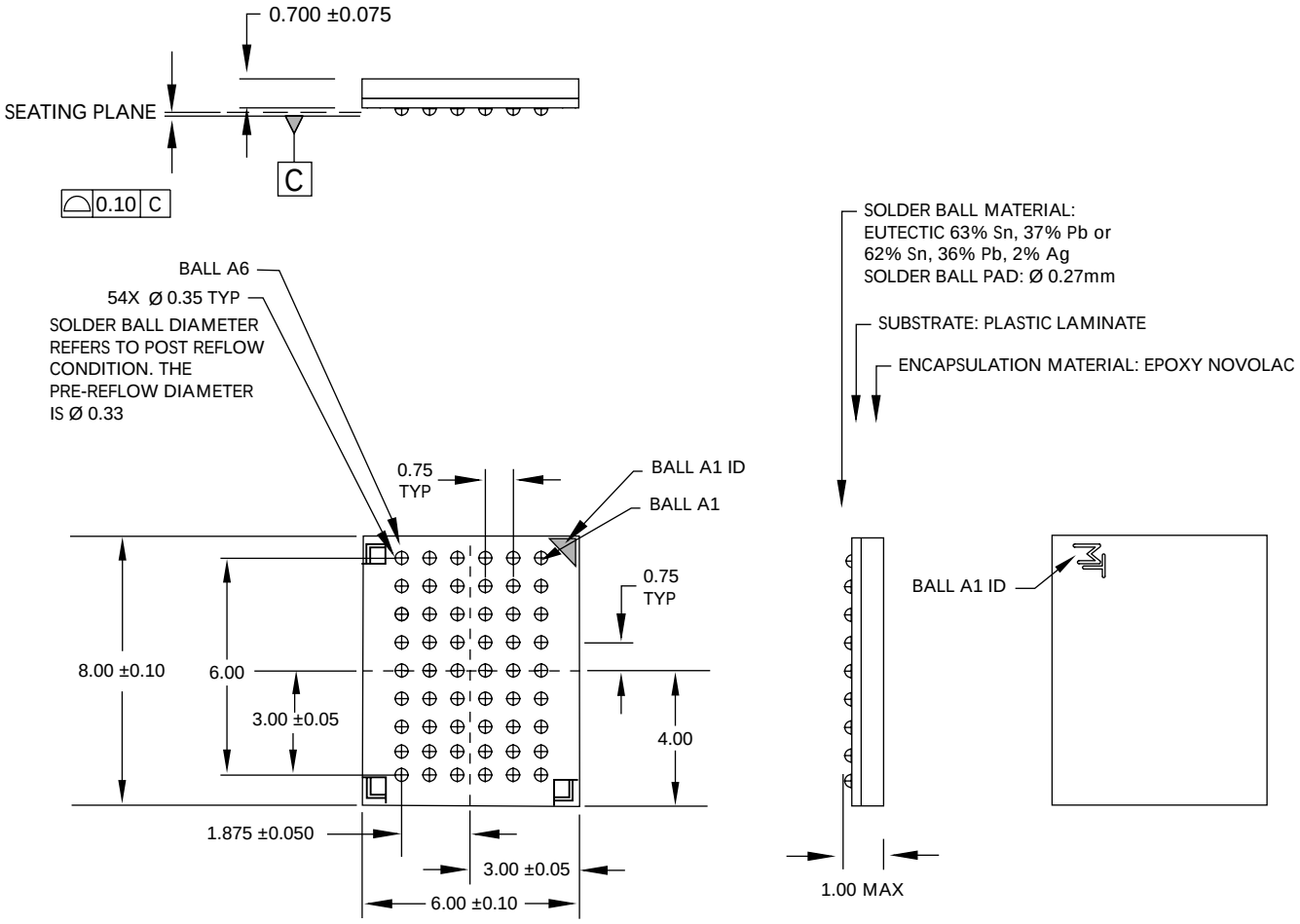
SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{VP}	10		10		ns
t_{VPH}	10		10		ns
t_{VS}	70		85		ns
t_{WC}	70		85		ns
t_{WHZ}	0	8	0	8	ns
t_{WP}	46		55		ns
t_{WPH}	10		10		ns
t_{WR}	0		0		ns

Table 46: READ Timing Parameters

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{AA}		70		85	ns
t_{BHZ}	0	8	0	8	ns
t_{BLZ}	10		10		ns
t_{CBPH}	5		5		ns
t_{CEM}		10		10	µs
t_{HZ}	0	8	0	8	ns

SYMBOL	-701, -706 MIN	-701, -706 MAX	-856 MIN	-856 MAX	UNITS
t_{LZ}	10		10		ns
t_{OE}		20		20	ns
t_{OHZ}	0	8	0	8	ns
t_{OLZ}	5		5		ns
t_{S}		10		10	µs

Figure 40: 54-Ball FBGA



NOTE:

1. All dimensions in millimeters; MAX/MIN, or typical, as noted.
2. Package width and length do not include mold protrusion; allowable mold protrusion is 0.25mm per side.

Data Sheet Designation: ADVANCE

This data sheet contains initial descriptions of products still in development.

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APPENDIX A

How Extended Timings Impact CellularRAM™ Operation

Introduction

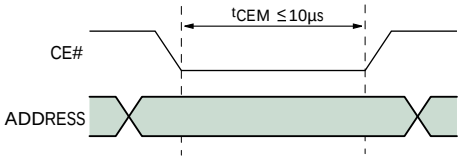
This note describes CellularRAM™ timing requirements in systems that perform extended operations.

CellularRAM products use a DRAM technology that periodically requires refresh to ensure against data corruption. CellularRAM devices include on-chip circuitry that performs the required refresh in a manner that is completely transparent in systems with normal bus timings. The refresh circuitry imposes constraints on timings in systems that take longer than 10µs to complete an operation. WRITE operations are affected if the device is configured for asynchronous operation. Both READ and WRITE operations are affected if the device is configured for burst-mode operation.

Asynchronous and Page-Mode Operation

CellularRAM products require that asynchronous WRITE operations must be completed within 10µs. After completing an operation, the device must either enter standby (by transitioning CE# HIGH), or perform a second operation using a new address. Figures 41 and 42 demonstrate these constraints as they apply during an asynchronous (page-mode-disabled) operation. Either the CE# active period (^{t}CEM in Figure 41) or the address valid period (^{t}TM in Figure 42) must be less than 10µs during any operation to accommodate orderly scheduling of refresh.

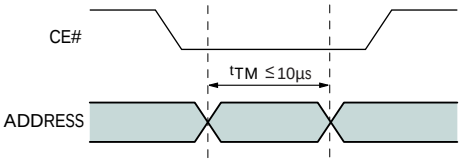
Figure 41: Extended Timing for ^{t}CEM



NOTE:

Timing constraints when page mode is disabled.

Figure 42: Extended Timing for ^{t}TM

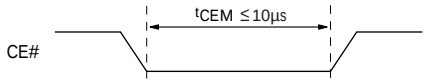


NOTE:

1. Timing constraints when page mode is disabled.

When a CellularRAM device is configured for page-mode operation, the address inputs are used to accelerate READ accesses and cannot be used by the on-chip circuitry to schedule refresh. CE# must return HIGH upon completion of all WRITE operations when page mode is enabled (see Figure 43 below). The total time taken for a WRITE operation should not exceed 10µs to accommodate orderly scheduling of refresh.

Figure 43: Extended Timing for ^{t}CEM[1]

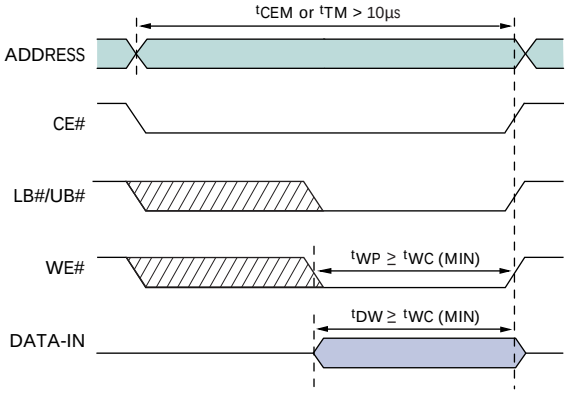


NOTE:

1. Timing constraints when page mode is enabled.

Modified timings are only required during extended WRITE operations (see Figure 44 below). An extended WRITE operation requires that both the WRITE pulse width (^{t}WP) and the data valid period (^{t}DW) be lengthened to at least the minimum WRITE cycle time (^{t}WC [MIN]). These increased timings ensure that time is available for both a refresh and successful completion of the WRITE operation.

Figure 44: Extended Asynchronous Write Operation



Burst-Mode Operation

When configured for burst-mode operation, it is necessary to allow the device to perform a refresh within any 10µs window. One of two conditions will enable the device to schedule a refresh within 10µs. The first condition is when all burst operations complete within 10µs. A burst completes when the CE# signal is registered HIGH on a positive (BCR[6] = 1) or a negative (BCR[6] = 0) clock edge. The second condition that allows a refresh is when a burst access crosses a row boundary. The row-boundary crossing causes WAIT to be asserted while the next row is accessed and enables the scheduling of refresh.

Summary

CellularRAM products are designed to ensure that any possible asynchronous timings do not cause data corruption due to lack of refresh. Slow bus timings will only affect asynchronous WRITE operations (READs are unaffected). The impact on asynchronous WRITE operations is that some of the timing parameters (^{t}WP and ^{t}DW) are lengthened. Burst mode timings must allow the device to perform a refresh within any 10µs period. A burst operation must either complete (CE# registered HIGH) or cross a row boundary within 10µs to ensure successful refresh scheduling. These timing requirements are likely to have little or no impact when interfacing a CellularRAM device with a low-speed memory bus.

Table 47: Revision History

CHANGE	DATE	CHANGED BY	DESCRIPTION
7	07/10/03	ddb	Input/Output leakage to 1µA. Added ^{t}AS, removed ^{t}S.
6	06/23/03	ddb	Incorporated Industrial Temperature data where applicable. Rounded initial latency and initial access to 39ns.
5	06/20/03	ddb	Added -706 part information where applicable.
4	06/19/03	ddb	Removed ^{t}SP and ^{t}HD from CE# in Burst diagrams.
3	06/18/03	ddb	Changed standby power to 90µA and 100µA as marked; changed specified values to “TBD.”
2	06/09/03	ddb	Absolute Maximum Signal Input value changed.
1	06/06/03	ddb	Initial release.