

MT3401A

P-Channel Enhancement Mode Field Effect Transistor

Product Summary

- $V_{DS} = -30V$
- $I_D = -4.2A$ ($V_{GS} = -10V$)
- $R_{DS(ON)} \leq 45m\Omega$ @ $V_{GS} = -10V$
- $R_{DS(ON)} \leq 55m\Omega$ @ $V_{GS} = -4.5V$
- $R_{DS(ON)} \leq 75m\Omega$ @ $V_{GS} = -2.5V$

Features

- Advanced Trench Process Technology.
- High dense cell design for ultra low $R_{DS(ON)}$.
- Lead free product is acquired.
- RoHS Compliant.

Applications

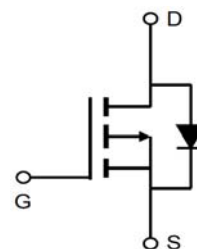
- Power Management in Notebook Computer
- Portable Equipment and Battery Powered Systems



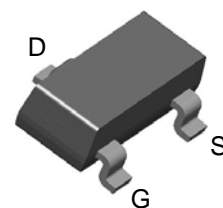
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Simplified Schematic



MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23-3L

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Steady State	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 12	V
I_D	Continuous Drain Current ¹	-4.2	A
I_{DM}	Pulsed Drain Current ²	-30	A
I_S	Continuous Source Current (Diode Conduction) ¹	-2	A
P_D	Maximum Power Dissipation ¹	1.25	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ C$

Notes:

1. Surface Mounted on 1" x 1" FR4 Board, $t \leq 10$ Sec.
2. Pulse width limited by maximum junction temperature.

Thermal Resistance Ratings

Symbol	Parameter		Typical	Maximum	Unit
R _{thJA}	Maximum Junction-to-Ambient	t ≤ 10 Sec	65	90	°C/W
		Steady State	85	125	
R _{thJF}	Maximum Junction-to-Foot (Drain)	Steady State	43	60	

Electrical Characteristics (T_A=25°C, unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
● Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = -250μA	-30	-	-	V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250μA	-0.7	-1	-1.5	V
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24V, V _{GS} = 0V	-	-	-1	μA
		V _{DS} = -24V, V _{GS} = 0V, T _J = 85°C	-	-	-30	
R _{DS(on)}	Drain Source On State Resistance ^a	V _{GS} = -10V, I _D = -4.2A		45		mΩ
		V _{GS} = -4.5V, I _D = -4A		55		
		V _{GS} = -2.5V, I _D = -1A		75		
g _{fs}	Forward Transconductance ^a	V _{DS} = -5V, I _D = -5A	7	11	-	S
V _{SD}	Diode Forward Voltage ^a	I _S = -1A, V _{GS} = 0V	-	-0.77	-1	V
● Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{DS} = -15V, V _{GS} =0V, f=1MHz	-	720	-	pF
C _{oss}	Output Capacitance		-	90	-	
C _{rss}	Reverse Transfer Capacitance		-	65	-	
Q _g	Total Gate Charge	V _{DS} = -15V, V _{GS} = -4.5V, I _D = -2.5A	-	11.5	14	nC
Q _{gs}	Gate-Source Charge		-	1.56	-	
Q _{gd}	Gate-Drain Charge		-	2.2	-	
t _{d(on)}	Turn-On Delay Time	V _{DD} = -15V, R _L = 15Ω I _D = -1.0A, V _{GEN} = -10V, R _G = 6Ω	-	8.3	12	nSec
t _r	Rise Time		-	7.6	15	
T _{d(off)}	Turn-Off Delay Time		-	26	46	
t _f	Fall Time		-	5.6	10	
R _g	Gate Resistance	V _{GS} =0, V _{DS} =0, f=1MHz	-	8	-	Ω
t _{rr}	Body Diode Reverse Recovery Time	I _F = -4A, di/dt = 100A/μs	-	11	-	nSec
Q _{rr}	Body Diode Reverse Recovery Charge		-	6	-	nC

Note:

a. Pulse test; pulse width ≤ 300μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

Characteristics Curve

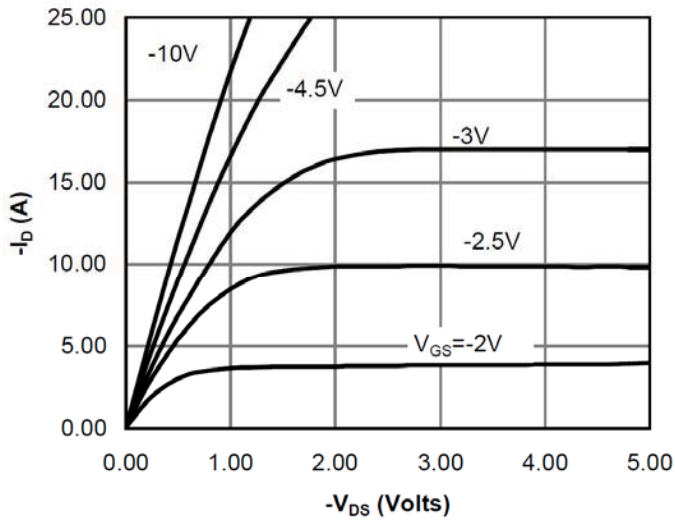


Fig 1: On-Region Characteristics

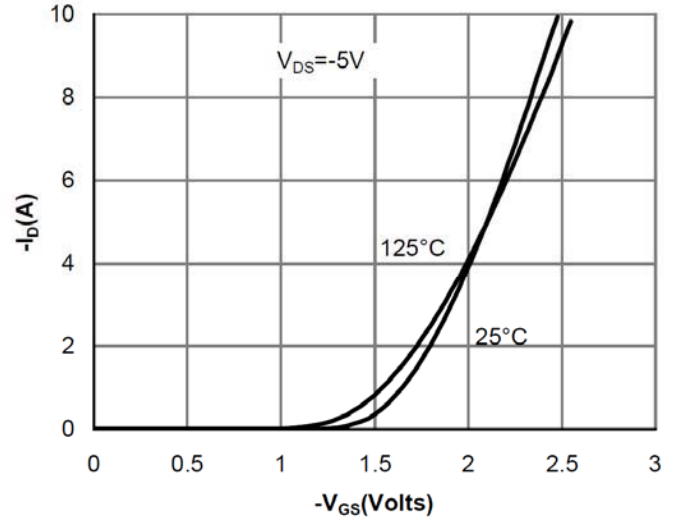


Figure 2: Transfer Characteristics

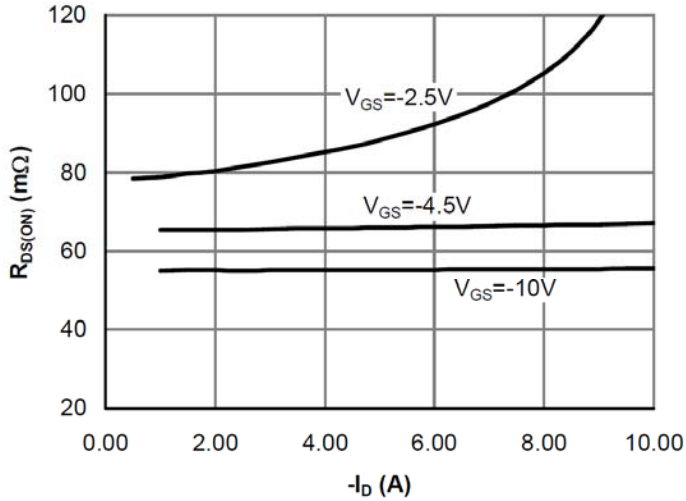


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

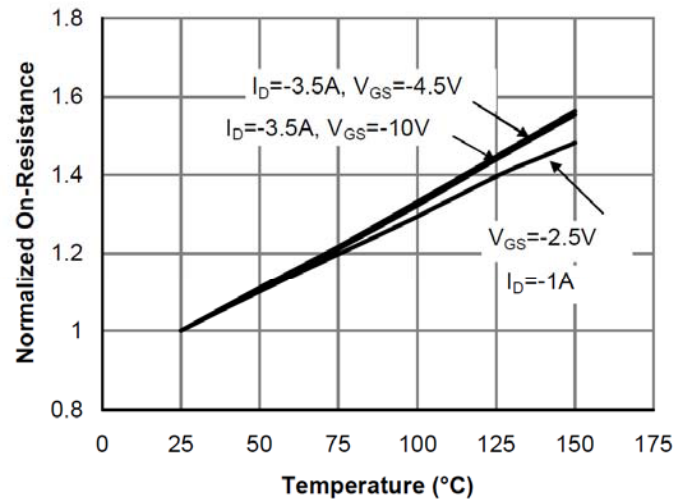


Figure 4: On-Resistance vs. Junction Temperature

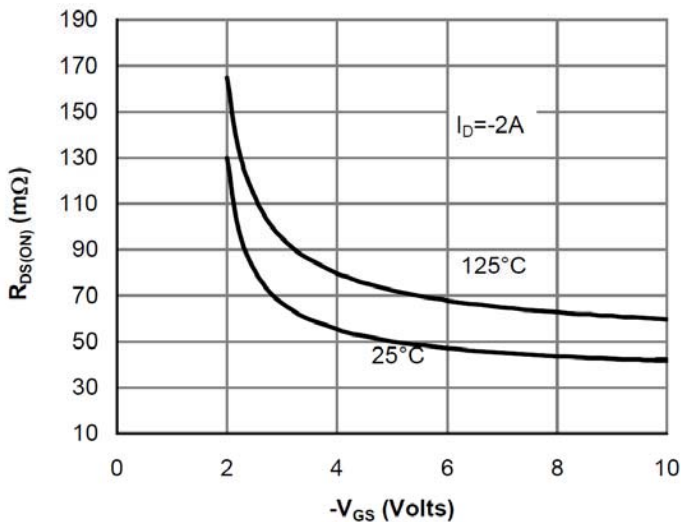


Figure 5: On-Resistance vs. Gate-Source Voltage

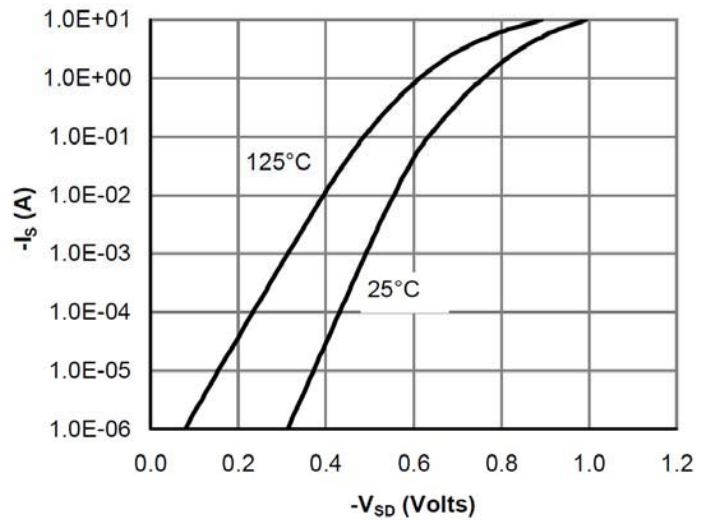


Figure 6: Body-Diode Characteristics

Characteristics Curve

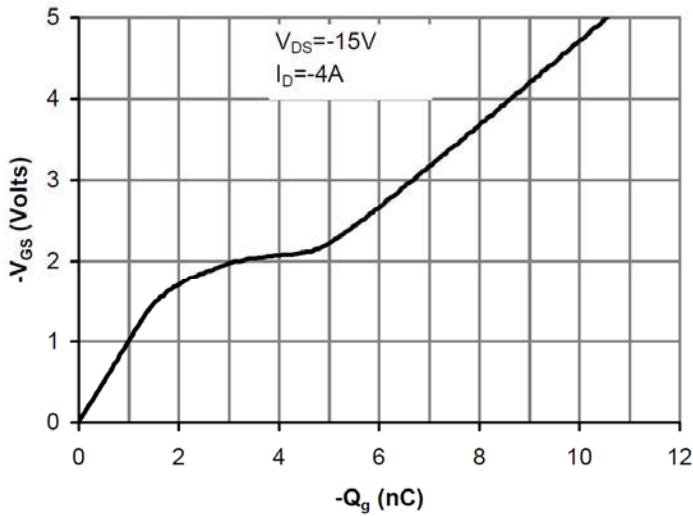


Figure 7: Gate-Charge Characteristics

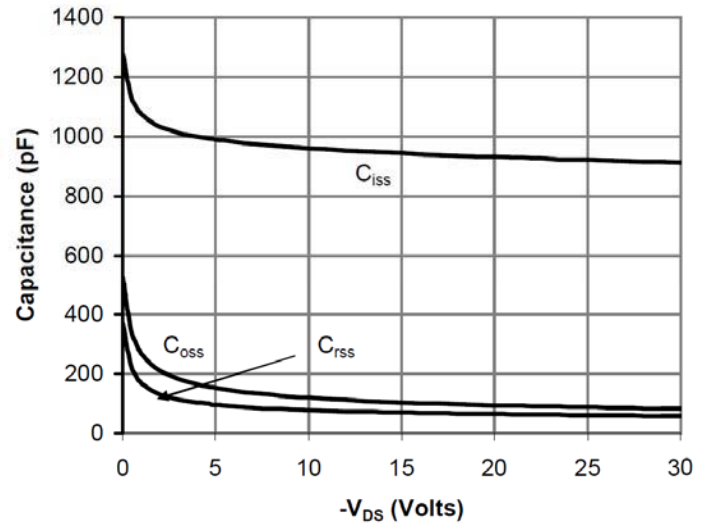


Figure 8: Capacitance Characteristics

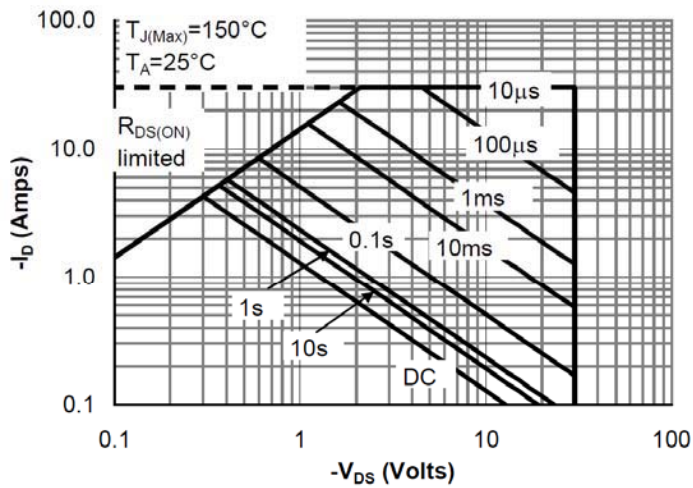


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

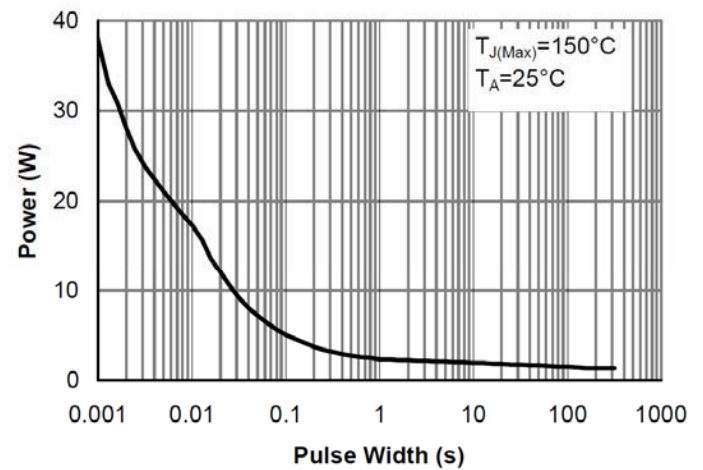


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

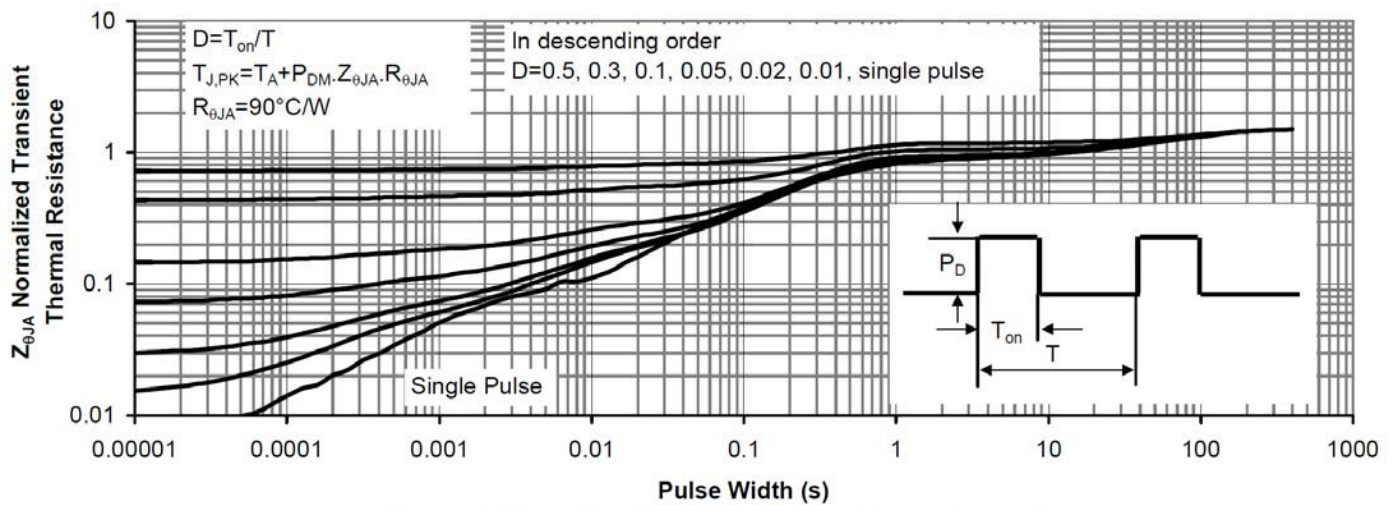
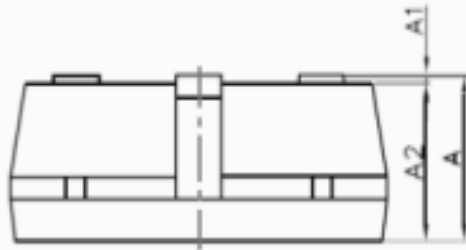
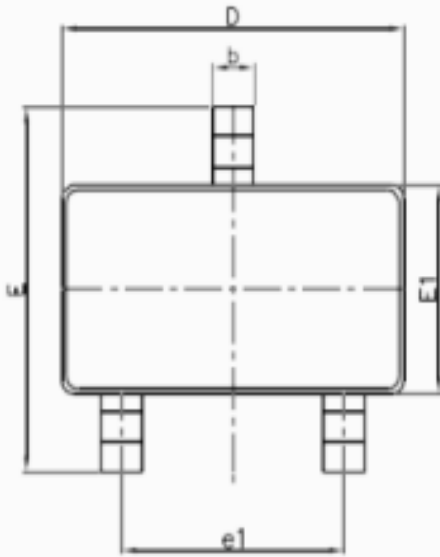


Figure 11: Normalized Maximum Transient Thermal Impedance

SOT-23-3L Package Outline Dimensions



DIM	MILLIMETERS
A	1.05~1.25
A1	0~0.1
A2	1.05~1.15
b	0.3~0.5
c	0.10~0.20
D	2.82~3.02
E	2.8~3.0
E1	1.5~1.7
e1	1.8~2.0
L	0.3~0.5

- NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH OR GATE BURRS.
MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 5 MILS EACH.
 2. TOLERANCE ± 0.100 mm (4 mil) UNLESS OTHERWISE SPECIFIED.
 3. DIMENSION L IS MEASURED IN GAUGE PLANE.
 4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
 5. ALL DIMENSIONS ARE IN MILLIMETERS.

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