MT3400

N-Channel Power MOSFET

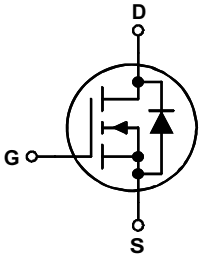
MT Semiconductor®

http://www.mtsemi.com

General Description

This N-Channel Logic Level MOSFET is produced using Mos-tech's Semiconductor's advanced PowerTrech process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

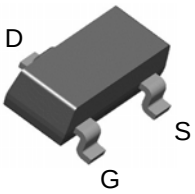
Simplified Schematic



Features

- 4.0 A, 30 V. $R_{DS(ON)}$ = 0.025Ω @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 0.042Ω @ V_{GS} = 4.5 V
- Very fast switching speed.
- Low gate charge (5nC typical)
- High performance version of industry standard SOT-23 package. Identical pin out to SOT-23 with 30% higher power handling capability.

MARKING DIAGRAM & PIN ASSIGNMENT



SOT-23-3L

Absolute Maximum Ratings (T_A = 25℃ unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Maximum Drain Current – Continuous	(Note 1a)	4.0	A
			10	
P_D	Maximum Power Dissipation	(Note 1a)	1.25	W
		(Note 1b)	0.76	
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	100	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
MT3400	MT3400	7”	8mm	3000 units

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA,Referenced to 25°C		21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		T_J = -55°C			10	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA		0.9	1.6	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA,Referenced to 25°C		–4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 2.7 A V_{GS} = 4.5 V, I_D = 2.4 A V_{GS} = 10 V, I_D = 2.7 A, T_J = 125°C		0.020 0.030 0.053	0.025 0.042 0.075	Ω
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	10			A
g_{FS}	Forward Transconductance	V_{DS} = 5V, I_D = 2.7 A		4.6		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		600		pF
C_{oss}	Output Capacitance			55		pF
C_{rss}	Reverse Transfer Capacitance			41		pF
R_G	Gate Resistance	f = 1.0 MHz		1.8		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		2.5		ns
t_r	Turn–On Rise Time			2.5		ns
$t_{d(off)}$	Turn–Off Delay Time			20		ns
t_f	Turn–Off Fall Time			4		ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 2.7 A, V_{GS} = 5 V		4		nC
Q_{gs}	Gate–Source Charge			0.6		nC
Q_{gd}	Gate–Drain Charge			1.5		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current				0.42	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.42 A (Note 2)		0.7	1.2	V
trr	Diode Reverse Recovery Time	IF = 2.7A, diF/dt = 100 A/μs		12	20	ns
Qrr	Diode Reverse Recovery Charge			3	5	nC

otes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.

b) 270°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics

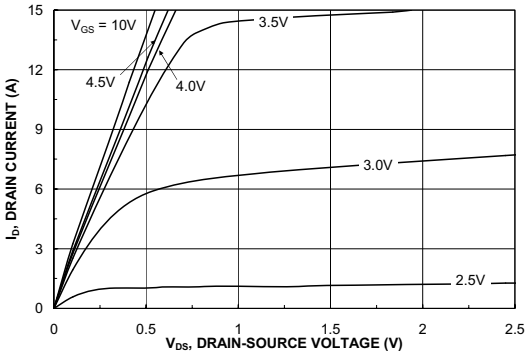


Figure 1. On-Region Characteristics.

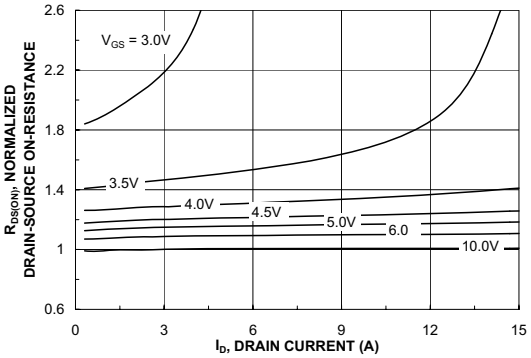


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

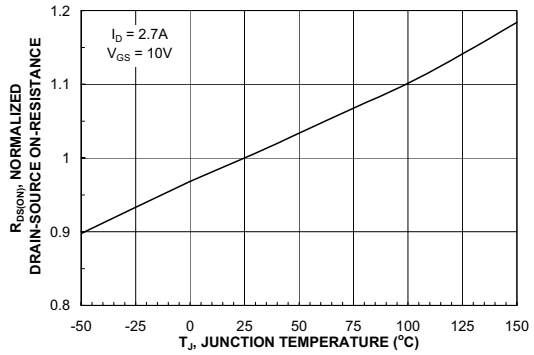


Figure 3. On-Resistance Variation with Temperature.

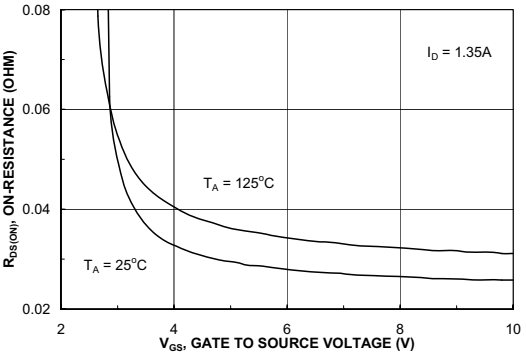


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

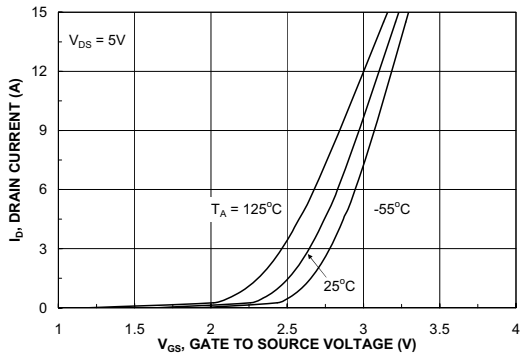


Figure 5. Transfer Characteristics.

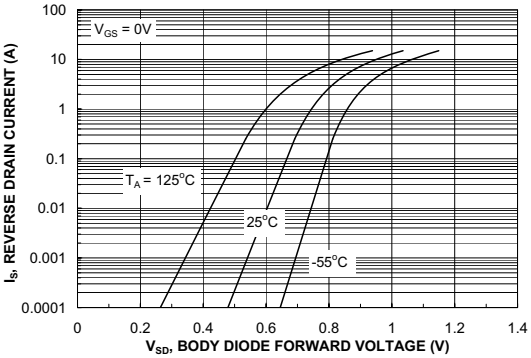


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

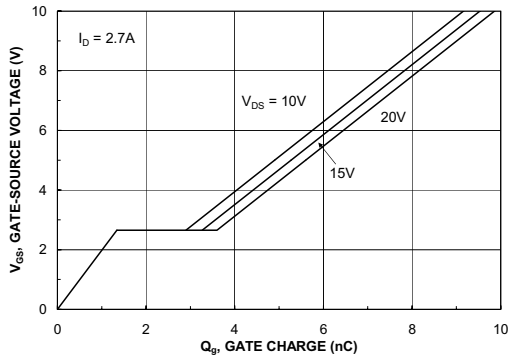


Figure 7. Gate Charge Characteristics.

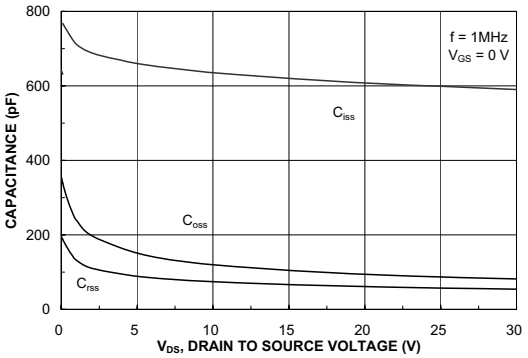


Figure 8. Capacitance Characteristics.

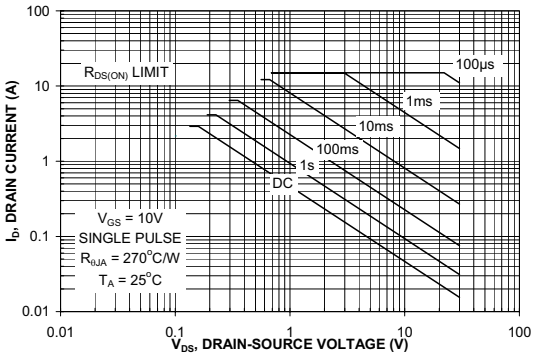


Figure 9. Maximum Safe Operating Area.

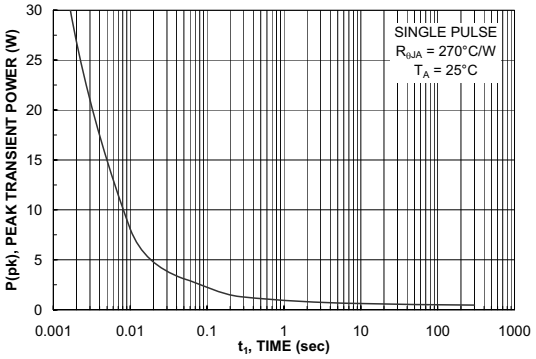


Figure 10. Single Pulse Maximum Power Dissipation.

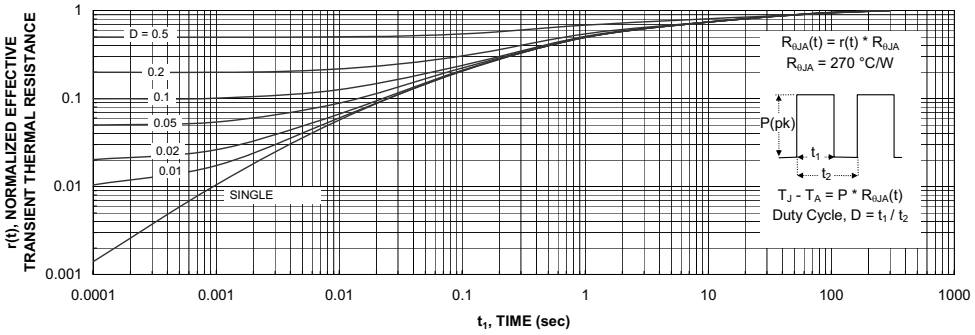
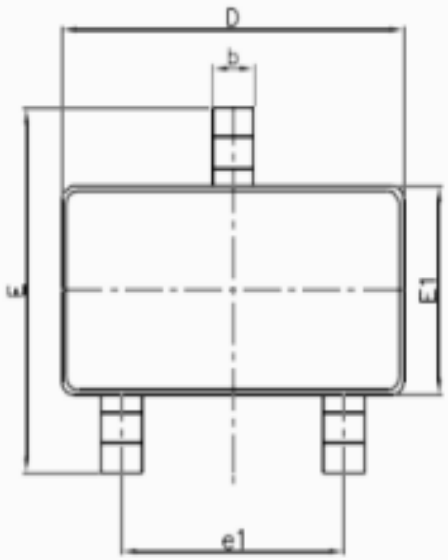
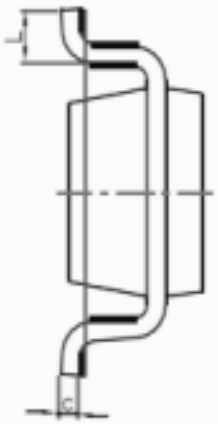


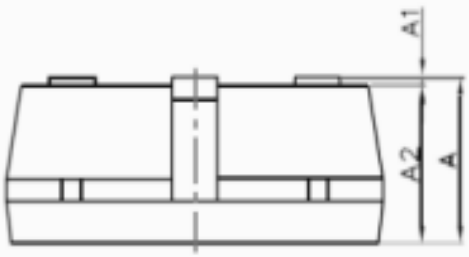
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

SOT-23-3L Package Outline Dimensions







DIM	MILLIMETERS
A	1.05~1.25
A1	0~0.1
A2	1.05~1.15
b	0.3~0.5
c	0.10~0.20
D	2.82~3.02
E	2.8~3.0
E1	1.5~1.7
e1	1.8~2.0
L	0.3~0.5

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH OR GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 5 MILS EACH.
2. TOLERANCE ±0.100 mm (4 mil) UNLESS OTHERWISE SPECIFIED.
3. DIMENSION L IS MEASURED IN GAUGE PLANE.
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS
   ARE NOT NECESSARILY EXACT.
5. ALL DIMENSIONS ARE IN MILLIMETERS.

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